O-J.04

Silicide Barrier SNS Junctions for AC Josephson Voltage Standards

Paul D. Dresselhaus, Yonuk Chong, Nicolas Hadacek, Burm Baek, Michio Watanabe, Charles J. Burroughs, and Samuel P. Benz

Abstract— **We have used $MoSi_2$ barrier superconductor-normal metal-superconductor (SNS) double stacked junctions to generate audio frequency ac waveforms with metrological accuracy. Circuits used in this experiment were two parallel arrays of 1280 stacks with 2 junctions per stack for a total of 5120 junctions per chip. Eliminating cross-talk between circuits, optimizing the output filter design, and implementing our flip-chip-on-flex technology allowed us for the first time to increase the operating margins to ± 1.5 mA on the dc bias while retaining 95 dB or better below the fundamental of distortion. These improvements allowed us to carefully investigate the metrology performance of the synthesized waveforms using a commercially available ac/dc thermal transfer standard. We measured ac/dc differences of less than 5 μV/V from 1 kHz to 5 kHz at an rms voltage of 100.00 mV. The ac Josephson reference has been found to be more stable and quieter than conventional voltage calibrators.**

I. INTRODUCTION

Superconductor-normal-metal-superconductor (SNS) Josephson junctions have proven to be an invaluable technology for voltage standard applications, particularly for ac voltages [1]. Arrays of several thousand junctions combine single flux quanta in-phase to produce 100 mV ac waveforms that have been used with metrological precision [2]. Circuits are made with Nb as a superconductor using a normal-metal barrier, and operate at 4 K. Higher voltages and increased junction density have been realized by vertically stacking SNS junctions. Similar circuits have been made elsewhere for voltage standard applications [3-4].

Understanding the device physics of these junctions has allowed us to tailor the desired junction characteristics for specific applications–either low speed junctions for low-voltage sources, or high-speed junctions for higher voltage–while maintaining the high critical currents and uniformity needed for large operating margins.

The choice of a normal-metal barrier is a key to well-behaved SNS junctions. The barrier must have both material and electrical properties conducive to high quality junctions. We have found a metallic silicide, particularly $MoSi_2$, to be an effective barrier material. Metallic silicides are generally etchable in fluorine chemistry and compatible with the Nb etch, thus allowing vertical stacking of the junctions.

II. NORMAL-METAL BARRIERS

We have successfully used three different metallic silicides for normal-metal barriers–WSi_2, $TiSi_2$, and $MoSi_2$. Each of these materials is normal at 4K and all etched well in the SF_6 plasma used for etching the Nb. The resistivity of the silicide is 230 μΩ·cm for WSi_2 and $TiSi_2$, and 650 μΩ·cm for the $MoSi_2$. This large resistivity range produces a correspondingly large range in critical current density, which is advantageous for exploring different applications.

All of the metallic silicide barrier devices have proven to be very reproducible, presumably because the boundary condition at the normal-metal/superconductor interface is rigid: thus the superconducting order parameter changes very little inside the superconductor [5]. Note that this is not the case in lower resistivity films such as PdAu where the superconducting order parameter has a large variation inside the superconducting electrodes. This variation negatively affects junction reproducibility because the order parameter suppression is highly dependent on the quality of the barrier, the superconducting film, and the interface.

Both the WSi_2 and $TiSi_2$ materials had measured superconducting transitions below our 4 K operating temperature–$TiSi_2$ at 1.72 K and WSi_2 at 2.85 K. The disadvantage of operating near the superconducting transition of the barrier is that the junction electrical properties are very sensitive to temperature variations. Nevertheless, devices using these barriers allowed us to study the SS'S junction system–in which the barrier is near the superconducting transition [5]. Because the $MoSi_2$ material had no measurable superconducting transition down to 100 mK, we use this barrier for the SNS junctions in our metrology applications.

III. CIRCUITS

In order to fabricate Josephson voltage standards with useful output levels, thousands of SNS junctions are needed in a circuit that operates from dc to microwave frequencies. The use of metal silicide barriers and their inherent etching properties allows us to decrease the total length of the array by vertical stacking of the Josephson junctions. Typically double-junction stacks can be fabricated with little or no loss of either

---

P.D. Dresselhaus, Y. Chong, N. Hadacek, B. Baek, M. Watanabe, C.J. Burroughs, and S.P. Benz are with the National Institute of Standards and Technology, Boulder, CO 80305 USA. Y. Chong's present Address is Korea Research Institute of Standards and Science, Daejeon 305-600, Korea; e-mail : yonuk@kriss.re.kr

This work was supported in part by Office of Naval Research contract N0001405IP20017. Contribution of the National Institute of Standards and Technology, not subject to copyright.

margins (due to nonuniformity) or yield (due to etch-loading) across the wafer. Triple-junction stacks may also be fabricated with good uniformity, but, using our present etch recipe, the yield is high only in the middle of the 76 mm diameter wafer. Higher stacks suffer similar problems with yield, but short (1000-stack) arrays with 10 junctions per stack have been fabricated with uniform junction critical currents and constant voltage steps with applied microwave power [6].

The junction stacks are embedded in a 50 Ω coplanar superconducting transmission line with a 50 Ω termination resistor at the bottom. Inductive taps are placed at either end of the array for low-speed (DC - 1 MHz) bias and output voltage measurement. Typically two arrays are series-connected on a single chip to increase the total output voltage. Thus our cryoprobe has two separate microwave transmission lines for the two independent arrays. In addition to high-speed signals, the arrays are current biased with low-speed signals, either at the fundamental output frequency for ac synthesis or with dc bias for dc synthesis.

For ac waveform generation it is important to minimize coupling of all ac signals between the two arrays. Crosstalk between the arrays at any frequency, but in particular from out-of-band (>1 MHz) quantization harmonics, will reduce the operating margin and degrade the circuit performance. We found that on-chip connections between the two arrays caused decreased margins with respect to uncoupled arrays because the high-frequency filtering was insufficient to decouple the arrays. Therefore for the work in this paper, we used two arrays that were coupled off-chip.

Designing filters to project a high impedance broadband filter to the microwave tap, while retaining low impedance for low-frequency audio signals was another important issue. SPICE simulations were performed over a number of different designs to optimize the filter design parameters. Care was taken to remove any microwave resonances caused by the inductive taps in the circuit, while increasing the inductance to get the maximum high-frequency rejection.

IV. MEASUREMENTS

Driving the arrays with the electronics as described in Ref. 1, a sine-wave code is run at 10 Gb/s with a 15 GHz sine drive. The code is designed such that the amplitude is exactly 100 $\mathrm{mV_{rms}}$ at a frequency of 2.5 kHz. The two series-connected arrays each contain 1280 double-junction stacks for a total of 5120 junctions for both arrays. The operating margins are checked by sweeping a global bias current while observing the output spectrum: if the spectrum shows no distortion greater than 95 dB from the fundamental tone (-95 dBc), the circuit is defined as being "on margins." For a 10 mA critical current array, typical margins for good circuits are 3 mA for a 100 $\mathrm{mV_{rms}}$, 2.5 kHz tone.

In order to make a metrological measurement of the ac voltage, we measured the waveform using an ac-dc thermal transfer standard that compares the power from the ac source with an equal power from a dc source. Using this technique it is possible to measure the dc-equivalent voltage with an accuracy of better than 0.1 μV on a 100 mV signal. The Josephson array is then driven with a code to produce a dc tone at ±100 mV such that a direct dc-ac comparison may be made. Low-pass filters prevent out-of-band microwave signals from reaching the thermal transfer standard.

We measured ac-dc differences of less than 10 μV/V for a frequency range of 1.25 kHz to 5 kHz using the ac-dc thermal transfer standard. At 10 kHz and higher frequencies error signals that reduce the accuracy arise from parasitic effects of the output transmission line and filters. We believe that this is due to unwanted currents at the fundamental frequency flowing through the output leads.

The thermal transfer standard is also used to determine the true operating margins for precision voltage synthesis. The output voltage is measured while varying each of the input parameters to the array – the so-called "flat-spot" measurement [2]. Using this more sensitive measurement technique, we find that the margins needed for precision voltage measurement at a 1 μV/V uncertainty are much smaller than the margins needed to reduce distortion to -95 dBc. For these 100 mV measurements the 3 mA distortion margin was more than twice as large as the 1.2 mA margin for the precision voltage flat-spot at 1 μV/V uncertainty. This 1.2 mA dc bias margin occurred while varying each of the remaining bias parameters over ±5 % of their applied values [7].

V. CONCLUSIONS

We fabricated metal silicide-barrier stacked junction arrays with improved circuits that allowed us for the first time to demonstrate accurate ac voltage metrology measurements. This quantum voltage reference was measured with a thermal ac-dc transfer standard and shown to be accurate to better than 10 uV/V at 100 $\mathrm{mV_{rms}}$ at frequencies below 5 kHz. The accuracy and range of this measurement could be extended with improved filtering of the output voltage.

ACKNOWLEDGMENT

We thank Joe Kinard and Tom Lipe at NIST for helpful conversations and for use of their ac-dc transfer standard.

REFERENCES

[1] S.P. Benz, C.J. Burroughs, P.D. Dresselhaus, "Low Harmonic Distortion in a Josephson Arbitrary Waveform Synthesizer," *Appl. Phys. Lett.*, vol. 77, no. 7, pp. 1014-1016, Aug. 2000.

[2] C.J. Burroughs, S.P. Benz, P.D. Dresselhaus, Y. Chong, "Precision Measurements of AC Josephson Voltage Standard Operating Margins," *IEEE Trans. Instrum. Meas.*, vol. 54, no. 2, pp. 624-627, Apr. 2005.

[3] R. Pöppel, D. Hagedorn, T. Weimann, F-I. Buchholz, and J. Niemeyer, Supercond. Sci. Technol. **13**, 148 (2000).

[4] H. Yamamori, M. Itoh, H. Sasaki, A. Shoji, S. P. Benz, and P. D. Dresselhaus, Supercond. Sci. Technol. **14**, 1048 (2001).

[5] Y. Chong, N. Hadacek, P.D. Dresselhaus, C.J. Burroughs, and S.P. Benz, "Properties of Josephson Junctions with Superconducting Metal Silicide Barriers," submitted to *Appl. Phys. Lett.*

[6] N. Hadacek, P.D. Dresselhaus, Y. Chong, S.P. Benz, and J. Bonevich, "Fabrication and Measurement of Tall Stacked Arrays of SNS Josephson Junctions," to be published in *IEEE Trans. Appl. Supercond.* 2005.

[7] C.J. Burroughs, S.P. Benz, P.D. Dresselhaus, Y. Chong, "Precision Measurements of AC Josephson Voltage Standard Operating Margins," *IEEE Trans. Instrum. Meas.*, vol. 54, no. 2, pp. 624-627, Apr. 2005.