Spatial distributions of trapping centers in HfO_2/SiO_2 gate stacks

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A methodology to analyze charge pumping (CP) data, which allows positions of probing traps in the dielectric to be identified, was applied to extract the spatial profile of traps in SiO_2/HfO_2 gate stacks. The results suggest that traps accessible by CP measurements in a wide frequency range, down to few kilohertz, are located within or near the interfacial SiO_2 layer rather than in the bulk of the high-k film. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2195896]

As the gate oxide thickness of metal-oxide semiconductor field effect transistors (MOSFETs) is scaled down, gate leakage current increases exponentially raising concerns about power dissipation and the reliability of traditionally used silicon dioxide.[1–4] To reduce the large gate leakage while further scaling oxide thickness, gate dielectric materials with high dielectric constants (high-k), in particular HfO_2 and Hf silicates, have been proposed to replace SiO_2.[5–7] However, these materials, as other transition metal oxides, exhibit a high density of intrinsic electron traps.[8,9] The growth of Hf-based oxides on the Si substrate by any deposition method is known to lead to the formation of a multilayer dielectric stack, which includes a SiO_2 layer at the interface between the Hf film and the substrate. This interfacial layer, whose properties are strongly process dependent, is suggested to be essentially substoichiometric,[10,11] which would result in a higher density of the electron traps. Therefore, to evaluate high-k dielectrics and deposition methods, it is critical to separate contributions from the traps in high-k film and the interfacial layer to device electrical characteristics. Knowing the spatial distribution of the traps affecting transistor performance can help in understanding the physical nature of the defects.

Charge pumping (CP) has been widely used to study interface traps in Si/SiO_2 system for more than 30 years.[12,13] It has been shown qualitatively that, by changing the pulse frequency of the CP measurement, the trap probing in the Si/SiO_2 system can be controlled.[14,15] In this work, we first describe a quantitative model for interpreting the probing depth dependence of the CP measurements under various test conditions (frequency, raise/fall time, amplitude, etc.). We then apply the developed model to the HfO_2/SiO_2 system having various SiO_2 interface thickness values.

The devices used in this work are fully processed MOSFETs with HfO_2/SiO_2 stacked gate dielectrics. High-k gate dielectric transistors were fabricated on 200 mm $p/p+$ epitaxial Si<100> wafers using a standard complementary metal-oxide-semiconductor process with 1000 °C/10 s dopant activation anneal. The gate stacks were formed by depositing a 3 nm ALD HfO_2 dielectric on various scaled thermal oxide interface layers (ILs). A gate electrode was formed by chemical vapor deposition TiN with a poly-Si cap.[16] CP measurements were performed by applying periodic trapezoidal pulses with a fixed rise/fall (t_r/t_f) time and amplitude (V_a) to the gate. The dc electron-hole recombination current was measured from the substrate. To probe traps at different depths in the dielectric, pulse on and off times (t_{on} and t_{off}) were kept of equal value and varied from 50 ns to 100 ms.

The generalized CP equation can be expressed as[17]

$$I_{CP,MAX} = qfA_G N_{mit} = qfA_G \int_0^{x_{min}} \int_{E_{min}}^{E_{max}} N_t(x,E_t)\Delta F(x,E_t)dE_t dx, \quad (1)$$

where N_{mit} (cm^{-2}) is the total measured trap density per unit area during the CP measurement and could be expressed as a double integral of multiplication of N_t and ΔF. N_t is the trap volume density (cm^{-3}), and ΔF indicates the probability that a trap can be probed by CP measurement. Both of these are functions of the distance from the Si-substrate/gate-dielectric interface (x) and the trap energy (E_t). Figure 1 shows a three-dimensional (3D) simulation contour of ΔF as a function of

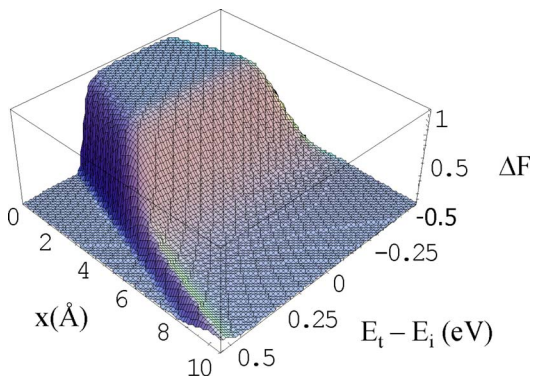

FIG. 1. 3D ΔF contour simulation result. ΔF is equal to one within the trapezoidal plateau, which indicates the region having the maximum probability of being probed. The parameters used in this simulation are $t_{on/off}$=50 ns, $t_{r/f}$=30 ns, V_a=1.2 V, $m_{e/h}$=0.5/0.4 eV, $\Phi_{e/h}$=3.1/3.8 eV, and $\sigma_{n/p}(0)=10^{-14}/10^{-16}$ cm^{-2}.

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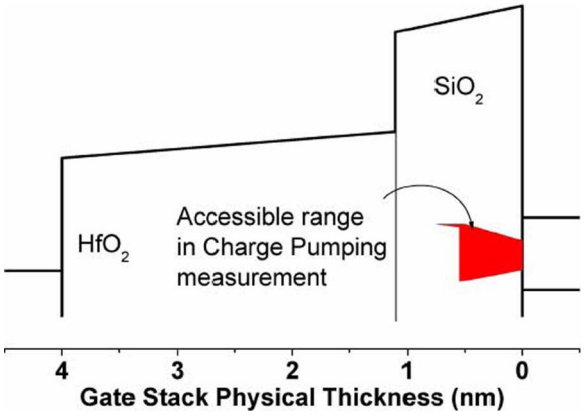

FIG. 2. Schematic of the band diagram for the high-k gate stack. The CP accessible range for the employed CP measurements conditions is shown overlapping the band diagram.

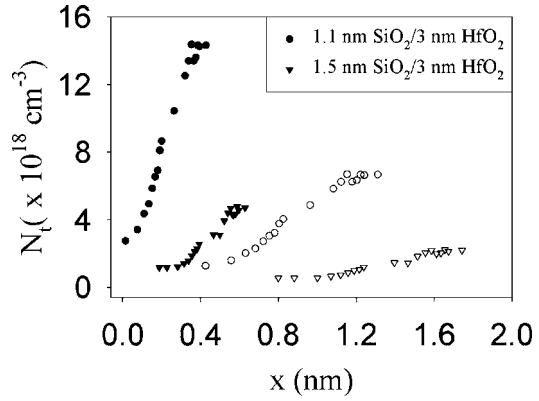

FIG. 4. The comparison of N_t in dielectrics with different thicknesses of the SiO_2 interfacial layer. The pure SiO_2, SiO_2/HfO_2 diffusion, and pure HfO_2 regions can be identified clearly in both dielectrics.

E_t and x. Traps located inside the trapezoidal plateau with ΔF equal to 1 have the maximum probability of being probed and contribute to $I_{CP,MAX}$ during the CP measurement. Details of the simulation can be found elsewhere.[15] It can be seen that ΔF drops from 1 to 0 at approximately 0.3 nm. Traps beyond this depth are not detectable by CP. Therefore, the maximum depth probed by CP (x_{max}) can be defined. The parameters used in this simulation are also shown in the figure. The accessible range during CP and the band diagram were schematically shown in Fig. 2. It suggests that detectable traps by CP are most likely to be located within the interfacial layer.

Figure 3 shows the total measured trap density per unit area (N_{mit} cm^{-2}) as a function of t_{on}/t_{off} for devices with interfacial layer oxide thicknesses ranging from 1.1 nm to 1.9 nm. N_{mit} for a control SiO_2 dielectric is also shown for comparison. The values of N_{mit} at the smallest t_{on}/t_{off} (or x) for all dielectrics are very similar, which suggests that all dielectrics have approximately the same number of traps within the SiO_2 interfacial region. These traps are attributed to the commonly observed interface traps at the Si/SiO_2 interface. The SiO_2 control shows a constant N_{mit} throughout

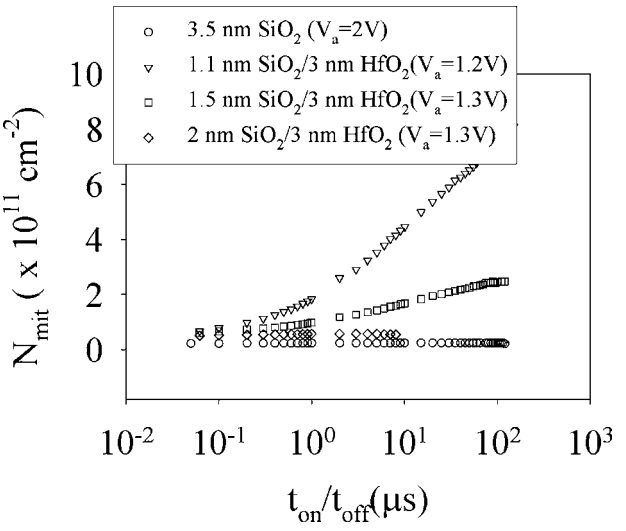

FIG. 3. The comparison of N_{mit} in dielectrics with different thicknesses of the SiO_2 interfacial layer. At the same depth, N_{mit} is higher for the dielectric with a thicker interfacial layer. As for the SiO_2 dielectric, N_{mit} is constant, which indicates no further traps exist in the bulk dielectric.

the detectable depth range. It suggests that all of the traps are located near the Si/SiO_2 interface, which is expected and is consistent with observations from other groups.[12,13] For HfO_2/SiO_2 stacks, N_{mit} increases with depth and N_{mit} at a given depth decreases with increasing SiO_2 interfacial layer thickness. The thickest interfacial layer (1.9 nm) shows behavior similar to that of the control SiO_2 dielectric. This suggests that the 1.9 nm interfacial layer is sufficiently thick that the depth probed by CP does not reach the transition region between the SiO_2 and HfO_2 layers.

To obtain the trap volume density, N_t (cm^{-3}), the derivative of $N_{mit}(x)$ with respect to x is taken and the result is shown in Fig. 4. Since the dielectric with a 1.9 nm SiO_2 interfacial layer does not indicate the measurement of the SiO_2/HfO_2 interface, only dielectrics with thinner SiO_2 interfacial layers are plotted. It should be recalled that the relationship between t_{on}/t_{off} and x is affected by values of dielectric parameters such as effective electron/hole mass inside the dielectric ($m_{e/h}$), effective electron/hole barrier height ($\Phi_{e/h}$), electron and hole capture cross section at the substrate/IL interface [$\sigma_{n/p}(0)$], and V_a.[12,13] In Fig. 4, N_t is plotted as a function of x by using two different sets of parameters under the simplified assumption of a homogeneously thick dielectric. For the solid symbols, the parameters are $m_{e/h}=0.5/0.4$ eV, $\Phi_{e/h}=3.1/3.8$ eV, $\sigma_{n/p}(0)=10^{-14}/10^{-16}$ cm^{-2}, which are the commonly accepted values for pure SiO_2.[18,19] The trapping appears to occur within the first 5 Å of the 1 nm interfacial layer by using these parameters. These traps may be generated by the interaction between HfO_2 and the interfacial layer, which was modified by the HfO_2 film and became oxygen deficient.[10,11]

To estimate the upper depth limit for traps probed by the CP measurements, a set dielectric parameters corresponding to HfO_2 was employed: $m_{e/h}=0.1/0.1$ eV (the smallest values reported), $\Phi_{e/h}=1.5/3.1$ eV, $\sigma_{n/p}(0)=10^{-14}/10^{-15}$ cm^{-2} (Ref. 20) (σ_p is chosen to be an order of magnitude larger than SiO_2), as open symbols in Fig. 4. Even with this set of parameters, which favor deeper penetration, the accessible traps are still located within the interfacial layer, and their density gradually increases toward the interface with the high-k film. As can be seen in Fig. 4, the N_t distributions for the gate stacks with 1.1 and 1.5 nm interfacial SiO_2 layer are shifted with respect to each other by approximately 0.3 nm, which is close to the difference between the SiO_2 interfacial layer thicknesses. This indicates that although the exact

probing depth is unknown, the relative trap spatial distribution is accurate.

The results of this study clearly show that the trap density in the high-k gate stack increases with CP probing depth, from the Si/SiO_2 interface toward the SiO_2/HfO_2 region. This trap profile appears to reflect on structural modifications of the interfacial SiO_2 layer by the overlaying HfO_2 film. The spatially deepest traps accessible by the CP measurements at the kilohertz range are located within or near the interfacial layer rather than in the bulk of the HfO_2 film. This result suggests that the quality of the interfacial layer in high-k gate dielectric stacks may represent an important factor that significantly affects high-k transistor performance.

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