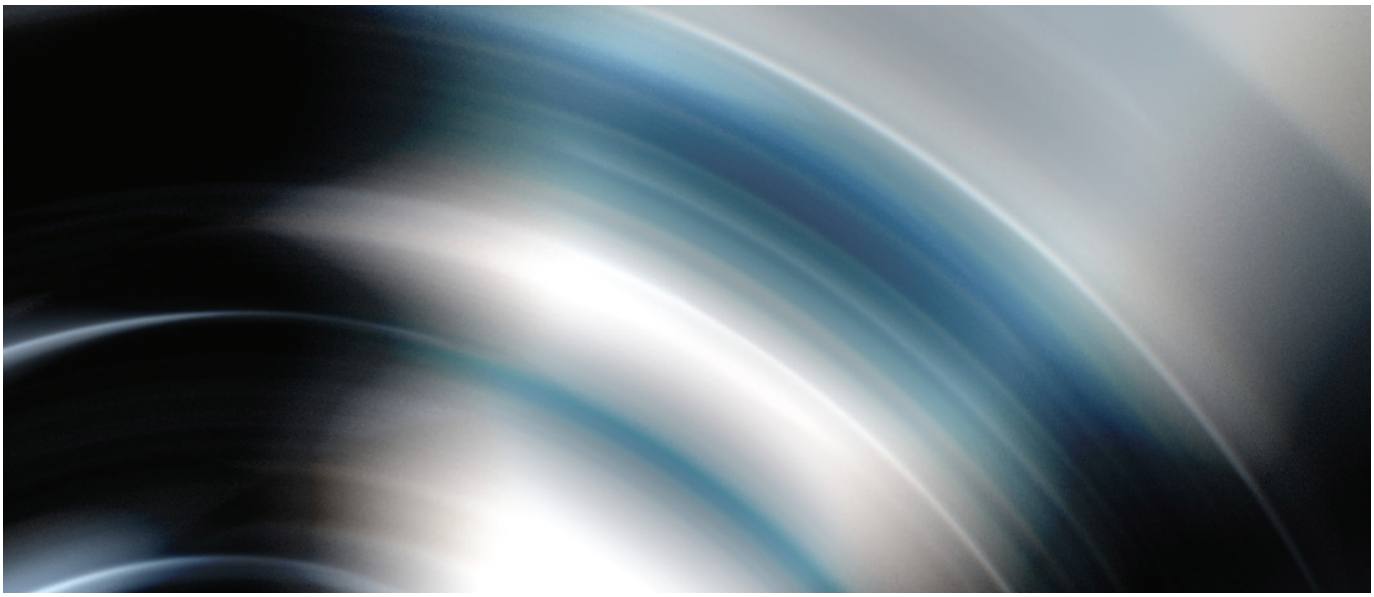

100 mV AC-DC Transfer Standard Measurements Using An AC Josephson Voltage Standard

C.J. Burroughs, S.P. Benz, and P.D. Dresselhaus[1]

Abstract: NIST is implementing the Josephson arbitrary waveform synthesizer as an ac Josephson Voltage Standard (ACJVS). Over the past few years we have demonstrated precise measurements of synthesized sine waves at rms voltage amplitudes up to 170 mV. The system can generate a variety of precision voltage outputs including dc voltages and ac sinewaves, so it can be used as a quantum-based voltage source for ac metrology. In this paper, we explore the capability of the ACJVS as an audio frequency calibration source for the lower voltage ranges of an ac-dc transfer standard such as the 220 mV range where the transfer standard uses a high-impedance input buffer amplifier. In particular, we investigate the ACJVS measurement accuracy over the frequency range from 1 kHz to 10 kHz at 50 mV and 100 mV. This work demonstrates the feasibility of a practical ac Josephson voltage standard based upon a quantum voltage source that produces precisely calculable ac and dc voltages.

1. Introduction

For a number of years, NIST has been developing a Josephson arbitrary waveform synthesizer and utilizing this technology to create an ac Josephson Voltage Standard (ACJVS) system. This system can generate a variety of precision voltage waveforms, including single-tone ac sinewaves and dc voltages so that it can be used as a quantum-based voltage source for ac metrology. The present system uses a chip with two Josephson arrays and digital-to-analog conversion techniques based on delta-sigma modulation [1], in which a digital data stream at 10 Gbit/s is combined with a 15 GHz sinusoidal drive signal for a maximum bipolar pulse-repetition frequency of 1.5×10^{10} pulses/s. This combined signal is fed to the Josephson junctions, which precisely quantize the pulses, thus producing a nearly ideal delta-sigma pulse train and a precisely known output waveform. The unprecedented accuracy of this technique for generating ac and dc waveforms for voltage metrology has been discussed previously [2-5].

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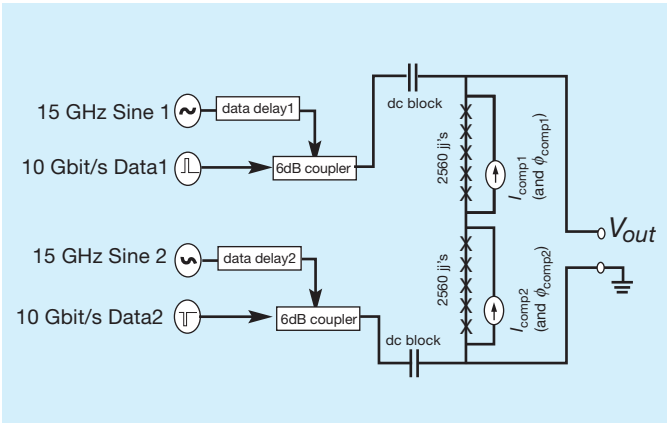

Figure 1. ACJVS circuit diagram for the dual-array Josephson chip illustrating the ten individual bias parameters.

We have fabricated and tested a number of different chip designs to determine how best to realize an ACJVS system. Most of our previous circuits have used a dual Josephson array configuration with as many as 8200 Josephson junctions to produce voltages as high as 242 mV (zero-to-peak) for ac waveforms, and ±254 mV for dc voltages. Having reasonable operating margins, these circuits allowed us to perform practical metrology measurements with rms amplitudes up to 170 mV. The results presented in this paper are from another dual-array chip with 5120 total junctions that was designed for optimum performance at a lower 100 mV_{rms} output voltage. With shorter arrays and fewer junctions, there is less dissipation of the high frequency pulses from the beginning of the arrays to the end. This results in better overall signal uniformity at microwave frequencies, and allows the bias parameters to have larger ranges over which the chip operates properly. In fact, this chip design demonstrates significantly improved margins for every bias parameter as compared to our previous chips with longer arrays. These new circuits also use our new double-stacked $MoSi_2$ junction-barriers [6-8], with pairs of junctions vertically stacked on top of each other. The stacked junctions provide improved uniformity of junction characteristics due to the larger junction area, and reduce the array length by half. Operating margins were also improved because the shorter arrays use shorter on-chip transmission lines with only a single 180 degree turn. Operating margins were also enhanced through improved on-chip filters. Finally, contact reliability and chip lifetime have been improved by permanently soldering the chips to 'flip-chip on flex' carriers [9].

Figure 1 shows the bias circuit for the ACJVS where the two arrays are connected in series on-chip so that their low-frequency output voltages add. This configuration allows either end of the dual-array circuit to be connected directly to ground, an essential feature for connecting the ACJVS output to spectrum analyzers, ac-dc thermal transfer standards, and other ac and dc voltage metrology instruments. A number of circuit innovations on the chip make this configuration possible, and those details have been presented elsewhere [5].

In order for the ACJVS to produce the correct output voltage, there are ten independent bias parameters in Fig. 1 that must all be set to the correct value. Complementary sources symmetrically bias the two individual arrays. Bipolar current pulses are applied to each array by combining three separate biases, namely, a 10 Gbit/s broadband digital waveform from a digital code generator (DCG), a 15 GHz microwave sinusoidal drive (Sine), and a low-speed compensation current (audio frequency or dc). The two high frequency signals (Data and Sine) are combined using 6 dB couplers and applied to each array through separate 10 MHz dc blocks that act as high-pass filters, removing the low frequency components of the broadband waveform. This is important to reduce common mode signals on transmission-line termination resistors (not shown) [5]. The two low-speed bias currents to each array (I_{comp1} or I_{comp2}) are applied by means of a programmable arbitrary waveform generator (AWG) through a battery-powered, floating differential preamplifier.

The DCG clock, the two AWGs, and the two microwave sine generators are all locked to a common 10 MHz reference to ensure relative phase stability for each source. The relative phase of the microwave generators and the AWGs can be independently adjusted with respect to the DCG clock using separate phase shifters (data delay1 and data delay2). Internal AWG controls (ϕ_{comp1} and ϕ_{comp2}) allow the compensation currents also to be phase shifted relative to the data signals. The digital bit-stream (Data2) to the Array 2 is the logical complement of the bit-stream (Data1) to Array 1, which results in an output waveform of opposite sign. Therefore, the two Josephson arrays are connected end-to-end at the microwave terminations so that the two array output voltages add. The compensation currents flow separately through each array, and do not provide any load current for $V_{out.}$ An additional output current could be used in order to provide source current to a low impedance device under test.

2. Operating Margin Optimization

In order to prepare the ACJVS for comparison with other instruments and reference standards, we first measure the operating margins for the Josephson circuit to determine the set-points for each of the ten bias parameters described above. We use the term 'operating margins' to represent the region in the ten-parameter space where each junction in each array is generating precisely one quantized pulse for every input pulse. Furthermore, for the ACJVS system to truly meet the definition of an 'intrinsic' ac and dc standard, there must be a finite range for each bias parameter over which the output voltage does not measurably change [3]. Every time the ACJVS system is used for a precision measurement, this multi-dimensional 'flat spot' in the operating margins needs to be confirmed for each synthesized output waveform. For the ACJVS to be a useful standard, all ten bias parameters must have a measurable 'flat spot' where the output voltage is constant at the level of parts in 10^6 or better.

To center each bias parameter value within a few percent, the set-points are determined using an oscilloscope and a spectrum analyzer in a procedure that previously has been described in detail [10]. Our spectrum analyzer has enough dynamic range to verify that distortion harmonics are –95 dBc [dB below the fundamental (carrier)], which is sufficient to confirm that con-

Parameter	Set Point	Margin
Data Amplitude 1	1.53 V	±5 %
Data Amplitude 2 (complement)	1.52 V	±10 %
RF Power (Sine 1)	35.1 mW	saturated
RF Power (Sine 2)	39.1 mW	±17 %
Data Delay 1	0 ps	±11 %
Data Delay 2	0 ps	±11 %
I_{comp1}	12 mA	±5.5 %
I_{comp2}	12 mA	±5.5 %
ϕ_{comp1}	0°	±10°
ϕ_{comp2}	0°	±10°

Table 1. ACJVS Operating Margins for a 100 mV_{rms} sinewave at 2.5 kHz for all ten bias parameters.

tributions to the rms voltage due to those harmonics are well below the required level of precision. However, since the spectrum analyzer is always measuring such a large signal at the fundamental frequency, it has limited ability to measure error signals occurring at that same frequency. In order to ensure the accuracy of the ACJVS we must verify through flat-spot measurements that the output does not include any in-phase error sources at the fundamental frequency. Such error signals would add directly to the output rms value [not as a root sum of the squares (RSS) contribution as in the case of distortion harmonics] [11]. To fully characterize the ACJVS operating margin flat-spots with the necessary precision, we measure the ACJVS output with an ac-dc transfer standard that is highly sensitive to any changes in the rms voltage applied to its input, especially at the fundamental frequency.

In these experiments, we use the transfer standard on its 220 mV full-scale range where it has a high-impedance buffer amplifier on its input so that the ACJVS supplies a minimal load current. To measure rms voltage, the transfer standard uses a power detector called a thermal voltage converter (TVC). It responds to the total rms voltage delivered to its input over a wide bandwidth (dc to many megahertz), so the full spectrum that the ACJVS generates in that band is included in the rms voltage measurement by the transfer standard. For our ACJVS

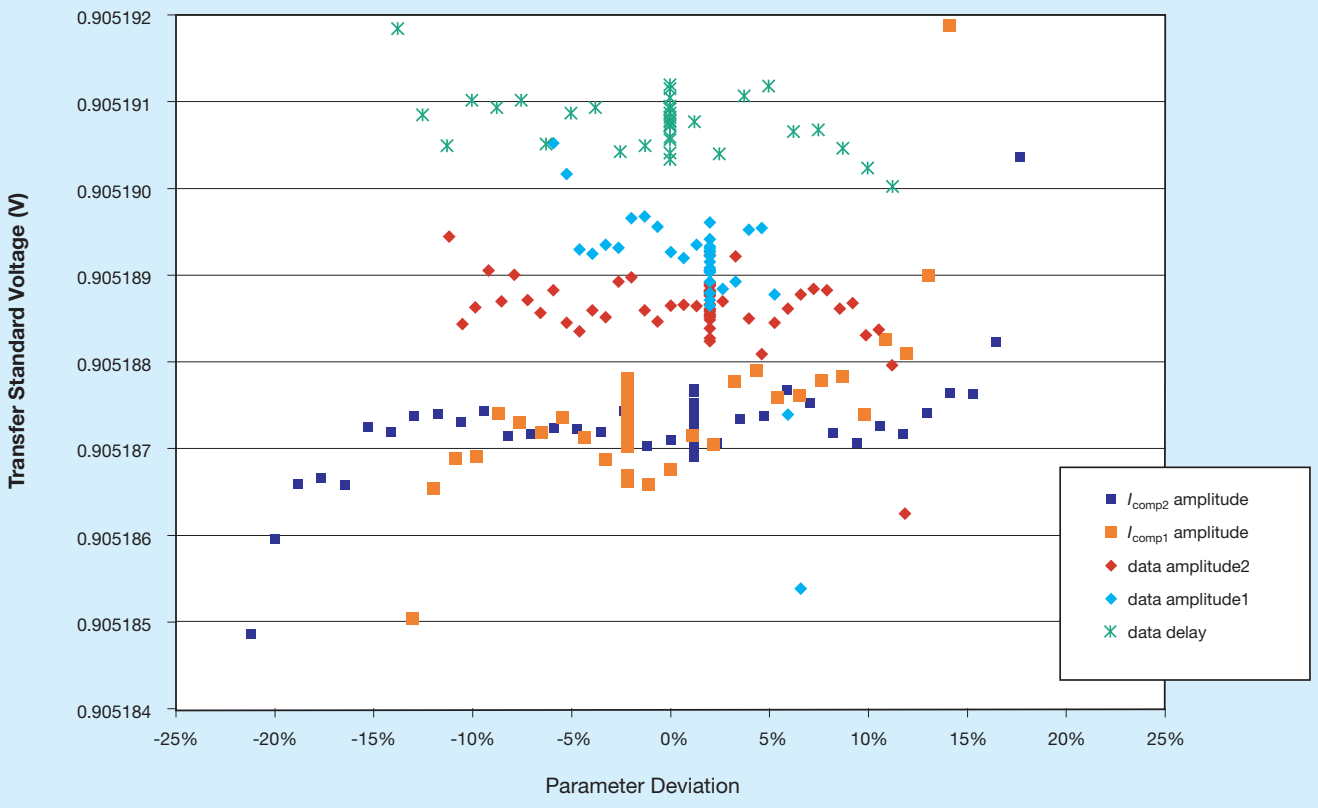

Figure 2. Plot showing the operating margins obtained using the ac-dc transfer standard and illustrating the 'flat-spots' for the five most critical parameters: I_{comp1}, I_{comp2}, data amplitude1, data amplitude2 (complement), data delay (both 1 & 2 moved together). One vertical division in this graph represents 1.1 parts in 10^6. Each cluster of points near 0% is caused by repeated measurement of this point that gives an indication of the overall noise and drift during each 3 minute data set. (Alternatively, this repetitive data near 0 % could be used to subtract the drift to first order).

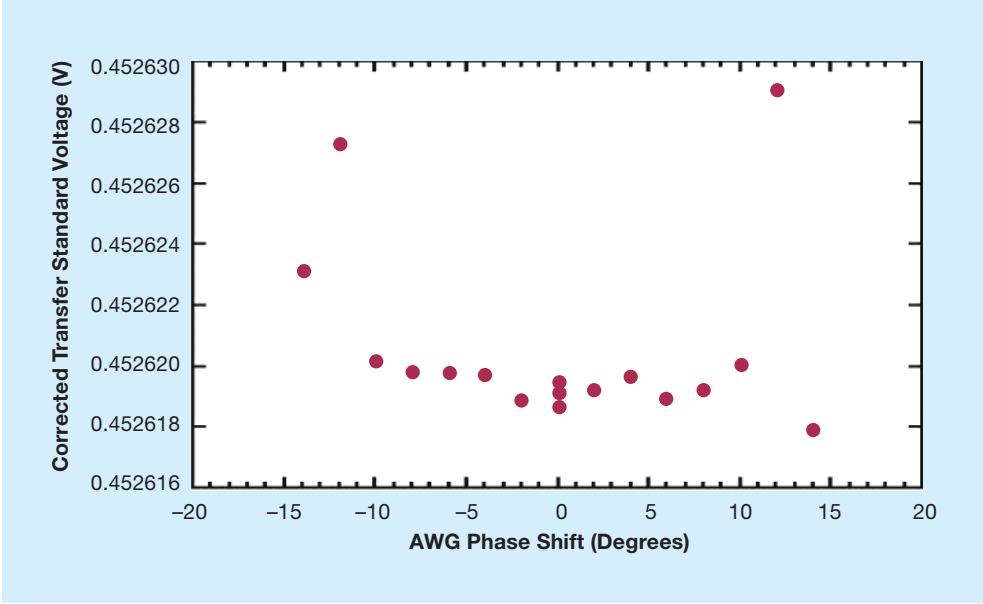

Figure 3. Measured flat-spot of the Array 2 output voltage as a function of the AWG phase ϕ_{comp2} after the slope due to the on-chip inductance has been subtracted. This data was for a single array producing a 50 mV_{rms} sinewave at 10 kHz. One vertical division in the graph corresponds to 4.4 parts in 10^6.

flat-spot measurements, the transfer standard allows us to determine the range over which the Josephson output signal remains constant for each of the ten bias parameters to better than a part in 10^6. Table 1 shows the measured set-points and margins of all ten bias parameters for a dual-array chip (design 18B with 5120 total junctions) generating a 100 mV_{rms} sinewave at 2.5 kHz using a 4 000 000 bit code at a data rate of 10 Gbit/s. The margins over which each parameter can be varied without changing the output voltage are significantly larger (a factor of 2 in most cases) for this 18B chip design as compared to data that we have reported previously [10].

The flat-spot measurement data of the five most critical parameters in Table 1 for this transfer standard are presented in Fig. 2, where each vertical division corresponds to 1.1 parts in 10^6. We define the 'flat spot' to be the range over which each parameter can be adjusted while the ACJVS output voltage measured by the ac-dc transfer standard remains constant within the measurement noise level (peak-to-peak scatter typically less than one part in 10^6). During the 30 minutes over which these measurements were made, the median output voltage of the transfer standard drifted up 3.3 parts in 10^6 from 0.9051875 V to 0.9051905 V. This slow drift occurred because the absolute gain of the transfer standard changed slightly with environmental conditions as the instrument was reaching thermal equilibrium after being turned on. The transfer standard output voltage, which is measured with a digital voltmeter, monotonically increased as the data was taken in the order suggested by the graph (first I_{comp2}, then I_{comp1}, data amplitude2, data amplitude1, data delay). Each data point is an average of four digital voltmeter measurements at 20 power line cycles each. Using such fast averaging, each bias parameter can be measured in only 3 minutes, allowing us to confirm that the ACJVS output is constant over each bias parameter range (flat spot) to a few parts in 10^7. With a factor of two to four longer averaging time, we could reduce the noise floor for these flat-spot measurements to 1 to 2 parts in 10^7.

The fact that Fig. 2 shows flat-spots for data amplitude1, data amplitude2, I_{comp1} and I_{comp2} is significant because it shows that the I/O coupling (the in-phase pickup of ac voltage from either the DCG or the AWGs) for these terms at this fundamental frequency is below the noise floor. This is critically important since uncertainty of the ACJVS output would increase dramatically if there were an appreciable slope for any of these four bias parameters. We have measured such I/O coupling in previous bias configurations in which the compensation biases were not independent.

Next we discuss the flat-spot measurement of the Josephson arrays as a function of the compensation phase shift ϕ_{comp}. For simplicity, the discussion assumes that only a single array is biased. The on-chip low-frequency bias connections use inductive coils to increase the lead impedances, thereby improving the broadband on-chip transmission of the data signals. In this present chip design, the compensation current also drives this inductance, which produces a voltage V_L that is 90 degrees out of phase with the voltage from the Josephson array V_J at the fundamental frequency. Unfortunately, when we change the compensation phase, some of this inductive signal adds in phase with the Josephson signal, resulting in the measured output voltage

$$V_{out} = \sqrt{(V_J + V_L \cdot \sin(\phi_{comp}))^2 + (V_L \cdot \cos(\phi_{comp}))^2}$$

where ϕ_{comp} is the phase shift from the ideal compensation phase, in this case $\phi_{comp} = 0$.

When we initially set the ACJVS bias parameters using the oscilloscope and the spectrum analyzer, the optimization procedure sets the compensation phase ϕ_{comp} to nearly 0, the ideal value, so the equation reduces to

$$V_{out} = \sqrt{V_J^2 + V_L^2} \quad .$$

This is as expected because V_L is 90 degrees out of phase and combines with V_J as the square root of the sum of the squares when V_J and I_{comp} are precisely time aligned. When we vary ϕ_{comp} to measure its flat-spot, we actually measure a slope that is linear with ϕ_{comp} over the region that the Josephson junctions remain on margins (exactly one output Josephson pulse for every input current pulse). Figure 3 shows the flat-spot measurement of Array 2 at a frequency of 10 kHz with the slope due to the inductive voltage V_L subtracted. For small phase shifts, as in this case, the inductive voltage component that is in phase

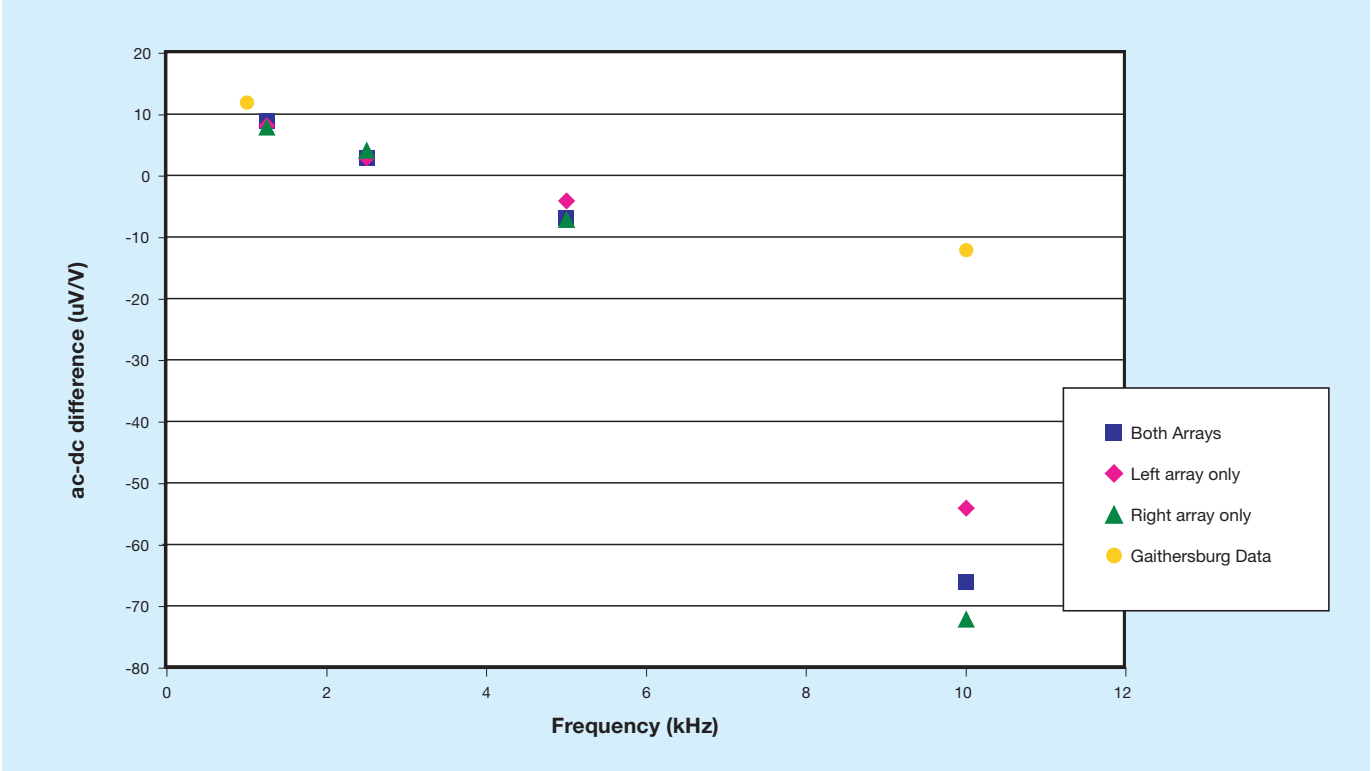

Figure 4. Measured ac-dc differences for an ac-dc transfer standard on its 220 mV range. Data points in blue, pink and green were measured using the ACJVS (uncertainty values for this new system have not yet been determined). The yellow points show measurements of the same instrument using conventional ac dc metrology techniques.

with the Josephson voltage is approximately given by $V_L \cdot \phi_{comp}$ The graph shows that the Josephson junctions themselves remain on margins up to about ±10 degrees, and the slope correction agrees with our expectations based upon separate measurements of V_L with the Josephson junctions off (about 30 μV at 10 kHz for I_{comp2}). Since the slope with respect to ϕ_{comp} increases linearly as the fundamental frequency increases, the alignment of ϕ_{comp} becomes increasingly important as the ACJVS frequency increases. For example, at 2.5 kHz, we can move ϕ_{comp} approximately only ±0.2 degrees before the measured in-phase inductive voltage becomes evident above the noise. However, because there is excellent phase stability in low-speed audio sources, achieving this phase stability is not difficult. Since V_L can be accurately measured and modeled, we can easily account for it in our measurements when it becomes significant for frequencies above 10 kHz. In future chip designs, we will add separate on-chip taps for compensation bias and output voltage, so that this inductive signal will be 100 times lower.

Finally, the largest ACJVS margins shown in Table 1 are for the 15 GHz microwave signals. The power level for Sine2 can be moved ±17 % with the output voltage remaining on a flat-spot. However, we discovered later that the power amplifier on the Sine1 bias is in saturation, which means that the amplifier is delivering a nearly constant power without regard to the input level applied. We would need to repeat the experiment with another amplifier that does not saturate to determine an actual margin for Sine1 power, but we expect that the margin on this parameter is similar to Sine2. Since Array 1 is clearly getting lower power than Array 2 due to the saturated amplifier, we believe this may explain why the flat-spot for data amplitude1 is smaller than that for data amplitude2 in Figure 2 (and in Table 1).

3. AC-DC Difference Measurements

After using the transfer standard extensively to measure ACJVS operating margins and 'flat spots", we then used it to assess the accuracy of the ACJVS delivered signal by measuring ac-dc differences. Figure 4 shows the ac-dc difference measured at several audio frequencies synthesized by the ACJVS source with the amplitudes of the ac and dc (both positive and negative polarity) waveforms set at precisely 100 mV_{rms}. The plot also shows the ac-dc difference measured with the individual Josephson arrays (1 and 2) turned on independently, resulting in two 50 mV_{rms} ac-dc comparisons. All measurements were performed on the 220 mV range of the transfer standard. We expect the ac-dc difference measured for the two separate arrays to match exactly since the rms voltage output should be identical in both cases. Furthermore, assuming reasonable linearity of the transfer standard, we expect the ac-dc difference with both arrays on (100 mV_{rms}) to be similar (within a few parts in 10^6) to that of the individual arrays (50 mV_{rms}) at each frequency, but not necessarily identical since the input power to the transfer standard is different by a factor of four.

The ac-dc differences shown in Fig. 4 are in good agreement with each other as expected at 1.25 kHz, 2.5 kHz, and 5 kHz. The plot also includes ac-dc difference data for this transfer standard at 1 kHz and 10 kHz measured by NIST Gaithersburg

using conventional build-down methods. Around 1 kHz, the conventional value is in reasonable agreement with our results. However, at 10 kHz there appears to be an inconsistency since the left and right arrays do not agree with each other, and the 10 kHz ACJVS points are clearly outside the general trend of the conventional calibration data. The problem appears to scale with increasing frequency, and requires further investigation because all indications are that both Josephson arrays are on operating margins with 'flat spots' for all bias parameters. However, since the ACJVS has been able to produce consistent ac-dc difference results at lower frequencies, we believe that we will be able to resolve this issue for operation at 10 kHz and above.

4. Conclusion

We have demonstrated significant improvements in operating margin range and flatness for a dual-array ACJVS system generating 100 mV_{rms} from 1.25 to 5 kHz. We have used the ACJVS as a precision source at this amplitude to measure the ac-dc transfer difference of a transfer standard and found reasonable agreement (from 1.25 to 5 kHz) with values determined for the transfer standard using conventional methods. We discovered that at 10 kHz and above the ACJVS needs further characterization to determine why the left and right array output voltages disagree with each other and with the conventional calibration data. Nevertheless, for the first time we have shown that potential errors due to I/O coupling from the bias electronics to the ACJVS output are not a significant problem in the present system configuration.

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