Metrology for High-Voltage, High-Speed Silicon-Carbide Power Devices[†]

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Abstract: *Performance metrics and test instrumentation needs for emerging high-voltage, high-speed SiC power devices are described. Unique power device and package thermal measurement test systems and parameter extraction methods are introduced, and applied to assess performance of recently developed 10-kV SiC MOSFETs and PiN diodes.*

Keywords: Silicon-carbide; power semiconductor; high-voltage; performance metrics; measurement systems.

Introduction

Recent breakthroughs in Silicon Carbide (SiC) material and fabrication technology have led to the development of High-Voltage, High-Frequency (HV-HF) power devices with 10-kV, 15-kHz power switching capability. The emergence of HV-HF devices with such capability is expected to revolutionize utility and military power distribution and conversion by extending the use of Pulse Width Modulation (PWM) technology to high voltage applications.

Currently, there are significant efforts underway to accelerate the development and application insertion of the new HV-HF SiC devices needed for commercial and military power conversion and distribution applications. The goal of the ongoing Defense Advanced Research Projects Agency (DARPA) Wide Bandgap Semiconductor Technology (WBST) High Power Electronics (HPE) program is to develop 15-kV, 110-A class power semiconductor devices enabling future electric ships, more electric aircraft, and all electric combat vehicles. DARPA is particularly interested in developing the power electronics device technology deemed necessary to enable 2.7 MVA Solid State Power Substations (SSPS) for future Navy warships. The benefits of HV-HF semiconductor technology have also been identified by the Electric Power Research Institute (EPRI) including advanced distribution automation using solid-state distribution transformers with significant new functional capabilities and power quality enhancements. In addition, HV-HF power devices are an enabling technology for alternative energy sources and storage systems.

The emergence of HV-HF power devices presents unique challenges in specifying the device requirements and establishing HV-HF PWM converter topologies. The purpose of this paper is to introduce device and package performance metrics required for HV-HF power conversion applications, and to describe the unique power device and package measurement test systems and parameter extraction methods required to assess the HV-HF SiC device performance. The device and package performance metrics presented in this paper along with the wafer level performance metrics developed at the Naval Research Laboratory will form the basis to assess progress toward the development of 15-kV, 110-A SiC half-bridge modules in Phase 2 of the DARPA HPE program.

The performance metrics presented in this paper include static, dynamic, and safe-operating-area (SOA) evaluation of SiC power diodes and switches as well as device and package reliability evaluation. The unique test equipment developed for this purpose includes: 1) a 25-kV variable pulse width curve tracer, 2) a 10-kV resistive and inductive load switching tester, 3) a 5-kV dI/dt and dV/dt controlled diode reverse recovery tester, 4) SiC model parameter extraction tools, 5) a high-speed transient thermal current uniformity imaging system, 6) a high-speed transient thermal response system, 7) a rapid thermal cycling stress system, and 8) an automated multi-channel forward bias stress and monitoring system. The discussion of these performance metrics and test systems is highlighted below using measured results for devices recently developed in Phase 1 of the DARPA WBST HPE program.

High Voltage, Variable Pulse Width Curve Tracer

The static performance evaluations required for HV-HF devices include forward output conduction characteristics and high voltage blocking characteristics. For switching devices, gate leakage (or input characteristics for bipolar drive devices) and reverse conduction characteristics are also required. Each characteristic is measured versus temperature (25° C – 225° C) and current uniformity is evaluated from the shape of the current pulse to identify potential SOA vulnerabilities.

The evaluation of experimental and application capable HV-HF devices required the development of a 25-kV variable pulse width curve tracer. Figure 1 shows the user interface and Figure 2 shows the circuit schematic for the curve tracer. From the user interface the operator can set up the pulse width, rise time, and measurement interval, as well as, the gate step and drain sweep parameters. The user also selects the appropriate current sensing and current limiting resistors (shown in Figure 2) for the measurement being performed. Essential safety interlocks and warning devices are employed but not discussed here.

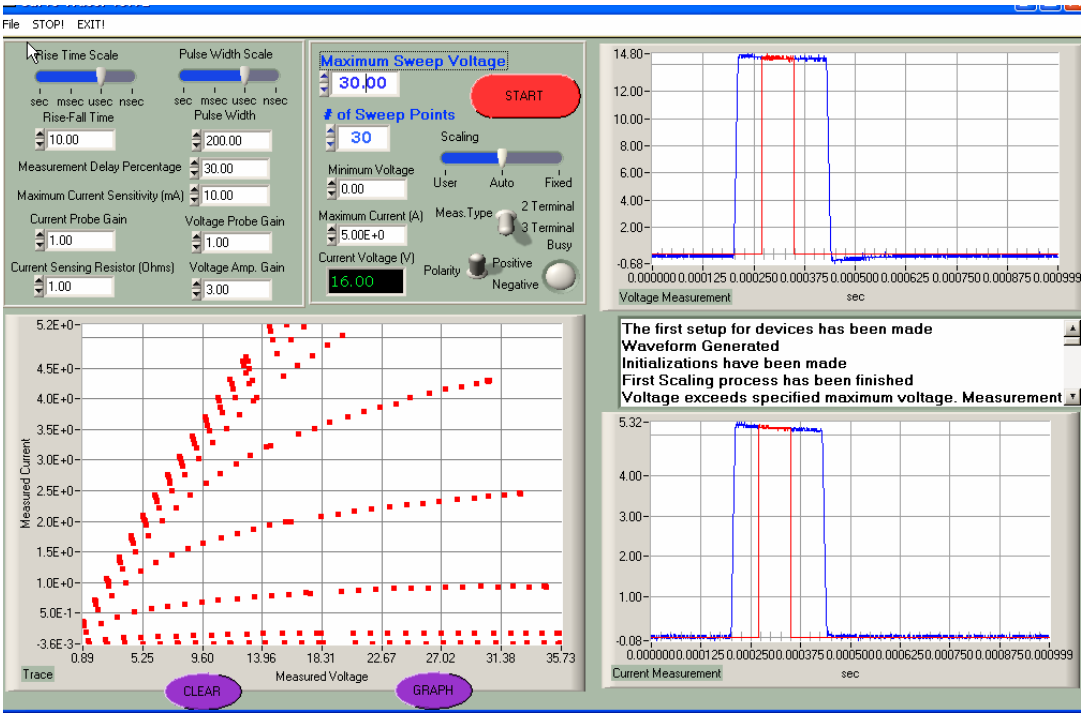

Figure 1. User interface for high voltage variable pulse width curve tracer measuring 10 kV SiC MOSFET.

When the measurement is initiated, the program performs the series of voltage pulses (defined by the maximum sweep voltage and number of points per sweep) using the arbitrary waveform generator. This is performed for each gate voltage (or base current) step applied by the source meter. The measured current-voltage pairs are obtained by averaging the data in the center portion (measurement interval) of each voltage pulse waveform (upper right graph of Figure 1) and the current response waveform (lower right graph of Figure 1).

The measured results in the lower left-hand graph in Figure 1 are the output characteristics of a 0.04 cm^2 10-kV SiC power MOSFET [1]. Each curve is for a gate voltage of 0 to 20 V in 2 V steps. The continuous current capability of this device is 2 A (50 A/cm^2) using the 250 W/cm^2 power dissipation capability of typical power packages. The pulse width for this measurement is 200 µs to reduce self heating. The forward conduction characteristics of the 0.5-cm^2, 10-kV PiN diodes [2] are measured similarly and have a continuous conduction capability of 40 A (80 A/cm^2)

Figure 3 shows the blocking characteristics of the MOSFET for different gate voltages indicating that the device is fully off for gate voltages less than 1 V and that the breakdown voltage defined at 1 mA/cm^2 is 9500 V. The pulse width for this measurement must be at least 10 ms due to the device capacitance charging time for low current measurements. However, these developmental devices are not yet capable of longer pulse widths at high voltage due to localized heating at defects. Sporadic behavior is often observed in the current pulses during leakage current tests.

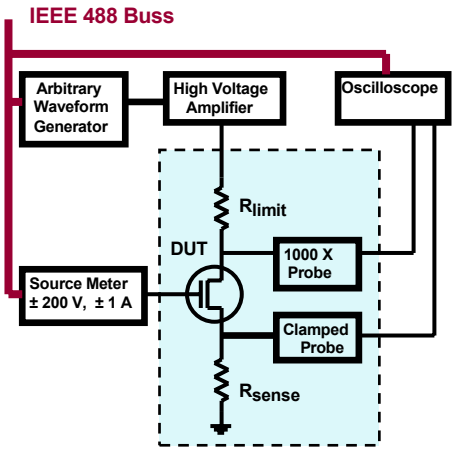

Figure 2. High voltage curve tracer circuit schematic.

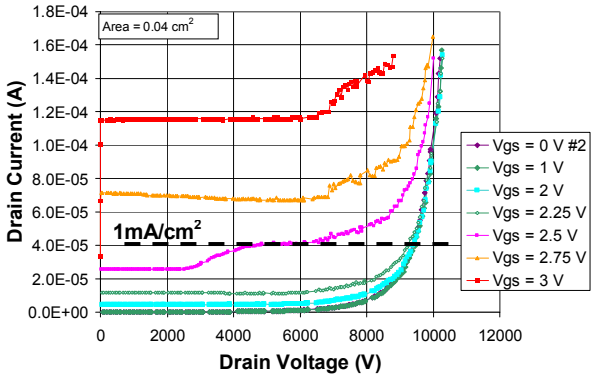

Figure 3. SiC MOSFET reverse leakage versus Vg.

High Voltage, High Speed Switching Testers

The dynamic performance evaluations required for HV-HF devices include transient waveforms for different load circuit types and different drive impedances in the case of switching devices. Several unique dynamic test systems have been developed for both HV-HF diodes and switching devices. These test systems also permit the evaluation of switching failure modes such as reverse bias SOA, unclamped-inductive-switching (UIS) energy capability, and short circuit withstand time.

For power diodes, the primary consideration is the measurement of the reverse recovery transient waveforms. This requires development of a driver circuit that establishes the initial forward current and then ramps the current with a constant controllable dI/dt and controllable dV/dt. The dV/dt is controlled by connecting a capacitor at the output of the driver circuit. The different dI/dt and dV/dt conditions emulate the range of conditions produced in different switching applications. The decay rate of the current tail for the low dV/dt condition can also used to determine the diode excess carrier lifetime.

Figure 4 shows the current and voltage waveforms of a 10-kV 40-A (0.5 cm^2) SiC PiN diode for three different dI/dt and two different dV/dt conditions. The test system used to make these measurements employs four paralleled vacuum tubes operated as a linear amplifier to produce the controllable linear current ramp. The tubes are critical for achieving the fast speed, high-voltage, and low parasitic capacitance. The current tail for the low dV/dt condition can be used to determine the diode base lifetime.

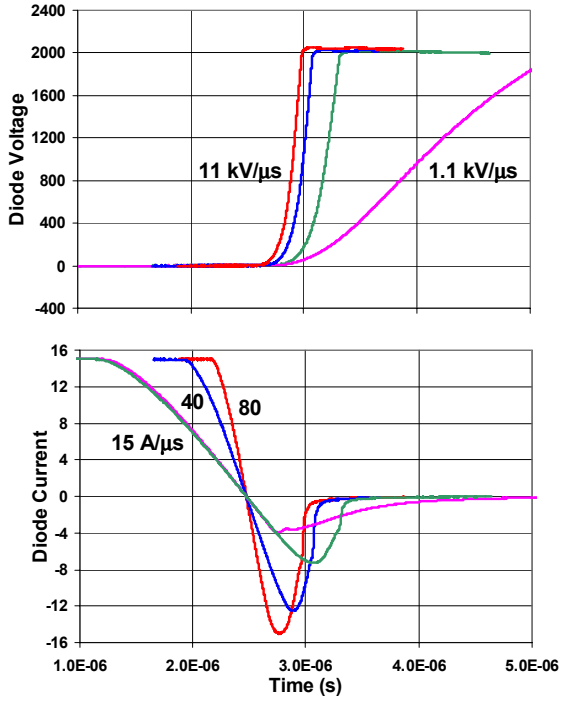

Figure 4. SiC PiN diode reverse recovery waveforms for different dI/dt and dV/dt conditions.

For switching devices, the primary considerations are resistive and inductive load switching. Figure 5 shows the 10-kV 2-A (0.04 cm^2) SiC MOSFET resistive load turn-off waveforms for different external gate resistors. The device internal gate resistance is 20 **Ω**. For small gate resistances, the switching time is approximately 100 ns and the switching energy is approximately 0.3 mJ or 150 W/cm^2 at 10 kHz. Figure 6 shows the 5-A, 6000-V clamped inductive load turn-off waveforms. This is near the RBSOA requirement of twice the continuous current and 80% of blocking voltage typically specified for Silicon IGBTs.

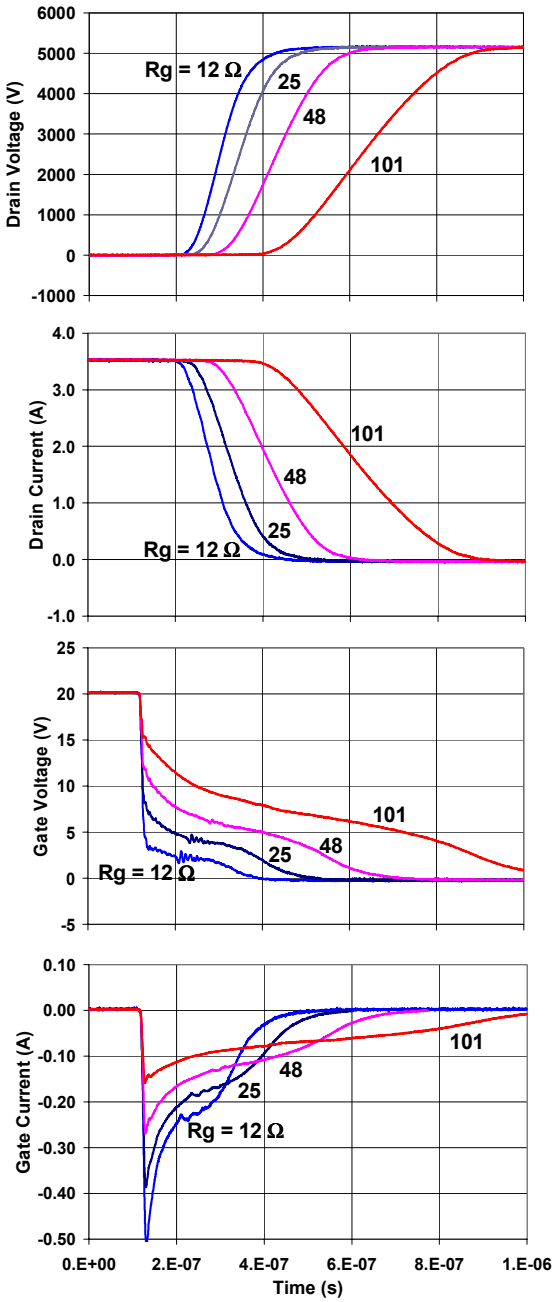

Figure 5. SiC MOSFET resistive load turn-off waveforms for different gate resistors.

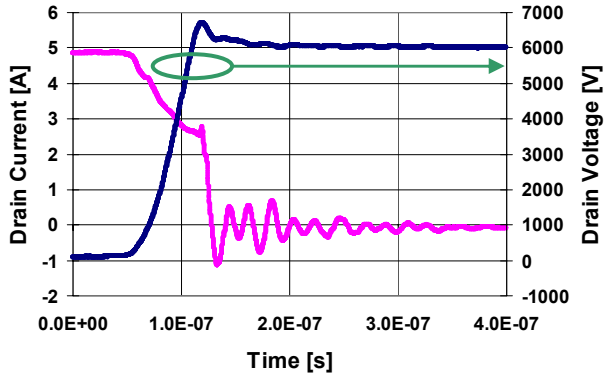

Figure 6. SiC MOSFET clamped inductive load switching waveforms for 2-Ω external gate resistor.

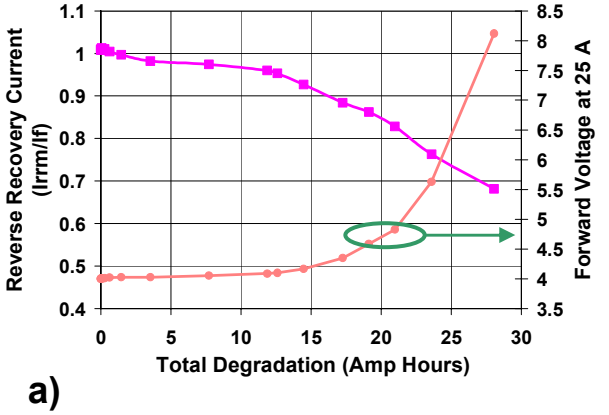

Figure 7. SiC PiN diode a) Vf and Irrm degradation and b) current uniformity images before and after.

Table 1: Linear region parameters extracted from LINMSR program.

	BV_{DS}, I_M	A (cm^2)	R_{SP} Bulk	R_{SP} Channel	K_{Plin} 25° C	K_{Plin} TC
Si MOSFETS						
IRF1010	55V, 85A	0.25	1.46	0.571	31.1	-1.57
IRF710	400V, 2A	0.04	97.9	8.028	1.01	-2.27
IRFBG20	1kV, 1.4A	0.10	769	13.52	1.39	-3.02
SiC MOSFETS						
Low Voltage	2kV, 3A	0.028	4.30	16.19	0.12	0.94
HPE-Type A	10kV, 1.5A	0.05	121	26.84	0.08	1.66
HPE-Type C	10kV, 1.5A	0.05	105	12.61	0.23	1.68

Device and Package Reliability Testing

The reliability evaluations required for HV-HF devices include static and dynamic SOA and long term stress and degradation monitoring. The power module package evaluations include thermal cycling stress and monitoring of dynamic thermal resistance, current uniformity, and voltage isolation. In addition to the curve tracer and switching testers discussed above, various unique test systems are being used to evaluate the HV-HF device and package reliability including: 1) a current uniformity imaging system, 2) a high-speed transient thermal response system, 3) a rapid thermal cycling stress system, and 4) automated long term stress and monitoring systems.

Forward bias stress induced degradation is a reliability issue that is particularly important for bipolar type SiC power devices such as PiN diodes [3]. An automated multi-channel forward bias stress and degradation monitoring system is used to subject the devices to forward current stress times ranging from a fraction of a second to over 1000 hours, and monitor degradation of device properties including on-state voltage, excess carrier lifetimes, and reverse recovery current.

Figure 7 shows example forward bias degradation results for a 10-kV 0.5-cm^2 SiC PiN diode where a) shows the forward on-state voltage Vf and reverse recovery current (Irrm/If) degradation and b) shows the current uniformity images before and after 28 amp-hours of degradation. While the electrical parameters change significantly, the current uniformity goes from being relatively uniform before stress (left image in Figure 7b) to only conducting in a few small regions after degradation (right image).

SiC Model Parameter Extraction Tools

To quantify and compare the performance of different devices, the automated IGBT Model Parameter Extractions Tools (IMPACT) are used to measure the device model parameters versus temperature. For power MOSFETs: 1) SATMSR first extracts the high and low current threshold voltage and saturation region transconductance parameters; 2) LINMSR then extracts the linear region trans-conductance parameter and calculates the epitaxial-layer and MOSFET channel components of specific on-resistance; and 3) CAPMSR finally extracts the gate-source capacitance, gate-drain overlap oxide capacitance, gate-drain overlap area, and the gate-drain overlap threshold voltage. Table 1 gives results extracted from the LINMSR program for different voltage silicon and SiC devices.

References

1. S.H. Ryu, et. al. "10 kV, 123 mΩ-cm^2 4H-SiC Power DMOSFETs," *IEEE EDL*, August 2004, pp. 556-558.
2. M.K.Das, et. al "Drift-Free, 50 A, 10 kV 4H-SiC PiN Diodes with Improved Device Yields," *ECSCRM* 2004.
3. A.R. Hefner et. al. "Characterization of SiC PiN Diode Forward Bias Degradation," *IAS* 2004, pp.1252 - 1260.