THE CONTRIBUTION OF HfO_2 BULK OXIDE TRAPS TO DYNAMIC NBTI IN PMOSFETS

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ABSTRACT

The Negative Bias Temperature Instability (NBTI) under pulsed bias stress conditions of devices with HfO_2 and SiO_2 gate dielectrics are studied and compared. The pulsed stress frequency responses of threshold voltage shift (ΔV_{th}) are quite different for both dielectrics as well as the acceleration parameters. Bulk traps in the HfO_2 film is used to explain these differences. Furthermore, it is shown that cautions must be taken when extrapolating the device lifetime of HfO_2 gate dielectrics. [*Keywords:* Hafnium oxide, negative bias temperature instability, high-k gate dielectrics, and bulk oxide traps.]

INTRODUCTION

As the scaling trend of CMOS goes on, new gate materials other than silicon dioxide are inevitably needed [1]. HfO_2 has been studied extensively and believed to a promising candidate [2, 3]. Before integrated into circuit, the reliability of the devices made with HfO_2 need to be characterized. One of the important problems with the CMOS devices is the NBTI phenomenon, which influences the threshold voltage (V_{th}) and driving current (I_{on}) of pMOSFETs [4]. Compared with SiO_2, with which high quality gate oxide can be achieved routinely, there exist more defects and traps inside HfO_2. It has been reported these bulk traps influence the V_{th} stability, thus the device performance [5, 6]. Several papers have been published on the NBTI of HfO_2 devices [7]. In those papers, the interface traps were evaluated using the charge pumping measurement, or the dc current-voltage method. However, the contribution of bulk traps to NBTI degradation needs further study. In this work, we evaluated the NBTI degradation of HfO_2 devices at different pulse bias stress conditions and compared them with SiO_2 control samples. The contribution of bulk traps are found to be important in NBTI study of HfO_2 devices and will influence the device lifetime extrapolation.

EXPERIMENT DETAILS

The devices used in this work are HfO_2/Hf silicate hybrid stacks pMOSFETs. The gate dielectrics were fabricated by metal organic chemical vapor deposition (MOCVD), post deposition annealing (PDA) with NH_3 at 700 °C for 60 s. The equivalent oxide thickness (EOT) is 1.7 nm. Between the HfO_2 bulk oxide and silicon substrate, there is an interfacial layer of SiO_2 with a thickness of 1.0 nm. For comparative study, a SiO_2 control wafer with a EOT of 2.0 nm is used. The channel width is 10 μm and the channel length 0.25 μm. Constant voltage stresses (CVS) are applied to the gate with dc and unipolar pulse stresses while the source, drain, and substrate are grounded. For the pulsed stress, the amplitude is identical to the dc stress voltage during the pulse "on" phase and was zero during the pulse "off" phase, and the duty cycle is maintained at 50 %. Unless specifically pointed out, the devices tested in this study are stressed with a –2.0 V dc or unipolar stress voltage. The experiment setup and stress waveforms are shown in Fig. 1. All the devices are stressed with equivalent time. The stress is periodically interrupted and the monitoring tests are performed immediately.

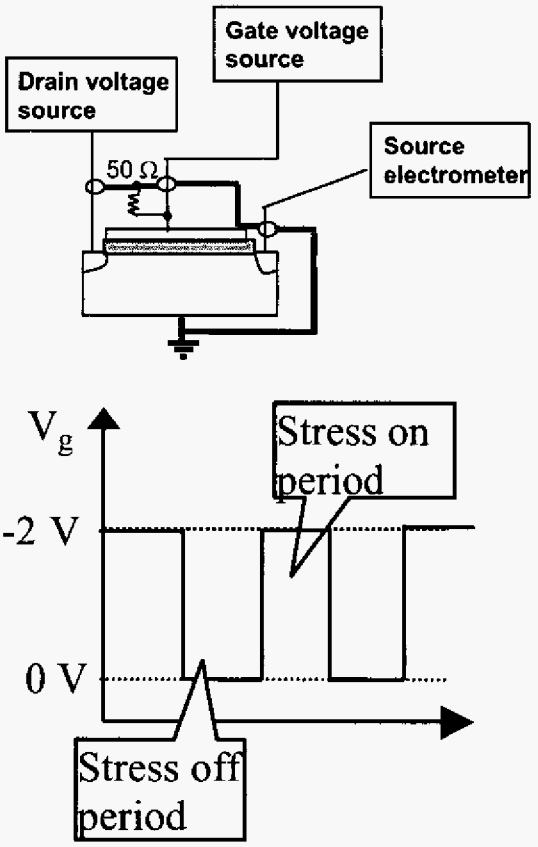

FIGURE 1. THE EXPERIMENT SETUP AND STRESS WAVEFORMS. DC AND PULSED BIAS STRESSES ARE USED.

RESULTS AND DISCUSSION

The Frequency Dependence

The NBTI degradation is first investigated by measuring the ΔV_{th} as a function of stress time, gate voltage and ambient temperature. V_{th} is determined using the constant current method [8]. It was found that when stress by dc gate voltages, ΔV_{th} of HfO_2 shows the similar trend as SiO_2 devices, except with different parameters, this is also observed by other reports [7]. A typical ΔV_{th} time evolution is shown in Fig. 2.

The frequency dependence of NBTI degradation of SiO_2 devices has been widely reported and several models have also been proposed to explain this behavior [9, 10]. For the HfO_2 devices in this study, we observed similar behavior, as shown in Fig. 3.

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In this figure, we compared the ΔV_{th} of HfO_2 and SiO_2 devices. For better understanding, Fig. 4 shows the normalized ΔV_{th} data with the dc stress condition set to be 1. Compared with SiO_2 control devices, HfO_2 devices show several noticeable features.

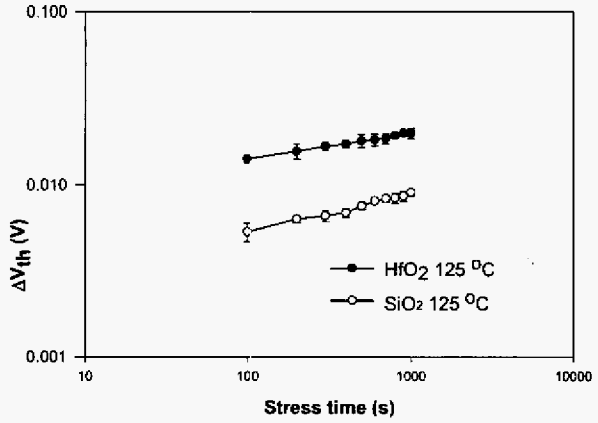

FIGURE 2. THE TIME EVOLUTION OF ΔV_{TH} OF HfO_2 DEVICES AND THE CONTROL SiO_2 SAMPLES.

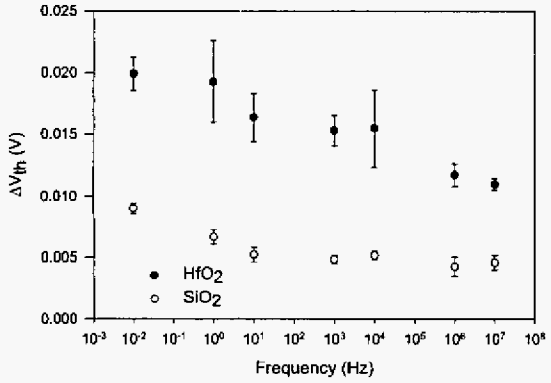

FIGURE 3. COMPARISON OF THE FREQUENCY DEPENDENCE OF ΔV_{TH} OF HfO_2 DEVICES AND THE CONTROL SiO_2 SAMPLE. TOTAL STRESS TIME IS 1000 S, STRESS TEMPERATURE IS 125 °C. FOR BETTER VIEW, THE FREQUENCY IS SET TO BE 0.01 HZ FOR THE DC STREES CONDITION.

First, the ΔVth of HfO_2 is much larger than SiO_2 devices as shown in Fig. 3. The oxide thickness difference itself cannot cause such a larger difference. This is must because of the intrinsic characteristics difference of the gate oxide, as we know there are larger interface trap density and bulk defects in HfO_2 gate oxide.

Second, the ΔV_{th} of both devices are significantly reduced at higher stress frequencies. With a 10 MHz gate voltage stress, the ΔV_{th} is only around 50 % of that caused by dc stress for both devices. This suggests there are time constants associated with the generation and relaxation of positive oxide charges and/or interface traps. It is believed that the injected holes generate the oxide traps [11]. With a higher frequency, i.e. a shorter stress on time, fewer oxide traps are generated. Possibly, the models proposed to explain this behavior of SiO_2 can also be adopted for HfO_2 devices.

At last, more importantly, the frequency dependence of HfO_2 and SiO_2 devices at middle frequencies are different. For example, ΔV_{th} of a 1 KHz stress voltage is about 80 % of that caused by dc stress with HfO_2 devices. However, for the SiO_2 devices, this ratio is about 60 %. In a separate study, we have demonstrated that for the SiO_2 devices, this dependence is found to be independent of gate oxide thickness [10]. Therefore, we believe the bulk traps inside the gate oxide could be one of reasonable explanations.

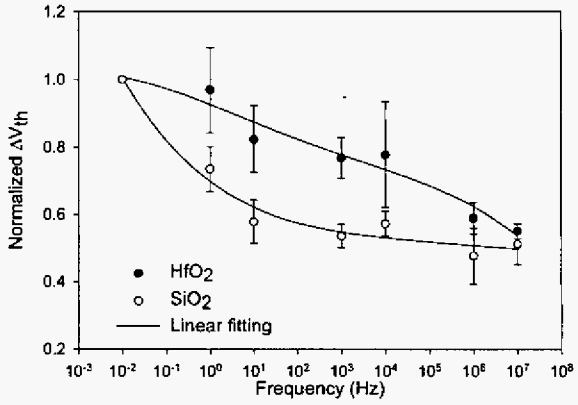

FIGURE 4. COMPARISON OF THE FREQUENCY DEPENDENCE OF NORMALIZED ΔVTH OF HfO_2 DEVICES AND THE CONTROL SiO_2 SAMPLE. THE DATA ARE TAKEN FROM FIGURE 3. THE LINE FITTING IS ONLY FOR BETTER VIEW. FOR BETTER VIEW, THE FREQUENCY IS SET TO BE 0.01 HZ FOR THE DC STREES CONDITION

The Contribution of Bulk Traps

Besides the positive oxide charges, the generation of oxide traps can cause reduced drain driving current, increased threshold voltage. It is believed that there is a large quantity of bulk traps inside the high-k dielectrics [5, 6, 12]. The charge pumping measurement is widely used to detect the trap density at and near the interface between the oxide and substrate. Since there are two interfacial layers in the high-k dielectric stacks, the conventional charge pumping measurement, in which the amplitude is fixed (FACP), cannot provide accurate information. In order to distinguish the bulk traps from the interface traps, a method called variable amplitude charge pumping (VACP) measurement was applied recently [5, 6]. A simplified setup is shown in Fig. 5. In our tests, we used both of these two methods to monitor the interface traps and bulk traps generation.

With the conventional charge pumping measurement, the interface traps generation is given by (1).

$$\Delta N_{it(t)} = \frac{\Delta I_{cp1}}{qAf} = \frac{\left(I_{cp1(t)} - I_{cp1(0)}\right)}{qAf} \quad (1)$$

Here $I_{cp1(t)}$ is the peak charge pumping current measured from substrate after stress time t, q is the electronic charge, A is the device area, and f is frequency. The charge pumping current measured from

the amplitude variable charge pumping method is believed to be originated from the total oxide trap density including the bulk traps and the interface states. With a similar definition, this trap density increase is given by (2).

$$\Delta N_{trap(t)} = \frac{\Delta I_{cp2}}{qAf} = \frac{\left(I_{cp2(t)} - I_{cp2(0)}\right)}{qAf} \quad (2)$$

$I_{cp2(t)}$ is the charge pumping current at a constant charge pumping amplitude after stress time t. Note this trap density is the sum of interface trap density and bulk trap density. Thus, the bulk trap density generation is given by the total trap density generation subtracting the interface state generation, as (3).

$$\Delta N_{bulk} = \frac{\Delta I_{bulk}}{qAf} = \frac{\Delta I_{cp2} - \Delta I_{cp1}}{qAf} \quad (3)$$

In this way, by measuring the charge pumping current change we can directly get the information of interface traps generation and bulk trap generation.

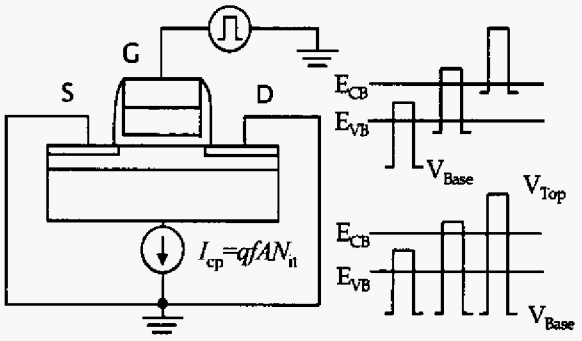

FIGURE 5. THE TWO CHARGE PUMPING MEASUREMENTS. IN FACP, THE VBASE IS SWEPT; IN VACP, THE VTOP IS SWEPT.

We performed both charge pumping measurements on the HfO_2 devices and the control SiO_2 samples. For the HfO_2 devices, we observed the distinct generation of bulk traps in addition to the interface traps with stress time. But there is almost no bulk traps generation from SiO_2 devices during the stress, which is similar to other reports [5, 6]. In addition to the dc stress, the same measurements were taken with different stress conditions. Fig. 6 shows the interface traps and bulk traps generations as a function of stress frequencies.

Evidently, the generation of bulk traps also depends on the pulsed stress repetition frequency. At dc stress conditions, the increased charge pumping current due to the bulk traps is comparable to that due to the interface traps. However, at higher frequencies, the bulk trap generation is about one order lower than the interface trap generation. This means that the contribution of bulk traps to the NBTI degradation at high stress frequencies is negligible even though it accounts a larger portion at the dc stress condition. This could be also the reason why the frequency dependence of ΔV_{th} is distorted compared with the SiO_2 control samples, since there is almost no bulk trap generation in the SiO_2 devices. The exact reason for the lower generation of bulk trap at higher stress frequencies is still unclear. We suspect that those bulk traps are caused by the injected holes. However, compared with interface traps, these traps are deep inside the oxide, thus it is more difficult for holes to reach those positions and create bulk traps when stressed with higher frequencies.

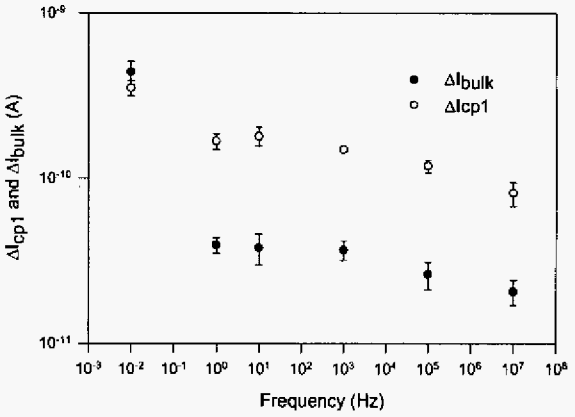

FIGURE 6. THE FREQUENCY DEPENDENCE OF GENERATIONS OF INTERFACE TRAPS AND BULK TRAPS. TOTAL STRESS TIME IS 1000 S, STRESS TEMPERATURE IS 125 °C. FOR BETTER VIEW, THE FREQUENCY IS SET TO BE 0.01 HZ FOR THE DC STREES CONDITION.

In addition to the different response to pulsed stress frequencies, we found the generation of bulk traps and interface traps also have different temperature dependences as shown in Fig. 7. For the interface traps generation, the activation energy is 0.11 eV, however, the bulk traps generation has a much higher activation energy, which is 0.24 eV. This suggests the interface traps generation of HfO_2 devices is less sensitive to the ambient temperature than bulk trap generation.

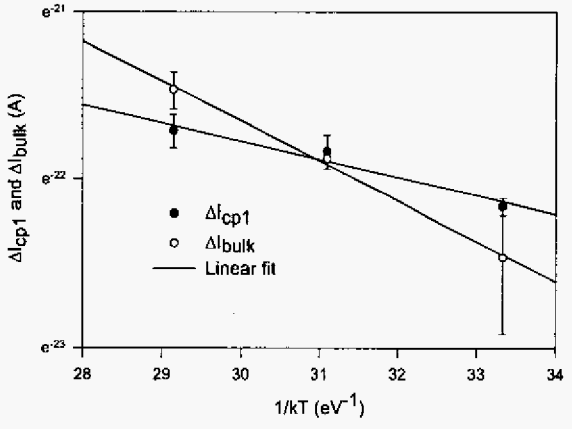

FIGURE 7. DIFFERENT TEMPERATURE ACCELERATION FACTORS OF CHARGE PUMPING CURRENTS DUE TO INTERFACE TRAPS AND BULK TRAPS.

To further study the influence of bulk traps NBTI degradation, we investigated the ΔV_{th} at different temperatures. In this test, we especially compared the dc and 10 MHz stress conditions. As we know, there are two factors that influence ΔV_{th}, the interface traps and trapped oxide charges. The oxide charge generation, which is mainly due to hole injection, is almost independent of temperature. Thus the activation energy extrapolated from the ΔV_{th} mainly reflects

the temperature dependence of interface traps. As shown in Fig. 8, the temperature dependences of SiO_2 devices at dc stress and 10 MHz stress are quite similar with activation energies of 0.14 eV and 0.13 eV respectively. However, the situation for HfO_2 devices is quite different. Even though the data don't fit well to a straight line, the activation energy extrapolated from dc stress is quite different from the 10 MHz stress. According to our experimental data, under dc stress conditions, the activation energy of ΔV_{th} is 0.11 eV, while it is only 0.05 eV for the 10 MHz stress. This clearly demonstrates the influence of bulk traps at different stress conditions, since we know from the previous test that the interface traps are less sensitive to stress temperature than bulk traps, and there are much less bulk traps generated with a 10 MHz gate voltage stress.

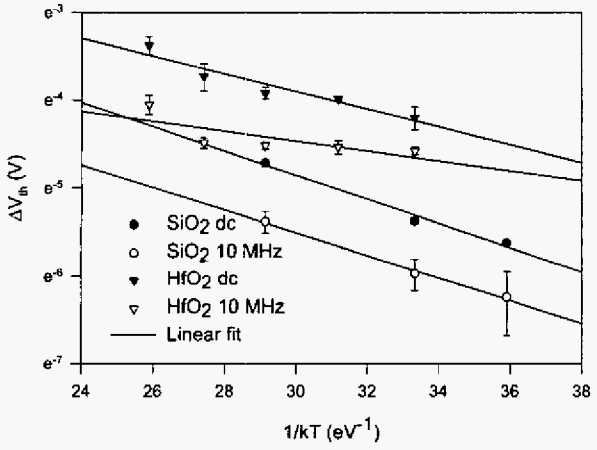

FIGURE 8. THE TEMPERATURE ACCELERATION OF GENERATIONS OF INTERFACE TRAPS AND BULK TRAPS. TOTAL STRESS TIME IS 1000 S, STRESS TEMPERATURE IS 125 °C.

In order to verify the influence of bulk traps, we add a 1.0 V, 10 s detrapping period before each I_d-V_g and charge pumping measurement. According to our tests, this detrapping period will not stress the device. Thus any further difference should not be caused by the stress during this period. We found that the charge pumping current due to the bulk traps almost disappeared after this detrapping period, as shown in Fig. 9, indicating that there was no more contribution from the bulk traps to the degradation of the device. In other words, the trapped charge observed during the NBTI stress are due to preexisting bulk traps and no additional bulk traps are generated during the NBTI stress.

Using this method, we did the similar temperature acceleration tests on the HfO_2 devices and the control SiO_2 samples. In addition to the annealing of the bulk traps, the injected holes could also be neutralized by this detrapping period. As shown in Fig. 10, after the detrapping period, the activation energies extrapolated under the dc stress and 10 MHz stress conditions are almost the same, which is similar to the control SiO_2 samples. Since the bulk traps and injected holes are already annualized during the detrapping period, these activation energies actually reflected the temperature sensitiveness of the interface traps. This could be the reason for the similar activation energies for two stress conditions of SiO_2 and HfO_2 respectively. In the HfO_2 devices, there is a 1.0 nm SiO_2 interfacial layer, thus we would expect similar interface traps. However, since the thickness of the interfacial layer is so small, the interface traps could have a structure of $Hf_3{\equiv}Hf\bullet$ in addition to the $Si_3{\equiv}Si\bullet$ structure. This can be the reason for the different activation energies between HfO_2 devices and the control SiO_2 samples.

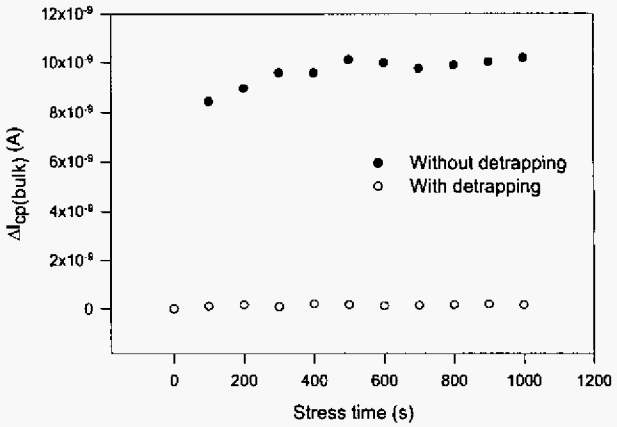

FIGURE 9. THE CHARGE PUMPING CURRENT DUE TO THE BULK TRAPS WITH AND WITHOUT DETRAPPING PERIOD.

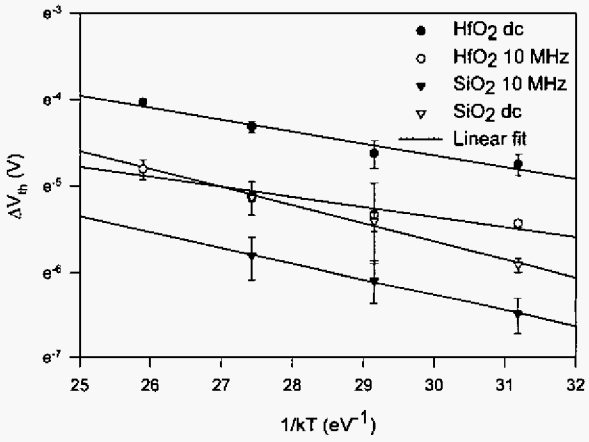

FIGURE 10. THE TEMPERATURE ACCELERATION OF ΔVTH OF HfO_2 DEVICES AND CONTROL SiO_2 DEVICES AT TWO STRESS CONDITIONS. THE STRESS CONDITION IS THE SAME WITH FIG. 7 EXCEPT THE ADDITION OF A DETRAPPING PERIOD BEFORE EACH MEASUREMENT.

CONCLUSION

The contribution of gate oxide bulk traps to NBTI degradation of HfO_2 devices is evaluated and compared with SiO_2 control samples. The ΔV_{th} and oxide trap generation of HfO_2 and SiO_2 devices show the dependence of gate voltage frequencies. Besides interface traps, bulk traps also influence the NBTI degradation of HfO_2, and this influence is also dependent on the stress conditions. At dc stress conditions, the bulk trap generation is comparable to that of interface traps, and thus plays an important role for the ΔVth, however it becomes negligible at higher frequency stresses. In addition to the different frequency response, the bulk trap generation also shows a different temperature dependence than the interface traps. We found that interface traps generation has much higher activation energy than bulk traps, which also explain the different temperature

dependences of ΔVth at dc and high frequency stress conditions. We should be cautious when extrapolating the device lifetime based on the experimental data especially using the temperature acceleration tests, as the extrapolation will be quite different under the dc and pulsed stresses.

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