NOVEL ELECTROSTATIC DISCHARGE PROTECTION STRUCTURE FOR A MONOLITHIC GAS SENSOR SYSTEMS-ON-A-CHIP**

J. A. Salcedo, J. J. Liou, M. Y. Afridi, A. R. Hefner**

Department of Electrical and Computer Engineering
University of Central Florida
Orlando, FL 32816, USA

*Semiconductor Electronics Division
National Institute of Standards and Technology
Gaithersburg, MD 20899, USA

ABSTRACT

A new on-chip Electrostatic Discharge (ESD) protection scheme is demonstrated for MicroElectroMechanical Systems (MEMS)-based Embedded Sensor (ES) System-on-a-Chip (SoC). The ESD protection scheme includes ground-referenced protection cells implemented with novel multifinger thyristor-type devices for 1) the Input/Output (I/O) protection, 2) the power supply clamp, and 3) the protection at the internal sensors' electrodes. The *I-V* characteristics of the thyristor-type protection cells are adjusted for providing an optimum ESD protection per unit area. Transmission Line Pulsing (TLP) measurements and ESD testing show superb high conductance on-state *I-V* characteristics with no latch-up problem when thyristor-type devices are subjected to an ESD event, while very low leakage current is obtained at the SoC operating voltage.

1. INTRODUCTION

The MEMS (MicroElectroMechanical Systems) microhotplate-based chemical gas sensor is an emerging CMOS (Complementary Metal Oxide Semiconductor)-based technology that has cost and performance advantages over the existing commercial gas sensing technologies [1]. The microhotplate gas sensor platform, heater power amplifier, signal conditioning, and control circuitry have been formulated as a Virtual Component (VC) conforming to the SoC block-based design methodology [2]. The SoC design methodology is necessary due to the complexity of large digital systems and facilitates functional block design reuse. Formulating the gas sensor as a VC enables incorporation into CAD (Computer Aided Design) libraries and facilitates the development of single chip gas sensing and classification solutions. The implementation of ES-VCs requires the use of a standard digital interface and standard DFT (Design for Test) functionality.

A major concern in fabrication, packaging and assembly and, even during normal handling and testing of CMOS ICs is the Electrostatic Discharge (ESD) induced damages. The ESD protection usually consists of protection devices for each Input/Output (I/O) pad and a power supply clamp. Because of the chip area constraints, sensor micromachining process, and presence of the ES, the design of ESD protection for the gas sensor SoC is more stringent than that for typical VLSI circuits.

The gas sensor SoC requires ESD protection at the peripheral I/O pads and at the internal electrodes of the ES. Fig. 1 illustrates such an ESD protection scheme. Bidirectional ground-referenced ESD protection elements are shown connected to the I/O pads and sensor electrodes. Fig. 2 depicts a Scanning Electron Microscope (SEM) micrograph of a microhotplate-based gas-sensor showing in more detail the internal sensor electrodes with ESD protection included.

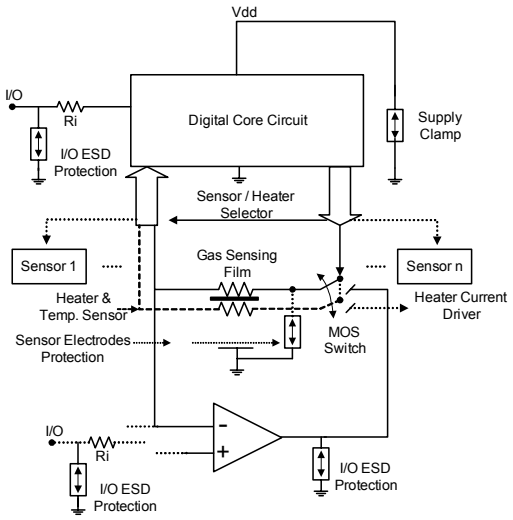

Fig. 1. ESD protection scheme for the gas sensor SoC.

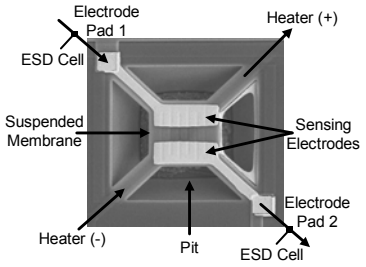

Fig. 2. An SEM micrograph of microhotplate showing sensor electrodes and ESD protection points.

In this paper, a novel ESD protection scheme is integrated in the gas sensor SoC. The microhotplate gas sensors are produced using a standard 1.5 μm CMOS foundry process as

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opposed to the custom MEMS fabrication conventionally used. The same approach can also be extended to submicron CMOS processes. Such a foundry process enables the monolithic integration of the custom ESD protection structure and the core circuit with functional blocks on the same chip. The protection scheme is built based on the ground-referenced thyristor-type devices which are particularly robust and useful for ESD solutions [3-4]. The design and bidirectional operation of the thyristor-type ESD protection device is first discussed. The *I-V* characteristics of the devices are scaled-up by designing novel multifinger thyristor-type structures. The performance of the protection system is finally demonstrated by using TLP measurements and ESD HBM (Human Body Model) testing.

2. ESD PROTECTION DEVICE

2.1 Thyristor-type ESD device structure

The thyristor- or Silicon Controlled Rectifier (SCR)-type device is applicable for ESD protection because it snaps back to a low holding voltage and high conductance during the ESD event (i.e., on-state). The current density in this device is uniformly distributed, which permits a better dispersion of the heat dissipation and to some extent avoids hot-spot generation during the ESD event. The Low-Voltage-Triggered-Silicon-Controlled-Rectifier (LVTSCR), an offspring of the SCR, further offers the advantage of reducing the trigger voltage to a level acceptable for use in CMOS IC protection [3]. However, the low holding voltage and the low holding current [5] of the LVTSCR often cause a latch-up problem in ICs with operating voltage above 1.5 V.

A modified version of the LVTSCR, shown in Fig. 3, with tunable holding and trigger voltages has been designed and fabricated using the CMOS process. This device can be triggered at a relatively low voltage and can have a holding voltage higher than the power supply (to avoid ESD latch-up) by properly adjusting the internal lateral dimensions L, D, and D2.

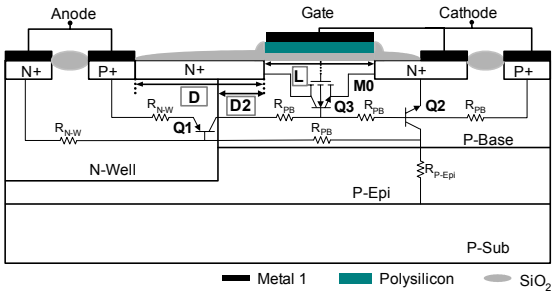

Fig. 3. Cross-sectional view of thyristor-type ESD protection device.

2.2 Thyristor-type ESD device operation

The thyristor-type ESD protection device shown in Fig. 3 can provide effective ESD protection in both forward and reverse operating conditions. The forward on-state characteristics result when the anode voltage increases abruptly and turns on the NPN bipolar underneath the gate (Q3). High injection of electrons and holes takes place in the cathode and anode regions, respectively, and the laterally distributed N-Well/P-Base blocking junction becomes conductive. This gives rise to a potential snapback between the anode and cathode from the trigger voltage (V_T) to the holding voltage (V_H) and a low impedance path when the voltage is increased beyond V_H.

The snapback behavior is attributed to a distributed vertical- and lateral-bipolar effect. In the region formed underneath the gate, the mechanism of operation involves avalanche breakdown and high impact ionization. The minimum potential difference in the N-Well to P-Base regions is related to the reverse junction barrier, consistent with the gradual junction approximation, and the holding voltage is the addition of this voltage and the voltage underneath the gate of the embedded MOS (M0), see Fig. 3. The tuning of the holding and trigger voltages is readily accomplished by adjusting the dimensions D, L, and D2 [4]. Fig 4 shows *I-V* characteristics of two stand-alone test devices with different dimension D. The adjustment in the holding and trigger voltages and the slight difference in the conduction resistance after snapback are illustrated. It is important to note that the leakage current at anode to cathode voltage approaching Vdd does not change with dimension D.

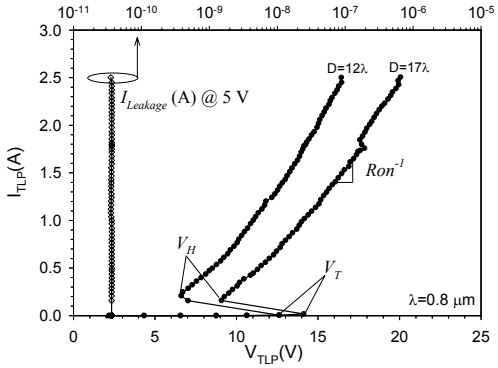

Fig. 4. Transmission Line Pulsing (TLP) *I-V* characteristics of two stand-alone 80 μm width thyristor-type devices as shown in Fig. 3.

For the reverse operating condition, the voltage at the anode is lower than that at the cathode, and it forward biases the vertical P-Sub/N-Well junction and the lateral P-Base/N-Well junction. The maximum voltage is thus clamped by lateral and vertical forward-biased junctions (see Fig. 3), and a low impedance path is created for ESD current.

The above-mentioned thyristor-type device is suitable for the design of the different ESD components in the ES-SoC (see Fig. 1), but proper tuning of the V_T, V_H, and *Ron* are required for each component. The trigger voltage is designed to be smaller than the transient voltage that causes circuit malfunction. Since Vdd and Vss are directly connected to the core circuit, the trigger voltage is more critical for the supply clamp than for the I/O protection. V_T cannot be arbitrarily small, however, since the protection device should not be activated without the presence of an ESD event.

The holding voltage is adjusted according a different criterion. It has to be higher than the normal operation voltage in the protected pad e.g., higher than Vdd. However, holding voltages below Vdd are allowed if the I/O pad current is sufficiently low and cannot withstand a latchup condition in the thyristor device. The current driven in the I/O pads of the gas

sensor SoC is low enough, which allows a more optimum design of I/O ESD protection with holding voltage below Vdd.

The required on-state resistance *Ron* is determined from the maximum voltage allowed at the pad and the maximum current level of ESD. This *Ron* value is then used to determine the required cell width of the device. The proposed thyristor-type device has a much lower *Ron*/width ratio than conventional ESD protection devices, thus minimizing the chip area needed for ESD protection.

3. COMPLETE ESD PROTECTION DESIGN

3.1 I/O pad protection and supply clamp

An ESD protection level of 3 kV HBM is required at the pads of the SoC periphery. Fig. 5 depicts a schematic of the pad level protection, which includes a bidirectional supply clamp and I/O pad protection constructed based on modified ground-referenced thyristor-type devices.

For the supply clamp, the holding voltage (V_H) should be higher than Vdd to avoid transient latch-up. For the I/O ESD protection, on the other hand, the protection structures can be designed with a smaller holding voltage because the driving current available in the logic pads during normal operation is relatively low and cannot sustain a latch-up condition. Smaller holding voltage results in smaller resistance in the forward and reverse conduction.

The requirement for the trigger voltage (V_T) is more stringent for the supply clamp than that for the I/O pad protection. The supply clamp is connected to the bias of the core circuit and is required to keep the power supply within a range of voltage safe for the circuit. Based on earlier experiments accomplished in the CMOS process, a V_T below 13 V provides a safe supply clamp protection, but this value can be relaxed to higher voltage levels for the I/O pads.

While a thyristor-type device that meets the requirements for the supply clamp can meet as well the requirements for the I/O protection, using slightly different thyristor-type devices for the pad protection is more optimal. Measurements have shown that removing the P-Base in the thyristor-type device (Fig. 3) leads to an increased V_T not allowed for the supply clamp but acceptable for the I/O protection. Doing so also results in desirable smaller forward and reverse conduction resistances [3], which allow for a higher ESD current per unit area in the protection device and a higher level of I/O ESD protection.

3.2 Sensor electrodes ESD protection

Fig. 6 shows the ESD protection devices at the ES electrodes and a cross-sectional view of the gas sensor, illustrating the effective capacitance (C) between the exposed metal oxide sensing film and the substrate. For this particular ESD protection device, an additional contact from the anode region to the drain of the embedded MOS device is added to further reduce V_T. This thyristor has a smaller area than that for the I/O pads and supply clamp, because the internal sensing nodes are subject to a lower level of ESD stress. The main objective of the protection is to avoid possible ESD mechanisms originated at the sensor and provide the necessary low impedance path for current/voltage overshoots at sensing electrodes. Moreover, ESD stress associated with the post-processing fabrication of gas sensors can also be protected [4].

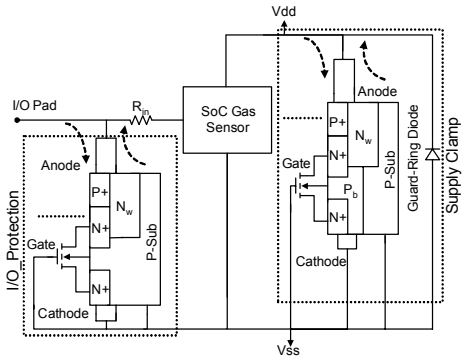

Fig. 5. Schematic of the supply clamp protection implemented with bidirectional multifinger thyristor-type devices.

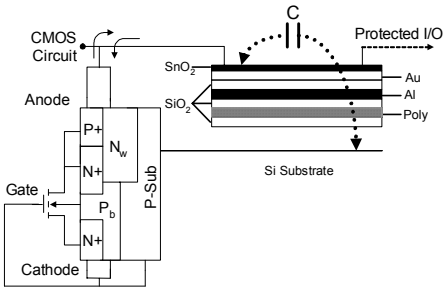

Fig. 6. Cross-Sectional view of microhotplate-based gas sensor with protection in the sensor electrode.

3.3 Layout of Multifinger Thyristor Cell

Integration of the ESD protection structure in the SoC requires fitting the protection elements with minimum extra area consumption and no major changes in the SoC core circuit layout. Fig. 7 shows a partial top-view of the layout for the novel thyristor-type protection device. Note that a multifinger structure is considered, as it has the advantages of scalability, is more immune to process variability, and has simpler on-chip integration. The anodes are connected through metal 1 (M1) to the protected pad, and the cathodes are connected to metal 2 (M2) and grounded. The width of M1 is increased from the top to the bottom so that a more uniform ESD current distribution in the multifinger device can be obtained.

To achieve different levels of ESD protections, different numbers of fingers must be used. Table I summarizes the HBM level obtained for 2x6 fingers and 2x8 fingers protection cells. This table shows that with a 2x6 fingers thyristor cell, HBM ESD protection of higher than 3 kV is obtained. Still higher ESD protection is obtained for the case of 2x8 fingers. These devices are robust and occupy a smaller chip area than the traditional dual-diode protection. The HBM level versus the number of fingers is very important in the sensor SoC design, as a trade-off between the ESD robustness and chip area can be optimized.

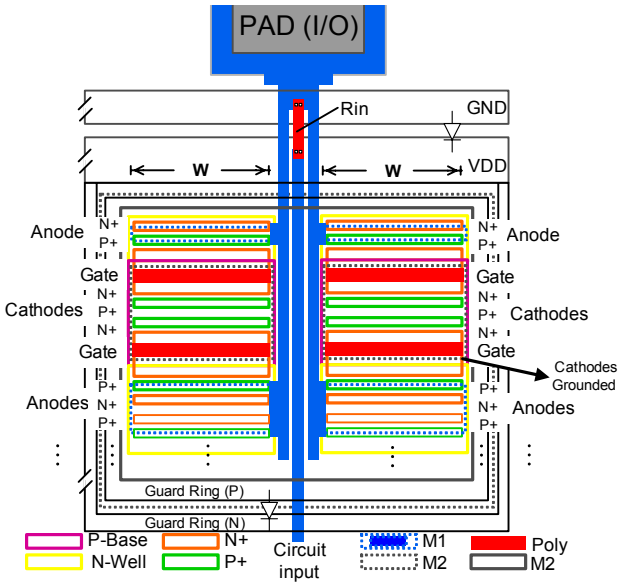

Fig. 7. Partial layout top-view of a 2x3 multifinger thyristor-type device for I/O ESD protection.

TABLE I

HBM ESD protection levels of multifinger thyristor-type devices (3 kV is required). VSS=Ground.

Dev. Fing.	I/O (+)	I/O (-)	Vdd (+)	Vdd (-)	I/O-I/O
2x6 Fing.	4.3 kV	3.3 kV	4.0 kV	3.4 kV	3.2 kV
2x8 Fing.	5.5 kV	4.2 kV	5.5 kV	4.1 kV	4.1 kV

4. ESD EXPERIMENTAL RESULTS

TLP data of the low and high current regimes of a 2x8 multifinger cell used for the supply clamp is depicted in Fig. 8. For better illustrations, the *I-V* characteristics are plotted in both the linear and logarithmic scales. Note that the low voltage current is very low, and thus the cell does not interfere with normal circuit performance biased at Vss= 0 V and Vdd= 5 V. During an ESD event, the protection cell triggers at a voltage of about 12.5 V and is able to protect the core circuit for TLP current levels over 5 Amp.

Table II summarizes measured V_T, V_H, and *Ron* of the supply clamp and I/O protection structures constructed using the multifinger thyristor-type devices. Consistent with the explanations presented in Section 3, the I/O protection has a higher V_T than the supply clamp, but V_H and *Ron* are lower in the I/O protection. For the sensor electrode protection, 2x2 thyristor cells are used, with over 2 kV ESD HBM capability and $V_T \cong 10.4$ V, $V_H \cong 7.3$ V, and $Ron \cong 3\ \Omega$.

The internal dimensions of the thyristor-type devices used for the custom design of the SoC ESD protection components are: 1) for the supply clamp, D=5.6 µm, D2=3.2 µm, and L=5.6 µm; 2) for the I/O protection, D=8 µm, D2=4 µm, and L=4.8 µm; and 3) for the ES electrode protection, D=6.4 µm, D2=2.4 µm, and L= 4 µm. The other dimensions of the thyristor-type devices follow the standard rules for the minimum feature sizes of the 1.5 µm CMOS process.

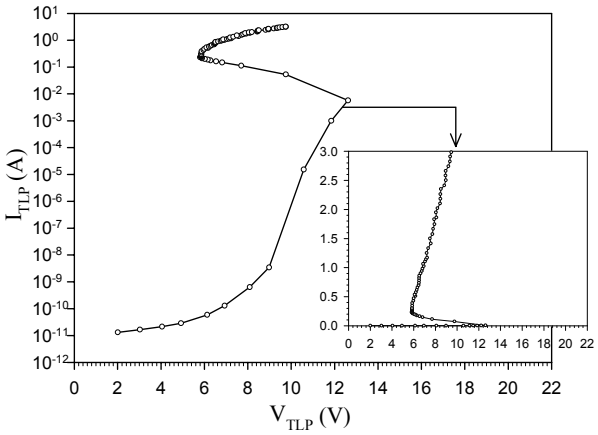

Fig. 8. TLP *I-V* characteristics in logarithmic and linear scales for a 2x8 multifinger thyristor-type device.

TABLE II

Measured V_H, V_T, and *Ron* of 2x8 multifinger thyristor-type devices used for the supply clamp and I/O protection.

Protection Dev.	$\approx V_T$ (V)	$\approx V_H$ (V)	$\approx Ron$ (Ω)
Supply Clamp	12.5	6.0	1.9
I/O protection	14.9	5.1	1.3

5. CONCLUSION

On-chip integration of an ESD protection scheme for a microhotplate-based gas sensor SoC is developed. The protection scheme includes multifinger thyristor-type devices for the custom implementation of the I/O protection, supply clamp, and sensor electrodes. The proposed ESD protection scheme occupies a smaller chip area than the standard dual-diode and ground gate protection, provides the required level of ESD immunity, and renders an optimal ESD solution for the MEMS SoC. Experimental results verify that the SoC passed the HBM ESD stress of more than 4.1 kV with no latch-up problem and low leakage current during the SoC normal operation.

6. REFERENCES

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