10-kV, 123-m$\Omega\cdot$cm^2 4H-SiC Power DMOSFETs

Sei-Hyung Ryu, *Senior Member, IEEE*, Sumi Krishnaswami, Michael O'Loughlin, James Richmond, Anant Agarwal, *Member, IEEE*, John Palmour, *Member, IEEE*, and Allen R. Hefner, *Fellow, IEEE*

***Abstract*—10 kV, 123 m$\Omega\cdot$cm^2 Power DMOSFETs in 4H-SiC are demonstrated. A 42% reduction in $R_{\mathrm{on,sp}}$, compared to a previously reported value, was achieved by using an 8×10^{14} cm^{-3} doped, 85-μm-thick drift epilayer. An effective channel mobility of 22 cm^2/Vs was measured from a test MOSFET. A specific on-resistance of 123 m$\Omega\cdot$cm^2 were measured with a gate bias of 18 V, which corresponds to an E_{ox} of 3 MV/cm. A leakage current of 197 μA was measured at a drain bias of 10 kV from a 4H-SiC DMOSFET with an active area of 4.24×10^{-3} cm^2. A switching time of 100 ns was measured in 4.6-kV, 1.3-A switching measurements. This shows that the 4H-SiC power DMOSFETS are ideal for high-voltage, high-speed switching applications.**

***Index Terms*—4H-SiC, power MOSFET, high voltage, high-speed switching.**

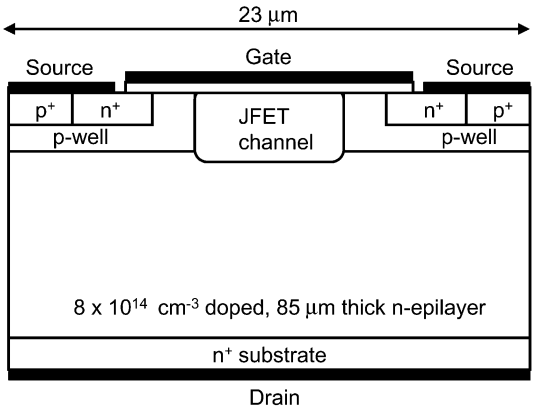

Fig. 1. Simplified cross section of the 4H-SiC power DMOSFET.

I. Introduction

POWER MOSFETs in 4H-SiC are very attractive for high-voltage switching applications because of their low specific on-resistances and fast, temperature independent switching characteristics [1]. Several groups have successfully demonstrated high-voltage, high-speed SiC power MOSFETs [2], [3] and the blocking capability of SiC MOSFETs has been continuously increasing ever since [4]. Recently, a 10-kV power DMOSFET in 4H-SiC was reported [5], [6], with a specific on-resistance of 236 m$\Omega\cdot$cm^2, which is approximately a factor of 85 lower than the theoretical value for a silicon majority carrier device. In this letter, we present our latest results in 10-kV 4H-SiC DMOSFET development—a specific on-resistance of 123 m$\Omega\cdot$cm^2 is demonstrated, which is a 42% reduction in specific on-resistance compared to the previous results. This is the lowest specific on-resistance value ever reported for 10-kV class majority carrier switches.

II. Experimental

A simplified cross section of the DMOSFET cell is shown in Fig. 1. An 85-μm-thick, 8×10^{14} cm^{-3} doped n-type drift epilayer was grown on the Si-face of an n$^+$, 4H-SiC substrate, cut with an 8° offset angle. A previously reported 10-kV device [6] used a 115-μm-thick, 6×10^{14} cm^{-3}-doped drift layer. The blocking voltage of the device in [6] was limited by the performance of the implanted junction termination extension edge termination, which suffered from shallow junction depths, and variations in implant activation rate and field oxide charges. The device reported in this paper used an edge termination structure with multiple floating guard rings, which is less sensitive to those problems. Fifty guard rings were used in this device, and the length of the termination structure is 400 μm.

Retrograde p-wells, with a surface concentration of 1×10^{17} cm^{-3} and a peak concentration of 5.5×10^{18} cm^{-3} at a depth of 0.4 μm, were formed by aluminum implantation at around 650 ° C, and the n$^+$ source regions were then formed by a heavy dose nitrogen implantation. The MOS gate length, determined by the distance between the p-well and the n$^+$ source implants, is 1.5 μm. The gate packing density for the mask design is 426 cm/cm^2. The JFET gap, defined by the distance between two adjacent p-wells, is 5 μm. The JFET regions were implanted with nitrogen ions to a doping concentration of 5×10^{15} cm^{-3} [7]. A heavy dose aluminum implantation formed the p$^+$ contacts to the p-wells as well as the floating guard rings. All the implants were activated at 1600 ° C in silicon overpressure. A 1.5-μm-thick PECVD oxide layer was then deposited and patterned as the field oxide. A 602-Å-thick gate oxide layer was thermally grown at 1200 °C in dry O_2, then annealed in N_2O at 1300°C [8]. A degenerately doped polysilicon layer was deposited and etched as gate electrode. A 8000-Å-thick LPCVD oxide layer was then deposited as an inter-metallic dielectric layer, and via holes were opened. 800-Å-thick Ni layers were deposited and sintered on the n$^+$ and p$^+$ regions as well as the backside to form ohmic contacts. Finally, 4-μm aluminum overlayer was deposited and etched on the front side, and 2-μm-thick Ti–Pt–Au layer was deposited on the backside to form the electrodes.

Fig. 2(a) shows the room-temperature linear region I_D versus V_{GS} characteristics measured from a test MOSFET ($W/L = 150$ μm/150 μm), built on a p-well adjacent to the power DMOSFETs. A peak effective channel mobility (μ_{eff})

Manuscript received April 15, 2004; revised May 2, 2004. This work is supported by DARPA under ONR Contract N00014-02-C-0302. The review of this letter was arranged by Editor K. T. Kornegay.

S.-H. Ryu, S. Krishnaswami, M. O'Loughlin, J. Richmond, A. Agarwal, and J. Palmour are with the Cree, Inc., Durham, NC 27703 USA.

A. R. Hefner is with the National Institute of Standards and Technology, Gaithersburg, MD 20899-8124 USA.

Digital Object Identifier 10.1109/LED.2004.832122

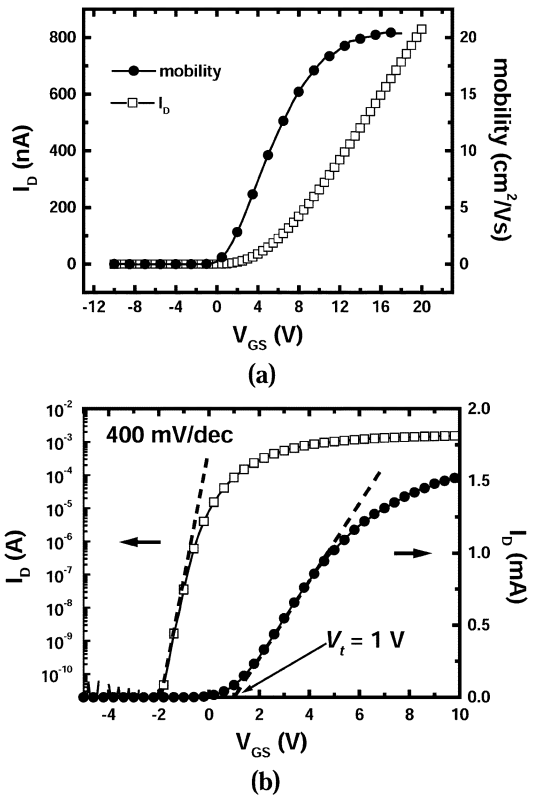

Fig. 2. (a) I_D versus $V_{\rm gs}$ measurement on a 150/150-μm test MOSFET and effective channel mobility. A peak effective mobility of 22 cm^2/Vs was measured. (b) I_D versus $V_{\rm gs}$ measurement on the 4H-SiC power DMOSFET. A $V_{\rm th}$ of 1 V was measured. A $V_{\rm DS}$ of 50 mV was used for both measurements.

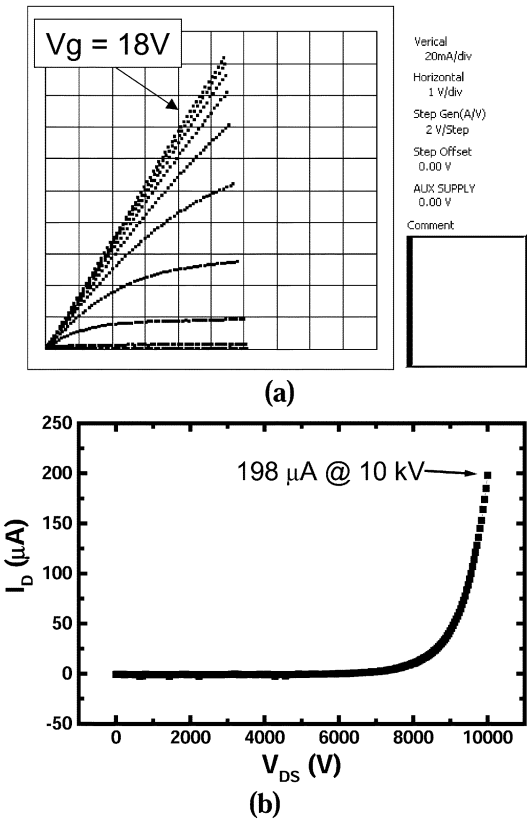

Fig. 3. Static *I–V* characteristics of a 4.24×10^{-3} cm^2 4H-SiC power DMOSFET measured at room temperature. (a) A specific on-resistance of 123 mΩ·cm^2 was measured with a gate bias of 18 V. (b) A leakage current of 198 μA was measured at a drain bias of 10 kV. A gate bias of -8 V was applied for this measurement.

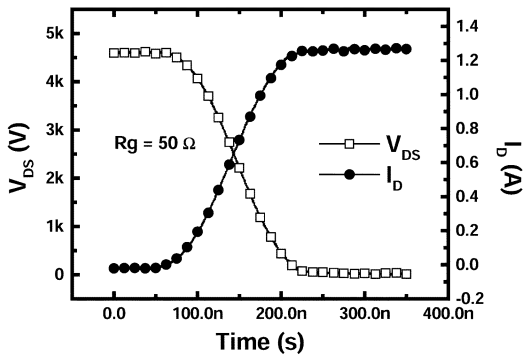

Fig. 4. Room-temperature switching characteristics of a 4.76×10^{-2} cm^2 4H-SiC power DMOSFET. A supply voltage of 4.6 kV, a load resistance of 3.6 k Ω, and a gate resistance of 50 Ω were used for this measurement. A switching time of 100 ns was measured.

of 22 cm^2/Vs was measured, and a threshold voltage ($V_{\rm th}$) of 4 V was extracted from the linear portion of the curve at room temperature. Fig. 2(b) shows the linear region I_D versus $V_{\rm GS}$ characteristics measured from the 4H-SiC DMOSFET. A $V_{\rm th}$ of 1 V was measured, which is significantly lower than the value measured from the test MOSFET. Even though the device had a positive $V_{\rm th}$, the device showed a significant drain current at $V_{\rm GS}$ = 0. This is due to the "soft threshold" effect caused by variations in the gate length [9]. The semilog plot of the I_D versus $V_{\rm GS}$ characteristics, shown in Fig. 2(b), indicates that the device requires a $V_{\rm GS}$ of -2 V for a complete turnoff. A subthreshold swing of 400 mV/dec was also measured, which is approximately a factor of five greater than the value expected from a silicon MOSFET. The large subthreshold swing can be explained by high MOS interface state density in 4H-SiC, which is at least an order of magnitude greater than that of a silicon MOS structure [8].

Fig. 3(a) shows the on-state characteristics of a 4H-SiC power DMOSFET with an active area of 4.24×10^{-3} cm^2 at room temperature. Although it was shown that the thermally grown gate oxide layer in a 4H-SiC MOSFET is reliable for oxide fields ($E_{\rm ox}$) up to 4 MV/cm [10], $E_{\rm ox}$ was limited to 3 MV/cm for this measurement. With a gate bias of 18 V ($E_{\rm ox}$ = 3.0 MV/cm), the device showed a specific on-resistance ($R_{\rm on,sp}$) of 123 mΩ·cm^2. Gate biases greater than 14 V had little effect on the on-resistance, which indicates that the on-resistance is dominated by the drift layer resistances. This is a reduction of 42% in $R_{\rm on,sp}$, compared to the previously published result [6]. Fig. 3(b) shows the blocking characteristics of the 4H-SiC DMOSFET. The device required a gate bias of -2 V for a complete shutoff. The measurement was performed with a gate bias of -8 V. The device shows a leakage current of 198 μA at a drain bias of 10 kV, which corresponds to a leakage current density of 6.5 mA·cm^{-2}, normalized to the total device area including the edge termination.

Fig. 4 shows the turn-on characteristics of a 4H-SiC DMOSFET with an active area of 4.76×10^{-2} cm^2 (chip area = 0.11 cm^2). A supply voltage of 4.6 kV, a load resistance

of 3.6 kΩ, and a gate resistance of 50 Ω were used for this measurement. A current rise time (t_r) of 100 ns was measured.

III. Conclusion

10-kV, 123-m$\Omega\cdot$cm^2 power DMOSFETs in 4H-SiC are demonstrated. A 42% reduction in specific on-resistance, compared to previously reported value, was achieved by using a higher doped, thinner drift epilayer. The devices required a negative gate bias to be turned off completely. A more positive threshold voltage should be achieved for the optimization of 4H-SiC DMOSFETs. Switching measurements indicate that the 4H-SiC DMOSFETs will enable high-speed switching applications with extremely high bus voltages.

References

[1] A. Agarwal, S.-H. Ryu, and J. Palmour *et al.*, *Silicon Carbide, Recent Major Advances*, W. J. Choyke *et al.*, Eds, Berlin, , Germany: Springer-Verlag, 2004, pp. 785–812.

[2] S. Ryu, A. Agarwal, J. Richmond, J. Palmour, N. Saks, and J. Williams, "10 A, 2.4 kV power DiMOSFETs in 4H-SiC," *IEEE Electron Device Lett.*, vol. 23, pp. 321–323, June 2002.

[3] D. Peters, R. Schorner, P. Friedrichs, J. Volkl, H. Mitlehner, and D. Stephani, "An 1800 V triple implanted vertical 6H-SiC MOSFET," *IEEE Trans. Electron Devices*, vol. 46, pp. 542–545, Mar. 1999.

[4] I. A. Khan, J. A. Cooper Jr., M. A. Capano, T. Isaacs-Smith, and J. R. Williams, "High-voltage UMOSFET's in 4H-SiC," in *Proc. ISPSD*, Santa Fe, NM, June 4–7, 2002, pp. 157–160.

[5] S. Ryu, A. Agarwal, J. Richmond, and J. Palmour, "4H-SiC DMOSFETs for high frequency power switching applications," in *Proc. Mater. Res. Soc. Symp.*, vol. 764, 2003, pp. C.2.7.1–C.2.7.6.

[6] S. Ryu, S. Krishnaswami, A. Agarwal, J. Richmond, and J. Palmour, "Development of 10 kV 4H-SiC power DMOSFETs," presented at the ICSCRM Conf., Lyon, France, Oct. 5–10, 2003.

[7] V. R. Vathulya, H. Shang, and M. W. White, "A novel 6H-SiC power DMOSFET with implanted p-well spacer," *IEEE Electron Device Lett.*, vol. 20, pp. 354–356, July 1999.

[8] L. A. Lipkin, M. K. Das, and J. W. Palmour, "N_2O processing improves the 4H-SiC:SiO_2 interface," *Mater. Sci. Forum*, vol. 389–393, pp. 985–988, 2002.

[9] A. R. Hefner, and S. Bouche, "Automated parameter extraction software for advanced IGBT modeling," in *Proc. COMPEL*, July 2000, pp. 9–17.

[10] D. Stephani, "Recent progress in the development of SiC power switches," presented at the ICSCRM Conf., Lyon, France, Oct. 5–10, 2003.