Lumped-Parameter Thermal Modeling of an IPEM using Thermal Component Models

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***Abstract*—A thermal model for the CPES IPEM Gen. II is presented. The selected approach is the simulation of the thermal behavior of an experimental IPEM testbed using the 1D finite difference method. An equivalent electrical network representation of the thermal behavior of the IPEM is developed using a 1D finite approach. The SABER circuit simulation tool is used to verify the behavior of our network model and compare its results with previously acquired temperature measurements from the experimental testbed. Both experimental and simulated responses are presented and compared.**

***Index Terms*—Electro-thermal model, integrated power electronic module (IPEM), thermal components modeling.**

I. Introduction

THE Center for Power Electronic Systems (CPES) Integrated Power Electronic Module (IPEM) has been built using the embedded power packaging technology [1,2]. Electrical characteristics and reliability of the IPEM can be greatly influenced by the temperature distribution inside the module. A key specification for the design is the semiconductor device maximum allowable junction temperatures of 120°C, which is a critical issue for the reliability of this particular high power design. To study the thermal behavior of the IPEM, many computer simulations using CFD tools such as Flotherm, have been performed [3,4] during the design process. However, these simulations are slow and cumbersome, which make the development of fast models based on lumped parameters an attractive approach. Furthermore, accurate and fast electrothermal models with automated parameter extraction techniques are needed to evaluate new IPEM designs with higher power and packaging densities, and new IPEM-based power electronic systems to assess:

- long term reliability,
- maximum ratings characterization, and
- package design optimization

all of which are important to achieve CPES reliability and cost reduction objectives. This paper presents the development of a lumped parameter thermal model for the IPEM using the thermal component network approach [5,6]. IPEM geometrical and physical information is used to decompose the physical structure of the module into a series of geometrical prisms, or discrete thermal representative nodes, joined together as a network of thermal elements that are used to model the thermal behavior of the module. An equivalent circuit model is derived using a heat flow/current analogy and implemented in the SABER circuit simulation environment. This paper also present experimental validation results comparing model output with experimental results. Validation results show good agreement in steady state with errors of less than 1.5°C. The largest discrepancies were in the model time constants that shows that further model tuning is still needed.

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II. Thermal Model Development

The development of thermal models for power electronic modules and systems using thermal networks that result from direct discretization of the heat transfer equation using finite element (FEM) or finite difference (FDM) methods are presented in [7,8]. In order to consider new forms of heat dissipation and different configurations in the thermal analysis of an electronic package in these approaches, an extensive reformulation is required resulting in limited practical use of these methods in the context of design. Furthermore, the resulting thermal models are of high dimensionality, which require the application of model reduction techniques to obtain models that can be used with reasonable computation speed.

A different approach is based on thermal component networks [5,6]. A thermal component network is built in a similar fashion as a circuit, by interconnecting basic elements (compact thermal component models) where each element represents an indivisible building block (power module, heat sink, etc) used by the designer to form the thermal network. The modular structure of the models allows the designer to interchange different thermal components and examine different configurations of the thermal network easily and allows development of standard component libraries for simulation software such as SABER. The interface between the thermal and electrical networks is through the temperature dependent device models [9]. The dissipated power calculated by each device model supplies heat to the surface of the respective silicon chip thermal model through the thermal terminals. The instantaneous temperature at the surface of each silicon chip, calculated by the thermal network, is then used by the electro-thermal semiconductor model to calculate

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the electrical and power dissipation characteristics. In this way, the thermal network response is directly related to the power dissipation, and the electrical characteristics of the system are temperature dependent.

An example of the importance of modeling electro thermal interactions in electronic circuits and systems is shown in [10]. Results from this paper show that undesirable dynamical behavior such as oscillations can be caused by the electro thermal interactions that cannot be seen in a typical functional electrical model of electronic circuits.

We use an electric-thermal analogy to elaborate the IPEM thermal model. Heat transfer inside the module is modeled using several thermal resistances and capacitances. There are different methods that can be used to develop these models. We selected the finite difference method (FDM), as suggested by Hefner for its simplicity and the good results that it has shown previously [11]. Fig. 1 depicts the basic concept behind this approach. The material volume is divided into several blocks or prisms (assumed as isothermal) that will be interconnected with resistances for the thermal resistivity of the material, and capacitances that will represent the heat capacity of the material, combined altogether into an electrical network suitable for transient analysis using a circuit simulation tool such as SABER.

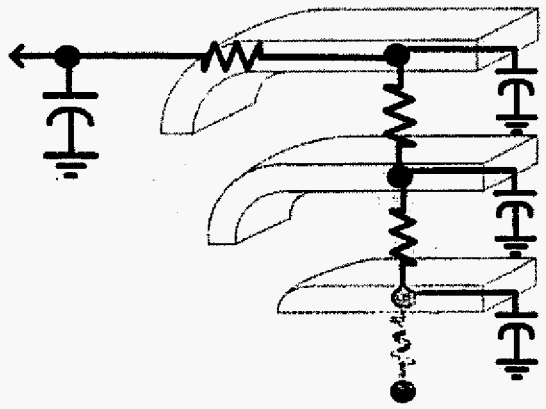

Fig. 1. Thermal node representation using an equivalent electrical network.

The SABER circuit analysis tool has the advantage of being able to represent a variety of environments other than electrical through the use of coded templates. That allows for many other systems, like mechanical and thermal networks, to be interpreted as circuit networks if their governing differential equations are coded adequately as SABER templates using the MAST language. Once these templates have all the necessary input/output pin definitions, they can be hierarchically associated to represent the whole system, or icons can be associated to them and added to the software libraries to be used in the same way as PSpice and other simulation tools do. In our case, our goal is to obtain a complete electro-thermal simulation of the CPES IPEM.

SABER has libraries of many electrical and basic thermal components. But the CPES IPEM has to be coded as a new user defined element or structure so it can be manipulated as a new thermal library component if necessary. Once this model is developed, an electro-thermal circuit simulation can be performed under the same experimental conditions of our laboratory testbed to compare its simulation results with our experimental measurements, and verify how well does the computer model fit the actual prototype behavior.

III. IPEM Structural Analysis

The first step in the development of our model is to decide how to decompose the IPEM structure into the different prisms that will compose our model. IPEM dimensions and materials are known from previous prototype designing steps. Our IPEM consists basically of two MOSFETs embedded within a ceramic dielectric, gate driver, ceramic substrate and layer, copper layer Fig. 2(b) shows a simple exploded view of the module alone without heat spreader and heat sink.

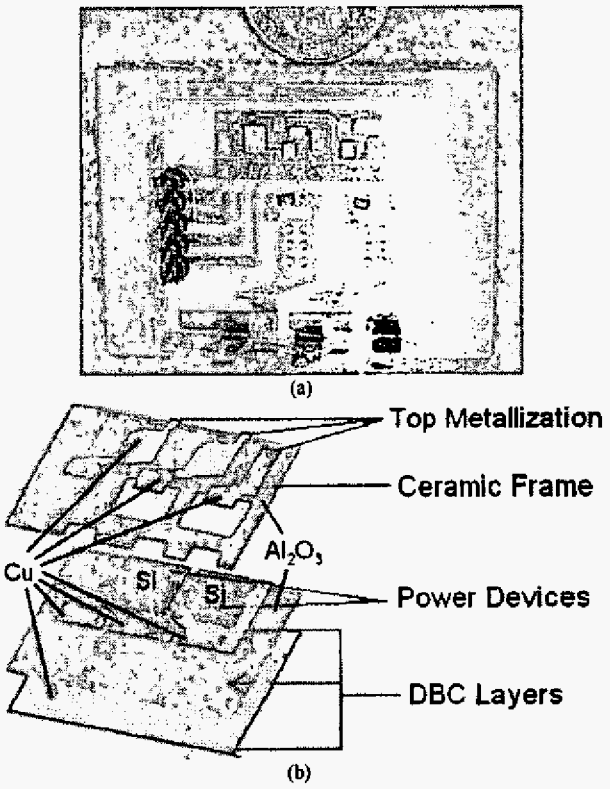

Fig. 2. CPES IPEM: (a) top view photograph, (b) exploded view of the basic module showing different materials present.

If we want to define the nodal arrangement that is to be considered for the IPEM, the influence of the junction locations is a major point of concern. It is at those locations that a higher density of nodes needs to be defined so that the thermal behavior can be correctly represented for short time-scale analysis. A higher node density will be assigned to the copper conductors in contact with the silicon elements. It will be presumed that both materials will have better heat conduction in our model geometry than the dielectric surroundings. As we get farther from the junctions, our nodes

will be less and will increase in volume due to the fact that the temperature gradients will start to decrease. Fig. 3 depicts a general representation of how the prism decomposition will be done.

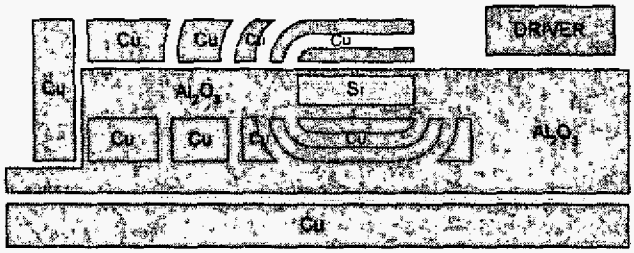

Fig. 3. Example of IPEM thermal node decomposition ("*side view*").

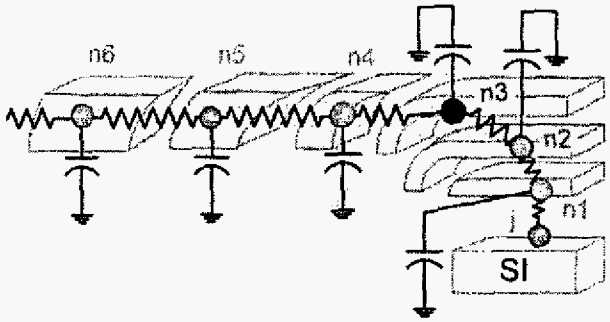

Fig. 4. Electrical network representation for the IPEM nodes.

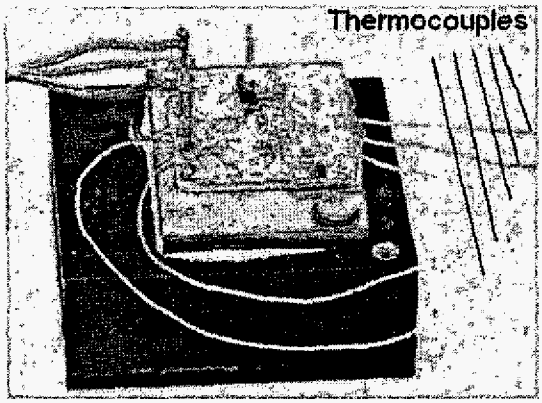

Fig. 5. Actual CPES IPEM prototype with heat spreader and heat sink.

Fig. 4 illustrates how the thermal model is derived for one of the top copper strips. The same process will be repeated for all the other elements. Once the equations of the different components are derived a Saber template is developed using the MAST language. This IPEM module will enter in contact at its bottom with whichever heat dissipation method is chosen according to the needed application. In the experimental setup, the IPEM is put on top of a copper heat spreader followed by an aluminum heat sink. Fig. 5 shows a picture of the IPEM and heat sink used in the experiment. Fig. 6 shows a diagram describing the structural composition of the experimental system.

To complete the model of the experimental system, we need to add a model for the heat sink. As described previously, at points relatively as far from the junctions, like the heat sink, there is no need to have too many nodes. The whole heat sink indeed can be represented as a single thermal lump. Fig. 7 shows the heat flow path assumed in the simulations. As we shall see, the dynamics of our assembly are dominated by the slow but strong influence of the heat sink dissipation capability. Fig. 6 is not representative enough of this effect because it is for illustrative purposes, but in Fig. 5 the actual IPEM (which has an actual area of about $1in^2$) can be compared to the rest of the assembly to get an idea of its true proportions.

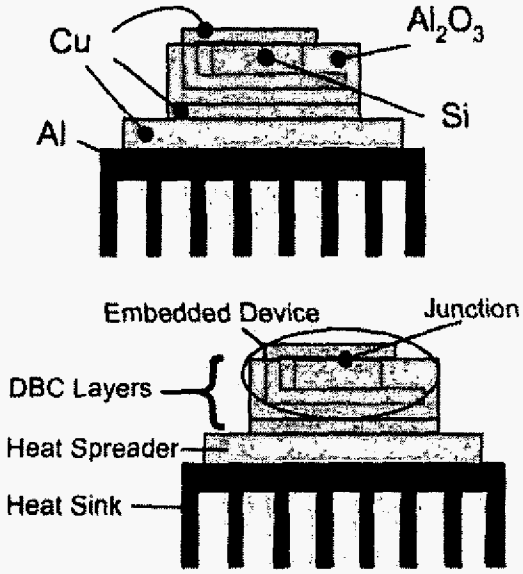

Fig. 6. IPEM materials and its basic structural description.

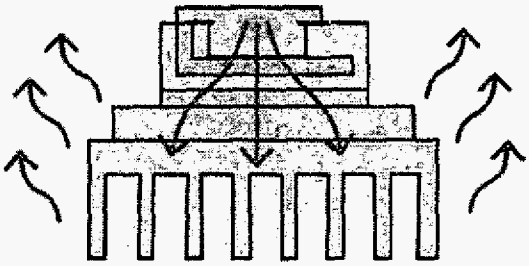

Fig. 7. Presumed heat dissipation path for the IPEM prototype.

IV. Experimental Testbeds

A. *Slow-transient experiment*

A photo of the experimental setup used to acquire slow-transient measurements when low power levels were applied to the IPEM is shown in Fig. 8. The set up is based on that described in [11,12] used for a commercial IGBT module. A matrix switch (*S*), which can handle an array of up to 39 thermocouples, and a multimeter (*M*) with integrated thermocouple-reading features capable of performing the necessary thermal measurements, are used to collect the temperature measurements. A high-power DC supply (*P*) is

used to power up the IPEM with constant but low power levels. A computer performs the automatic control of the equipment by interfacing all the instruments at once according to given specifications. All of this is coordinated through the use of a LabWindows graphical user interface application specifically designed for the experiment.

Five temperature measurements were recorded from specific locations in the IPEM. Fig. 9 shows the location of the five thermocouples. They will be identified as (G) for the one beneath the Gate driver; (L) and (R) for the "Left" and "Right" top MOSFET locations; (D) is for the one on top of the lower Dielectric layer; and (S) is for the one between the module and the Spreader. The five type-K thermocouples connected to the IPEM can be also seen in Fig. 5.

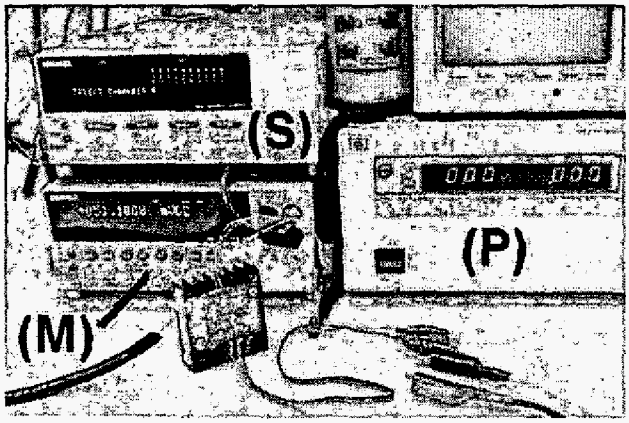

Fig. 8. Part of the experimental setup used for the slow-transient thermal measurements.

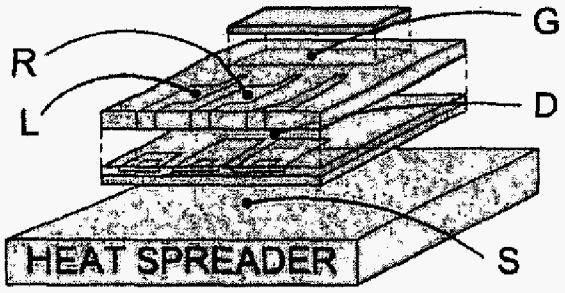

Fig. 9. Thermocouple locations for the experimental setup.

B. *Fast-transient experiment*

A photo of the experimental setup used to acquire fast-transient measurements when fast high-power levels were applied to the IPEM is shown in Fig. 10. This setup was developed in the NIST laboratories with the help of Dr. Allen Hefner and Mr. David Berning, which have performed similar analyses described in [11]-[13]. In this case, square pulses ranging from 125W to 850W, but lasting only milliseconds, were applied to the devices so that only the vicinity of the junctions would heat up for a brief instant. Temperatures would be measured indirectly by monitoring the gate voltage (which is temperature dependent) by using a controlled heat plate and an oscilloscope. Calibration curves were determined first by measuring the gate voltage at different temperatures, so that the measured gate voltages generated by the fast power pulses would give a temperature profile showing how the junctions heated up during the duration of the applied pulses.

V. Validation of Experimental Results

A. *Slow-transient validation*

In the slow-transient experiment, the MOSFETs in the IPEM were used as a constant power inputs to the package. A schematic for the experimental circuit is shown in Fig. 11. The data acquisition system collects data from the output of the thermocouples and the measured temperature responses are compared against the output of the model for validation. An alternative experiment approach is to control the MOSFETs using their gate drives to study high frequency behavior. Here we report results for the constant power source experimental work. The tests were performed applying 1 to 7W constant steps to each of the devices. The output voltage of the DC source varied between 1 to 1.5 volts and the current according to the required power level.

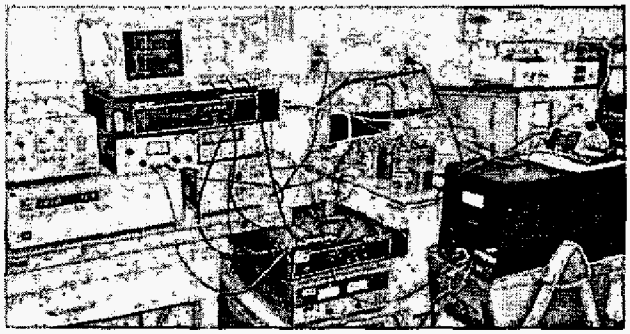

Fig. 10. Part of the experimental setup used for the fast-transient thermal measurements.

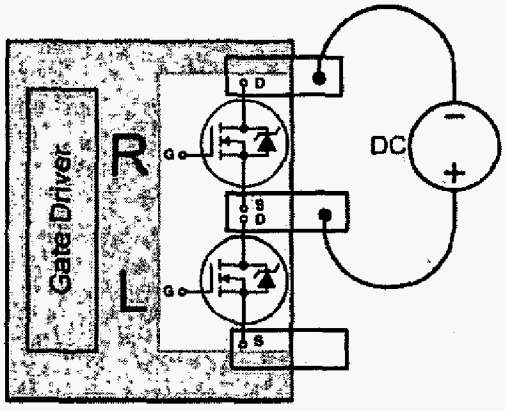

Fig. 11. Example of the power connection for the slow-transient experiment.

In some cases, the current signal from the source changed in magnitude as the device heated up but not significantly. Our computer-controlled system recorded all the five temperature measurements along with the power readings from the source and an ambient temperature reading from an

extra thermocouple. Fig. 12 shows the graphical representation in SABER of the IPEM thermal model that is being used to simulate the slow-transient experimental setup. It shows the SABER representation for the IPEM thermal model developed in this research. Samples of the experimental and simulated responses are shown in Fig. 13 and Fig. 14.

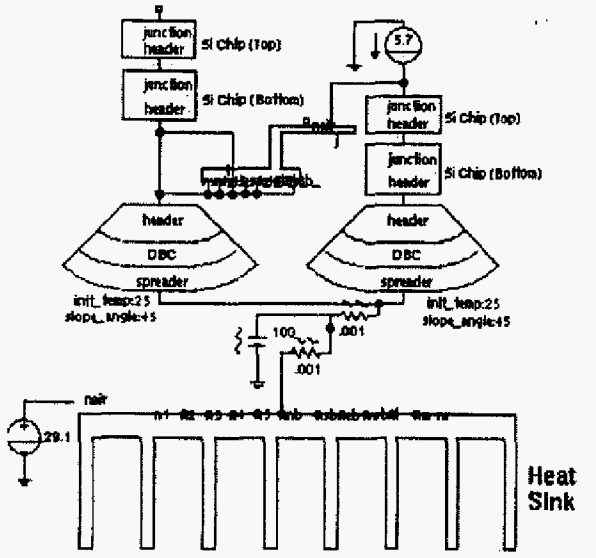

Fig. 12. SABER model for the slow-transient experimental system.

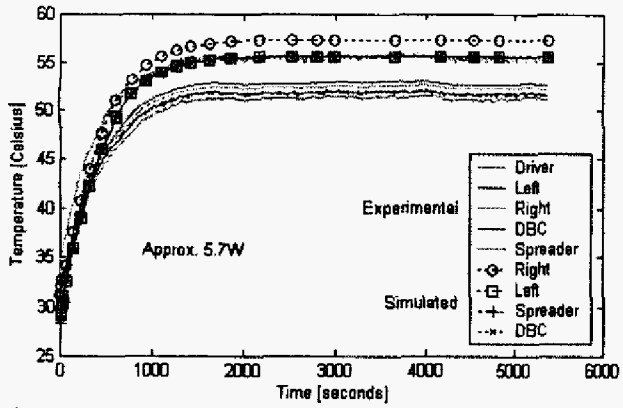

Fig. 13. 5.7W comparison of experimental vs. simulated behavior for the slow-transient experimental system (rightmost "*R*" chip).

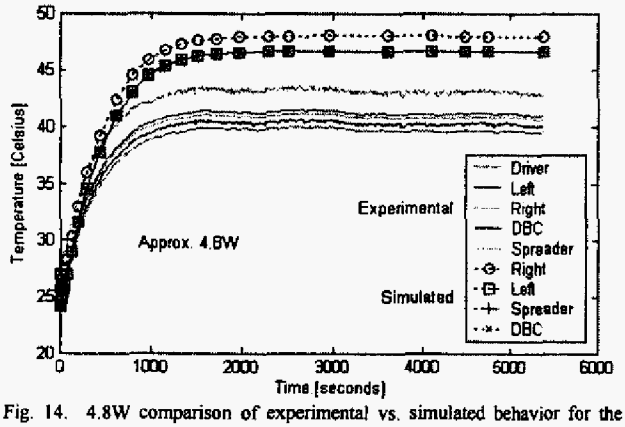

Fig. 14. 4.8W comparison of experimental vs. simulated behavior for the slow-transient experimental system (rightmost "*R*" chip).

It can be seen that, although their transient portions behave similarly, the final steady temperatures differ by a couple of degrees. This could be arising from the fact that the heat sink cannot be modeled following the IPEM thermal component approach due to the nonlinear behavior of the convection in the fins of the heat sink. We need to do further analysis on the model and parameters in order to fix this discrepancy. The heat sink dominates the heat flow dynamics in the slow-transient case. It is difficult to model the heat sink's complex geometry and thermal behavior using the method depicted in Fig. 1.

B. Fast-transient validation

A schematic of the experimental circuit for the fast-transient experiment is shown in Fig. 15. The data acquisition system was used initially to obtain necessary calibration curves to relate the gate voltages of the devices to their temperature, like the ones shown in Fig. 16. Fig. 17 shows the experimental results once analyzed according to these calibration curves. Fig. 18 shows the graphical representation in SABER of the fast-transient IPEM thermal model variation from that in Fig. 12. Note that in this case the heat sink is not present because the experiment is mounted in a controlled heat plate at a constant temperature of 25 degrees. This plate is being represented with a constant temperature source. Samples of the experimental vs. simulated responses are shown in Fig. 19- (a), -(b), and -(c).

It can be observed in Fig. 19 that our model represents better high-power levels than low-power ones. This arises from the fact that the high-power pulses generated during the experiment (and their simulated equivalents) are shorter in duration, thus they dissipate faster within the IPEM materials, mostly within the silicon, as their heat spreads within the module. These pulses will dissipate in the close vicinity of the silicon devices, but low-power pulses, lasting longer, have the opportunity to affect the surrounding ceramic layers. As the model thermal components grow in size and distance from the heat source, their thermal response starts to deviate from the experimental measured behavior.

VI. Conclusions and Future Work

A lumped parameter thermal model for the CPES IPEM based on the thermal component modeling method was presented. Experimental data was used to validate the developed model under different power levels. Comparison between experimental and simulation results show an acceptable agreement in steady state temperature with errors of less than 3°C for the slow-transient case, while the fast-transient analysis showed a very good agreement for high power levels. Nevertheless, some discrepancies also appeared when low power levels are simulated for the fast-transient experiment. We argue that a potential source of the error in both analyzed transients might be the effects arising from the heat sink model present in the slow-transient case, and the constant temperature hot plate in the fast-transient one, which dominate the thermal system response for each setup, respectively. These models will be revised to improve the model behavior under low-power level conditions.

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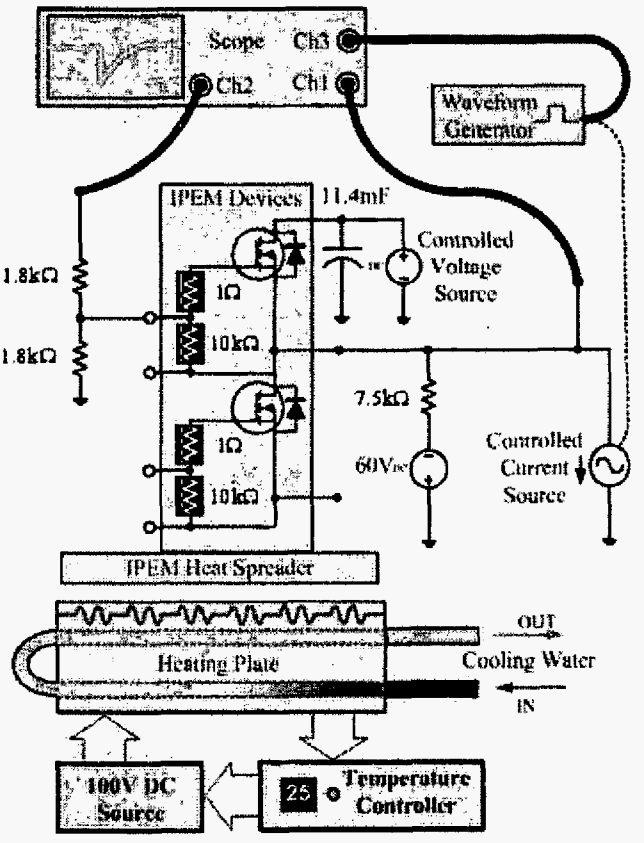

Fig. 15. Schematic of the electrical connections in the fast-transient experiment.

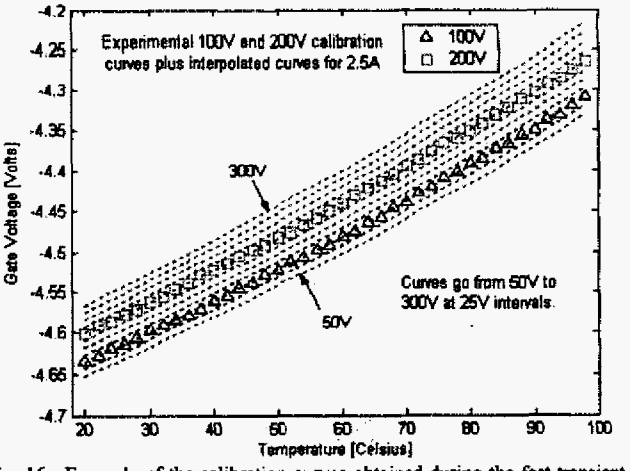

Fig. 16. Example of the calibration curves obtained during the fast-transient experiment.