Fabrication and Measurement of Tall Stacked Arrays of SNS Josephson Junctions

Nicolas Hadacek, P. D. Dresselhaus, Y. Chong, S. P. Benz, and J. E. Bonevich

***Abstract*—The authors have made tall, uniform stacked Josephson junction arrays by developing an etch process using an inductively coupled plasma etcher. This process produces vertical profiles in thin-film multilayers of alternating superconducting and normal metals. Such a vertical etch is necessary to obtain uniform properties in high-density arrays in order to achieve operating margins for voltage-standard applications.**

The authors use dry-etchable $MoSi_2$ for the normal metal barrier of our niobium Josephson junctions and obtain working series arrays with stacks up to 10 junctions tall. The authors present dc and microwave electrical characteristics of distributed and lumped arrays and discuss the technological improvements needed to fabricate lumped arrays for voltage-standard applications.

***Index Terms*—Josephson junction, lumped array, $MoSi_2$, multilayer, voltage standard.**

I. Introduction

Superconductor-normal metal-superconductor (SNS) junctions have greater fabrication reproducibility than Josephson junctions with an insulating barrier. They also have intrinsically stable voltage steps and better noise immunity due to their nonhysteretic electrical properties and large critical currents. This has allowed the development of programmable Josephson voltage standards (PJVS) [1] and of the Josephson arbitrary waveform synthesizer (JAWS) [2].

In order to improve the performance of voltage standards, there is a technological effort to pack junctions more densely into arrays [3]–[6]. For programmable voltage standards this will increase the output voltage for a given microwave drive frequency and chip area; for the ac voltage standard it will increase the output voltage, output bandwidth, and operating margins. In this paper we describe the fabrication technology of stacked junctions and report flat Shapiro steps for arrays with stacks of up to 10 junctions each. Arrays with two and three junctions per stack have already been used in functional PJVS chips [7] and JAWS circuits [8]. Stacked junctions have also been fabricated in $NbN - TiN_x - NbN$ [3] and BSCCO [4], but reproducible tall stacks with more than two junctions have been difficult to obtain in these material systems.

For sufficiently large junction density or low drive frequency, an array will act as a lumped microwave element, where its physical length is short with respect to the microwave drive wavelength. If the impedance of such lumped arrays can be matched to the transmission line, it will remove standing waves in the microwave structure, leading to higher microwave uniformity and thus larger operating margins. Higher junction density will also reduce parasitic and transmission-line inductances leading to lower input-output coupling and improved JAWS performance.

It has been suggested [9] that the optimal voltage-standard circuit will be a 50 Ω lumped array of Josephson junctions. If one assumes a 15 GHz drive frequency, a 40 μV matching characteristic voltage and a 10 mA critical current, one needs 12 500 junctions within a 1.85 mm long transmission line. This requires an average junction spacing of 148 nm—clearly a challenge for fabrication technology where planar junctions are typically separated by a few micrometers. Note that this maximum length per junction is independent of the chosen microwave frequency; for a given voltage the number of junctions decreases linearly with frequency, but the lumped-element length also decreases linearly.

In our distributed-array circuits, the typical junction spacing is 7 μm. Finer lithography leads only to small improvements in spacing because the junctions are already a few micrometers large in order to realize practical critical currents. Higher linear junction density can be reached either by reducing the size for in-line junctions or by vertically stacking planar junctions. Fabricating closely spaced in-line junctions requires a different technology, and such technologies have not shown the uniformity and scalability to large junction counts needed for voltage-standard applications [10].

The technology for planar junctions is well developed and has excellent uniformity because it is possible to sputter barrier materials with thickness variation less than 1 nm across a wafer. Since the critical current depends exponentially on the barrier thickness, a uniform barrier is key to a narrow distribution of critical currents in large arrays. In addition, lithographic definition of micrometer-sized junctions gives good control of the junction area on which the critical current depends linearly. These two technological advantages also aid the uniformity of stacked planar junctions. The same thin-film techniques that have already proven to yield voltage-standard circuits are used, with only the junction material and the etch process needing refinement.

II. Fabrication

The first step was to find a barrier material that could be dry-etched with niobium and produced uniform single-junction arrays. The authors found that $MoSi_2$ is an excellent barrier

Manuscript received October 5, 2004. This work was supported in part by the Office of Naval Research under Contract N00014-03-IP-20023 and Contract N00014-04-IP-20044.

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Digital Object Identifier 10.1109/TASC.2005.849706

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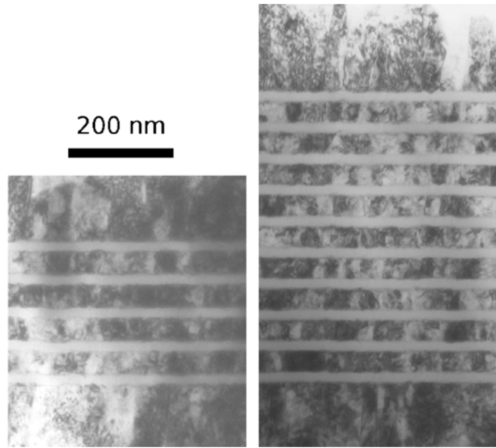

Fig. 1. Transmission electronic microscope (TEM) cross-sections of 5- and 10-junction multilayers. The 23 nm $MoSi_2$ barriers appear lighter than the niobium electrodes. The middle electrodes are about 40 nm thick.

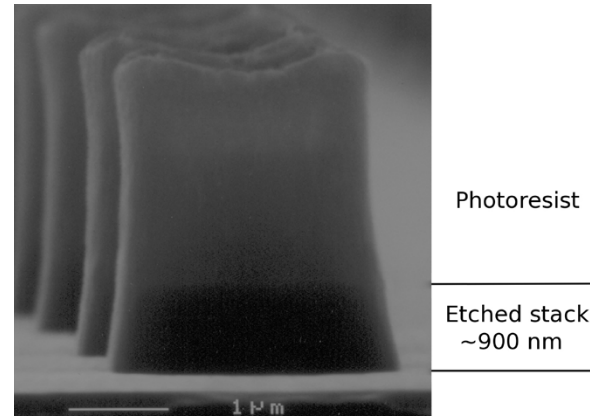

Fig. 2. Scanning electronic microscope (SEM) picture showing the etch profile for patterned 10-junction multilayers. The photoresist is still present on top of the stacks.

material compared to other materials [6]. The run-to-run reproducibility and high resistivity ($\sim 700\ \mu\Omega\,\mathrm{cm}$) with no measured superconducting critical temperature, provide reliable characteristic voltage targeting and straightforward processing [11]. $MoSi_2$ is sputtered in an argon plasma from a stoichiometric target. As shown in Fig. 1, the barrier is amorphous and has a very smooth interface with the niobium electrodes. $Nb/MoSi_2$ multilayers are alternately dc-sputtered from two targets; the thicknesses of the different layers are determined by the respective deposition times, precisely defined by a computer-controlled system of shutters.

The main fabrication challenge is to achieve a vertical etch profile so that all stacked junctions have the same area, and thus the same critical current. Most of the development work has been on finding a vertical etch process that was scalable to tall stacks, while we have kept the rest of our existing fabrication process for planar niobium SNS junctions. Preliminary etches used a reactive ion etcher (RIE) with a recipe similar to that used for niobium [6]. The process parameters were modified by adding oxygen to the SF_6 plasma to get similar etch rates for Nb and $MoSi_2$. Also the plasma pressure was reduced to get a more anisotropic etch. However, in RIE the plasma is capacitively coupled to the electrode, hence the energy and density of ions cannot be independently adjusted. As a result, the plasma pressure is relatively high compared to the ion density, and the resulting ion scattering limits the etch anisotropy.

In addition, the introduction of oxygen into the plasma leads to an increased etch rate for the photoresist combined with a lower etch rate for Nb. This results in longer etch times with excessive removal and degradation of the resist, even at reduced microwave power. Given all these constraints, the RIE process is limited to stacks with a maximum of five junctions.

Inductively coupled plasma (ICP) etching is similar to RIE except it offers more flexibility in process control [12]. The plasma is inductively coupled to the main microwave source ("ICP source"), which regulates ion density. Another microwave source ("RIE source") connected to the platen holding the wafer is capacitively coupled to the plasma and allows independent control of the ion energy. In this system, it is possible to obtain low-pressure plasmas with high ion density, thus enhancing the ion mean free path and etch anisotropy. ICP machines are used mainly for deep silicon etching with a special recipe, called the "Bosch process", consisting of short alternating steps of etching in a SF_6 plasma and passivating in a C_4F_8 plasma. This process allows vertical etch profiles hundreds of micrometers deep in Si [13]. For etching $Nb/MoSi_2$ multilayers we have developed a different recipe using a mixture of SF_6 and C_4F_8. At low pressure (7 mTorr) and high RIE power (30 W) the etch profile is vertical because the polymer layer deposited by C_4F_8, protects the etched Nb sidewalls from undercut, even though the etch rates for the two materials differ by over a factor of 10 (~3.3 nm/s for Nb and ~0.3 nm/s for $MoSi_2$). Back-side helium gas cooling at $30^\circ\mathrm{C}$ prevents degradation of the photoresist from heating. However, even at low ICP power (300 W), the etch selectivity to the photoresist is less than 1, only slightly higher than that obtained with RIE. A 3 $\mu\mathrm{m}$-thick photoresist must be used to etch multilayers with more than five barriers. Another problem in higher stacks is nonuniform etch rate across the wafer; this is caused most likely by either loading of the SF_6 plasma or insufficient reactant out-flow.

III. Measurement and Discussion

Our primary diagnostic to assess the quality of the etch process is direct observation with a scanning electronic microscope. Chips are cleaved perpendicularly to an elongated patterned structure to obtain cross-sectional views. Fig. 2 is such a picture of the etch profile for a test structure of 10-junction stacks with photoresist still on top. The profile shows a variation in lateral dimension of about 150 nm from the top to the bottom of the stack. For stacks of area $4\ \mu\mathrm{m} \times 8\ \mu\mathrm{m}$, this leads to a nonuniformity of about 11%, which should be tolerable for voltage-standard applications.

The junction uniformity can best be determined by measuring the electrical properties. The current-voltage $(I-V)$ characteristic of arrays with applied microwave irradiation is of particular importance since the size of the Shapiro steps is the main criterion for dc voltage standards. Usually a minimum step size of 1 mA is necessary for stable operation. For the JAWS, steps need to be large over a wide frequency band (e.g., from 1 to 20 GHz),

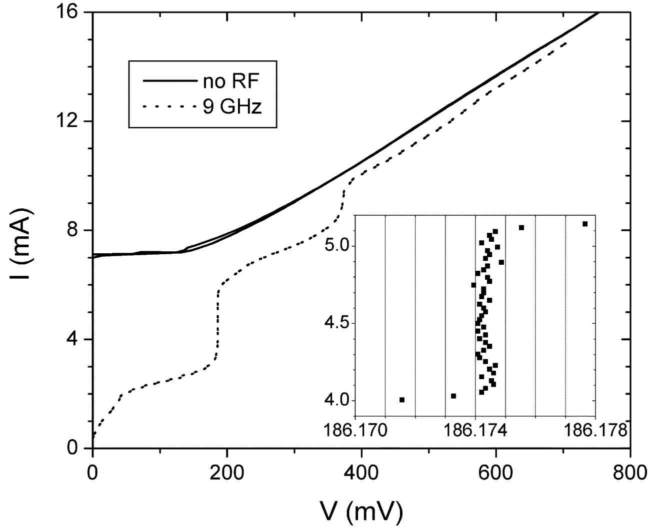

Fig. 3. $I-V$ characteristics at dc and with a 9 GHz applied microwave drive for an array of 1000 stacks of 10 junctions each. *Inset*: detail of the first step at 9 GHz showing a 1 mA step that is flat within the 1 μV measurement noise.

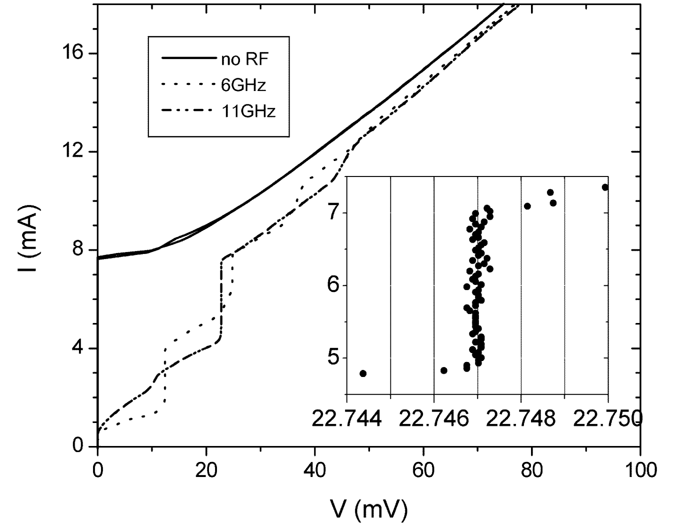

Fig. 4. $I-V$ characteristics at dc and with microwave drive at 6 and 11 GHz for an array of 100 stacks of 10 junctions each. *Inset*: detail of the first step at 11 GHz showing a flat step over 2 mA.

a much stronger requirement than for dc voltage standards that operate at fixed frequencies.

Fig. 3 shows $I-V$ characteristics for an array of 1000 stacks of 10 junctions each. The array is embedded in a coplanar waveguide (CPW) with a termination resistor of 50 Ω. Current bias and voltage measurements are made through taps and on-chip filters placed at each end of the array. The junctions are $5.5\ \mu\mathrm{m}\times 6\ \mu\mathrm{m}$ with 23 nm-thick $\mathrm{MoSi_2}$ barriers and 40 nm-thick Nb middle electrodes. The array has a critical current $I_c = 7.1$ mA, and a characteristic voltage $V_c = I_c.R_n = 36\ \mu$V, where R_n is the junction normal resistance. Constant-voltage steps are observed at the correct voltage with a $\sim$1 mA current range over the drive frequency range, 8 GHz to 10 GHz. This demonstrates that all 10 000 junctions are working correctly and have excellent uniformity.

Smaller flat steps are measured between 10 GHz and 14 GHz. The distributed nature of this array (total length $\sim$8 mm with one 180° CPW turn) and the large number of junctions (the total normal resistance is 51 Ω) significantly attenuate the microwave signal along the array, thus decreasing the step sizes. In addition the maximum current I_{max}, before the stack is driven normal due to heating [14], is $\sim$17 mA for this array, only 2.3 times larger than I_c, so we suspect that self-heating may also degrade the step current range. Removal of heat could be enhanced by fabricating the junctions on a bare silicon substrate instead of one with a thermal oxide [14]. Thus, reducing the array length and improving the heat flow would increase the size of the current steps, particularly at high frequencies.

Fig. 4 shows $I-V$ characteristics for a shorter array of 100 stacks with 10 junctions each. This circuit with only 1000 junctions, shows a larger step than the longer array in Fig. 3. Table I compares measured electrical characteristics for similar 100-stack arrays with 1, 5, 10, and 15 junctions per stack. Multilayers for the 1-, 5-, and 10-junction stacks have been deposited on oxidized silicon wafers; for the 15-junction array, trench holes were opened through the thermal oxide to make direct contact between niobium and silicon in order to have better removal of heat from the junctions. This increased I_{max} by about 20% as compared to a similar structure fabricated on the oxidized wafer. Measured critical currents decrease for taller stacks even with a constant nominal junction size $(4\ \mu\mathrm{m}\times 8\ \mu\mathrm{m})$ and barrier thicknesses (23 nm). This is caused most likely by an increased etch run-out (smaller junction area) for the longer etch times needed for these tall stacks.

TABLE I
PROPERTIES OF 100-STACK ARRAYS WITH DIFFERENT NUMBER OF JUNCTIONS PER STACK, SHOWING THE CRITICAL CURRENT I_c, THE CHARACTERISTIC VOLTAGE V_c OBTAINED BY FIT, THE NORMAL RESISTANCE R OF THE ENTIRE ARRAY, AND THE MAXIMUM CURRENT I_{max}. NOMINAL JUNCTION SIZE IS $4\ \mu\mathrm{m}\times 8\ \mu\mathrm{m}$, BARRIER THICKNESS IS 23 nm AND MIDDLE ELECTRODE THICKNESS IS 40 nm (60 nm FOR THE 15-JUNCTION STACKS)

	I_c (mA)	V_c (μV)	R (Ω)	I_{max} (mA)
1 junction	10.9	37	0.3	75
5 junctions	8.6	38	1.8	32
10 junctions	8.0	35	4.3	22
15 junctions	7.8	37	5.8	19

The length of the 100-stack arrays is $\sim 800\ \mu\mathrm{m}$, which corresponds to the quarter wavelength of a 37 GHz signal for our CPW. Unlike the distributed-array design, there is no termination resistor, and the array is instead shorted to ground at one end. A termination resistor is useful in reducing standing waves in distributed arrays but introduces a common-mode signal that prevents the circuit from being directly connected to the measurement system. The frequency dependences of the zero and first step are plotted in Fig. 5. Flat steps of more than 2 mA exist at all frequencies between 6 GHz and 15 GHz; the features around 9 GHz, 13 GHz, and 17 GHz are due to resonances in the microwave circuit (including the cryoprobe).

Arrays of the same design (shorted to ground) but with 250 10-junction stacks show steps with only very small current ranges. The greater length of these arrays (2 mm) corresponds to a quarter of the wavelength at 15 GHz and above this frequency, standing waves will occur inside the array, decreasing the current range. Since the junction characteristic voltage is

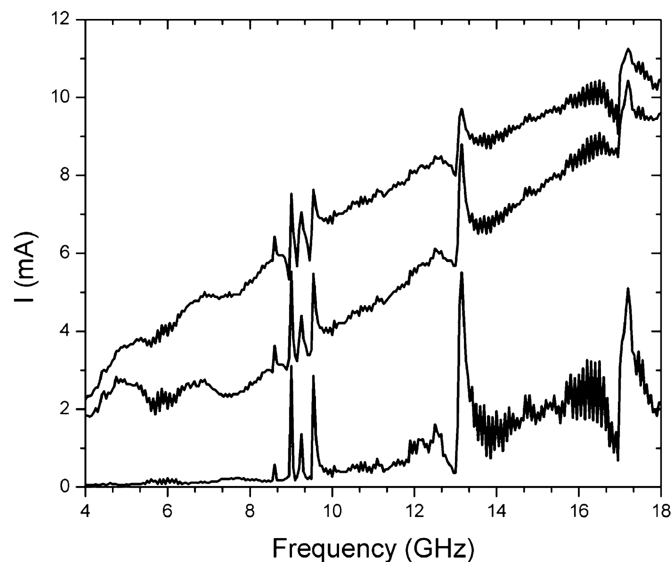

Fig. 5. Shapiro step size versus frequency for a 100-stack array with 10 junctions each. The bottom curve is for the zero-step upper bound, and the two top curves are the upper and lower bounds of the flat region of the first step (with a 20 μV measurement window). Microwave power was optimized to obtain the largest first steps.

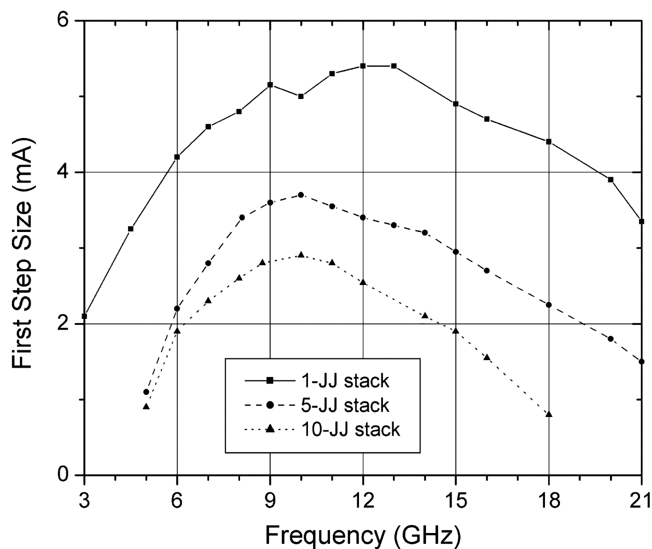

Fig. 6. First Shapiro step size versus frequency for 100-stack arrays with 1, 5, and 10 junctions each. Microwave power was optimized to obtain the largest steps.

optimized to have large steps also around 15 GHz, this may explain why these longer arrays do not have large constant-voltage steps.

Fig. 6 compares step sizes for 100-stack arrays with different numbers of junctions per stack. The maximum step size is obtained for the array with a single junction per stack around 13 GHz, which is close to the expected maximum for the characteristic voltage of 35 μV. However arrays with 5- and 10-junction stacks have maximum step sizes around 10 GHz, which is significantly lower than their characteristic voltage. Non-equilibrium effects under microwave irradiation (such as heating) in the thin 40 nm middle electrodes could reduce the effective characteristic voltage and cause this lower peak frequency response.

IV. Conclusion

The authors have developed a new etch process that gives vertical profiles for up to 15 stacked junctions (more than 1 μm tall). Flat Shapiro steps with current range ~1 mA have been measured over a narrow frequency range for distributed arrays of 1000 stacks with 10 junctions each. Shorter arrays of 100 stacks with 10 junctions each have yielded 2 mA steps between 6 GHz and 15 GHz. These results are promising, and we expect further improvements in the fabrication technology to provide denser arrays and to allow lumped arrays to be optimized for voltage-standard applications.

Acknowledgment

The authors are grateful to Charles J. Burroughs for developing and constructing the measurement probes.

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