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# Single-electron transistor spectroscopy of InGaAs self-assembled quantum dots

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**Abstract**

A single-electron transistor (SET) is used to detect tunneling of single electrons into individual InGaAs self-assembled quantum dots (QDs). By using an SET with a small island area and growing QDs with a low density we are able to distinguish and measure three QDs. The bias voltage at which resonant tunneling into the dots occurs can be shifted using a surface gate electrode. From the applied voltages at which we observe electrons tunneling, we are able to measure the electron addition energies of three QDs.


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The large Coulomb blockade and quantum efficiency of InGaAs self-assembled quantum dots (QDs) provides the potential for new optoelectronic devices. For example, in an electrically biased photon turnstile, a *p–i–n* diode structure with a QD embedded within the insulating (i) layer allows the tunneling of an individual electron and hole onto a QD with voltage biasing [1]. At the end of the biasing cycle, a created exciton decays radiatively, creating an electrically triggered single photon on demand. Such a single-photon source is desired for quantum cryptography systems because the production of multiple photons from currently available sources limits the security of data transmission [2].

Electrically biased sources of single photons have been realized with a QD etched from a quantum well [3] and by driving current through a large ensemble of self-assembled QDs and collecting light from a single dot [4]. A photon turnstile utilizing a single InGaAs self-assembled QD would combine the well-defined current path achieved in Ref. [3] with the quantum efficiency of the InGaAs QD used in Ref. [4]. Such a device promises high-fidelity production of single photons.

Precise control of a single-QD device requires a detailed understanding of the electrical behavior of the QD. A natural tool for probing a single QD is the single-electron transistor (SET) [5], whose extraordinary sensitivity as an electrometer allows the detection of one-electron tunneling into one QD even though only a small fraction of an electron charge *e* couples to the SET. SETs have previously been used to detect the addition of individual electrons in a QD etched from a GaAs quantum well [6] and in QDs formed from a gated two-dimensional electron gas [7].

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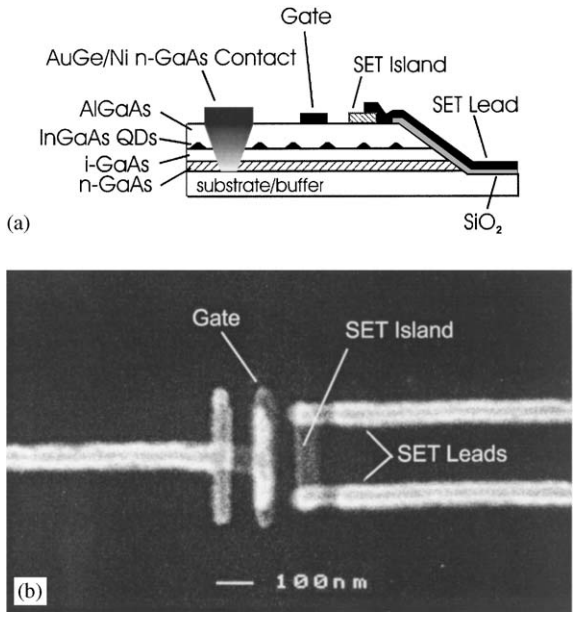


Fig. 1. (a) Cross-sectional diagram of device structure, (b) a scanning electron micrograph of an SET structure over QDs. From the area of the island ($60 \times 300$ nm$^2$) and the average density of the dots ($\sim 10^{10}$ cm$^{-2}$), there are approximately 2 QDs under the SET island.

Here we present results for an SET coupled to three InGaAs self-assembled QDs in the structure shown in Fig. 1(a). The QDs are separated from an n-doped GaAs layer below by an intrinsic GaAs tunnel barrier and from the surface above by an AlGaAs blocking layer. Metal electrodes on the surface form the SET and gate. For certain voltages applied to the n-doped layer and gate, electrons tunnel from the n-doped layer into the QDs. The SET detects these events through a charge induced on its island, which is typically different for each QD. The gate voltage dependence of the tunneling condition and the amount of charge detected by the SET allow us to determine the approximate positions of the individual dots. From the voltage dependence of the tunneling events, the electron addition energies of individual QDs are extracted. We also present conventional photoluminescence and capacitance–voltage ($C$–$V$) measurements from the same wafer for comparison, similar to previous $C$–$V$ measurements on InGaAs QDs [8], our $C$–$V$ measurements probe large ensemble properties of QDs.

The semiconductor structure is epitaxially grown on a 76 mm semi-insulating GaAs wafer, rotated during growth for uniformity. The epitaxial layers consist of an undoped GaAs buffer, a 200 nm n-doped GaAs layer, a 40 nm intrinsic GaAs layer, a layer of $In_{0.44}Ga_{0.56}As$ resulting in QDs of density $\approx 1 \times 10^{10}$ cm$^{-2}$, a 5 nm intrinsic GaAs buffer, a 40 nm$Al_{0.4}Ga_{0.6}As$ layer and a 5 nm intrinsic GaAs cap layer.

Device fabrication involves photolithography steps followed by an electron-beam lithography step. First, Ni/AuGe pads are evaporated and annealed to form contacts to the n-doped layer. Then a mesa is wet etched from the epitaxial layers, and its side walls are insulated with $SiO_2$. This is followed by evaporation of Ti/Au to define large-scale wiring, bonding pads, and the top electrode for $C$–$V$ measurements. Next, a bilayer of PMMA/copolymer is spun on the wafer and it is diced into chips. The SET and gate are formed with electron-beam patterning and double-angle evaporation of Al, with an oxidation step to form the SET junctions.

A top view of the SET structure is shown in Fig. 1(b). The SET contains an island and two leads that connect electrically to the island through tunnel junctions. Sweeping any nearby voltage, such as the gate voltage in our experiment, modulates the SET conductance [5]. The SET is also sensitive to any other sources that induce charge through their capacitances to the island, and thus it can detect electrons tunneling into nearby QDs. Background charge traps also influence the SET and we discuss how to distinguish tunneling into QDs from charge traps below.

We operate our SETs in the superconducting state in a $^3$He refrigerator. The chip is mounted inside an RF-tight box with metal powder filters attached to the leads entering the box. We current-bias the SET through a 1 MΩ resistor and apply a feedback voltage on the gate to keep $V_{SET}(\approx 1$ mV) constant. The modulation of the Coulomb gap in the SET implies a total island capacitance of $\approx 320$ aF. The gate and n-doped layer capacitances are $C_G = 0.74$ aF and $C_n = 27$ aF.

A schematic representation of the circuit is shown in Fig. 2. The gate voltage has three components: $V_G = V_{FB} + V_{bal} + V_{off}$. $V_{FB}$ is the voltage from the feedback circuit described above. $V_{bal} = -(C_n/C_G)V_G$ is a balancing voltage that counteracts the direct capacitive coupling between the n-doped layer and the SET

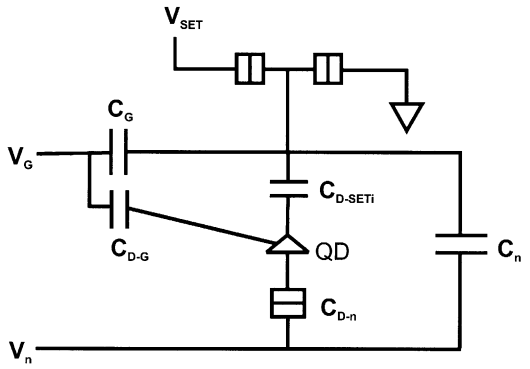


Fig. 2. Schematic diagram of InGaAs QD measurement with an SET. The SET island is capacitively coupled to the n-doped layer ($C_n$), the gate ($C_G$); and the QD ($C_{D\text{-}SETi}$).

island. $V_{off}$ is an offset that can be changed between data traces to help determine the positions of the QDs. Due to $V_{bal}$ when $V_n$ is swept $V_{FB}$ does not respond to the continuous variation of charge of $C_n$, but responds to the motion of discrete charge onto the QDs. The charge induced on the SET island is expressed as $Q^* \equiv C_G V_{FB}$. As an electron tunnels onto a QD, the measured signal is $\Delta Q^* = C_G \Delta V_{FB} = eC_{D\text{-}SETi}/C_{D\text{-}\Sigma}$, where $C_{D\text{-}SETi}$ is the capacitance between the dot and the SET island and $C_{D\text{-}\Sigma}$ is the total capacitance of the dot.

Writing all energies relative to the zero-bias Fermi energy, the $N$th electron is added when the Fermi energy of an electron from the n-doped layer, $-eV_n$, is equal to the change in free energy $F$ of the QD:

$$-eV_{n,N} = F(N) - F(N-1) \equiv E(N) - eV_{ext,N}. \quad (1)$$

For convenience, the addition energy

$$E(N) = e\alpha\left(V_{G,N}\frac{C_{D\text{-}G}}{C_{D\text{-}\Sigma} - C_{D\text{-}n}} - V_{n,N}\right) \quad (2)$$

is used to describe the energy levels of the QD, independent of the externally induced potential, $V_{ext} = (V_n C_{D\text{-}n} + V_G C_{D\text{-}G})/C_{D\text{-}\Sigma}$, of the QD. $C_{D\text{-}G}$ is the dot-to-gate capacitance and $\alpha = (C_{D\text{-}\Sigma} - C_{D\text{-}n})/C_{D\text{-}\Sigma}$ is a constant that depends on the sample geometry. To interpret our results, we make the approximation $C_{D\text{-}\Sigma} = C_{D\text{-}G} + C_{D\text{-}n} + C_{D\text{-}SET}$, where $C_{D\text{-}SET} = C_{D\text{-}SETi} + C_{D\text{-}SETl}$ is the sum of dot capacitances to the SET island and SET leads.

For a metallic QD with capacitance $C$, $E(N)$ would equal the Coulomb blockadge energy $E(N) = (N - \frac{1}{2})e^2/C$. In an InGaAs QD, there is an $N$-dependence of the addition energy spacing due to single particle energies and Coulomb interactions. The first electron will resonantly tunnel at $E(1)$ equal to the $s$ orbital energy level relative to the zero bias Fermi energy, and the second electron will enter the same orbital, separated by a Coulomb interaction energy $E_{ss}^{C} = E(2) - E(1)$. The difference in the first and third electron addition energy is $E(3) - E(1) = \Delta\varepsilon + 2E_{sp}^{C} - E_{sp}^{x}$, where $\Delta\varepsilon$ is the difference in the $s$ and $p$ orbital energies and $E_{sp}^{C}(E_{sp}^{x})$ is the direct (exchange) Coulomb energy.

$C$–$V$ and photoluminescence spectra taken at or below 4.2 K are used to characterize the ensemble average properties of the QDs. The inset to Fig. 3 shows $C$–$V$ data taken at $f = 100$ Hz from a (64 μm)$^2$ top electrode on the same chip as our SET measurements. The data show a large shoulder at $V_n = -1.2$ V, which represents electrons tunneling into the wetting layer surrounding the QDs. At $V_n = -0.80$ and $-0.95$ V, we observe peaks associated with electrons tunneling into QDs. Photoluminescence data, from the same wafer as our SET measurements (inset to Fig. 3), also show a QD exciton energy of 1.23 eV, which is close to the exciton emission of 1.36 eV from the wetting layer.

In Fig. 3 we show $Q^*$ as a function of $V_n$ for different $V_{off}$. The steps marked with symbols can be identified with tunneling into QDs for several reasons. (1) In the top curve of Fig. 3, the first reproducible and nonhysteretic step as we sweep down from $V_n = 0$ is observed at $V_n = -0.81$ V. Since $V_G$ is relatively small for this curve, we can compare this directly to the $C$–$V$ data, which also show the first feature at $V_n \approx -0.8$ V. (2) The steps do not depend on sweep direction and their heights and spacings for a particular QD are unchanged with thermal cycling. This distinguishes them from changes in trapped charge [10]. (3) The different curves in Fig. 3 (and the analysis below) show that the features shift as predicted by Eq. (2).

For $V_n \gtrsim -0.8$ V, $Q^*$ is relatively constant with occasional hysteretic features that change with thermal cycling. These features are charge traps and behave similarly to those studied in an SET on a bare substrate [10]. Charge traps are also observed near the QD features and two examples are marked by ovals in the lowest curve in Fig. 3. In the bias region where the $C$–$V$ measurement shows tunneling into the

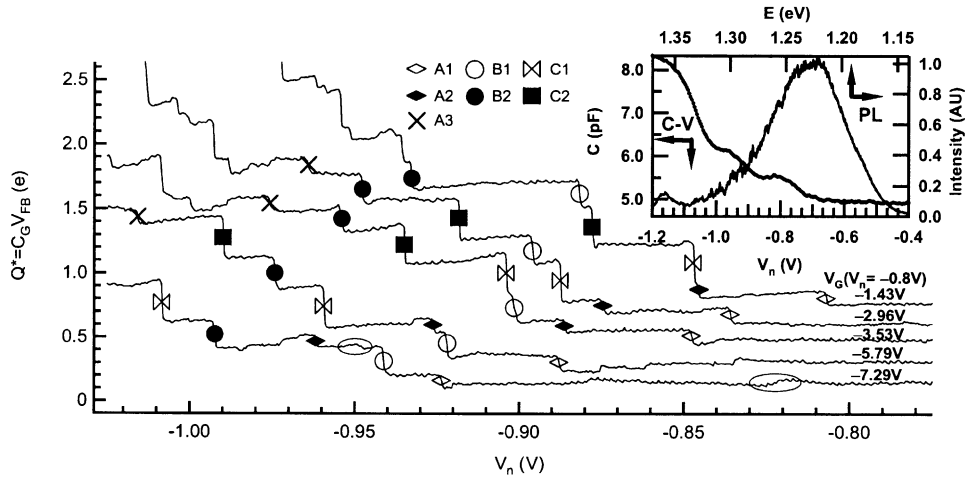


Fig. 3. $Q^*(e)$ for different gate voltage offsets, $V_{\text{off}}$, where $V_G = V_{FB} + V_{\text{off}} - V_n C_n/C_G$. Steps in $Q^*$ are marked with symbols to indicate tunneling into Dot A, B, or C, with electron number 1, 2, or 3. Inset: $C$–$V$ and photoluminesence data showing QD levels near the wetting-layer feature.

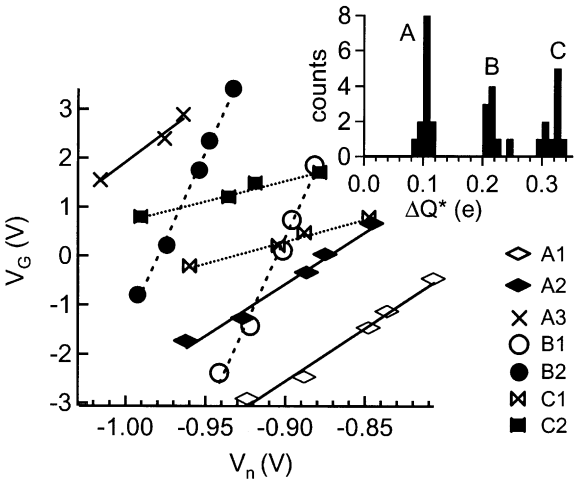


Fig. 4. Position of each feature from Fig. 3 as a function of $V_G$ and $V_n$. Inset: step heights $\Delta Q^*$ from Fig. 3.

wetting layer, $V_n \lesssim -1$ V, $Q^*$ shows dense steps. For $V_n \gtrsim -0.8$ V, we can distinguish between QD features and wetting layer features using the dependence on $V_G$ in the analysis below.

For each tunneling event marked with a symbol in Fig. 3, we record the step height $\Delta Q^*$ and the values of $V_n$ and $V_G$ at which it occurs. A histogram of $\Delta Q^*$, shown in the inset to Fig. 4, shows three step heights. We associate the three step heights with electrons tunneling onto three separate QDs, labeled A, B, and C. Two electrons are expected to tunnel into the $s$ orbital followed by a third electron in the $p$ orbital if the quantum dot is sufficiently large. In Figs. 3 and 4 we label the steps with a QD label A, B, or C followed by 1, 2 or 3, to represent tunneling of the first, second, or third electron, respectively.

For a given electron addition (i.e., a particular dot and $N$ value), Eq. (2) predicts that resonant tunneling will depend on a linear function of $V_n$ and $V_G$. This dependence is shown in Fig. 4 for each of the QD features in Fig. 3. Each feature follows a line and the lines for a particular dot are parallel but separated (e.g., Al A2, and A3) due to Coulomb and single particle energies. Thermal cycling up to 77 K reveals an equal shift for each set of curves belonging to an individual QD, which indicates that the local potential of the QD may change due to locally trapped charge, but the energy spectra E(N) capacitance ratios $C_{\text{D-n}}/C_{\text{D-}\Sigma}$ and $C_{\text{D-G}}/C_{\text{D-}\Sigma}$ remain unchanged. This confirms that the steps in Fig. 4 describe tunneling into three QDs as labeled.

By fitting Eq. (2) to the data in Fig. 4 for $N = 1$ and 2, we obtain $C_{\text{D-G}}/C_{\text{D-SET}}$, as shown in Table 1. $C_{\text{D-G}}$ is much smaller than $C_{\text{D-SET}}$; therefore all three QDs are closer to the SET than to the gate. Numerical 3D capacitance modeling of the device structure was performed to obtain estimates of capacitance

Table 1
Values obtained from linear fits in Fig. 4

| QD | $C_{\text{D-G}}/C_{\text{D-SET}}$ | $E(1)$ (eV) | $E_{\text{ss}}^{\text{C}}$ (meV) |
|---|---|---|---|
| A | 0.049 | 0.260 | 30 |
| B | 0.014 | 0.302 | 25 |
| C | 0.130 | 0.310 | 50 |

ratios which depend on the position of the QDs. The modeling indicated that dot C, with $\Delta Q^* = 0.33e$ (see inset to Fig. 4) and $C_{\text{D-G}}/C_{\text{D-SET}} = 0.13$, is centered left-to-right under the SET island and away from the ends of the island. The modeling also indicates that dot $A$, with a $\Delta Q^* = 0.10e$ and $C_{\text{D-G}}/C_{\text{D-SET}} = 0.049$, is near a tunnel junction and under one end of the SET island. Dots A and C both have $\alpha \approx \frac{1}{3}$ according to the model. Dot $B$ has a step height of $0.22e$ which is consistent with $\alpha \approx \frac{1}{3}$; however it has an unexpectedly small $C_{\text{D-G}}/C_{\text{D-SET}}$. We use $\alpha \approx \frac{1}{3}$ below to obtain the QD addition energies. The second and third columns of Table 1 show $E(1)$ and $E_{\text{ss}}^{\text{C}}$ for each QD. The Coulomb energies are larger than comparable studies on QDs [8], which is expected since our $C$–$V$ data show that these QD states are close to the wetting layer states.

Finally, using the linear fit to A3, we obtain $E(3) - E(1) = 99$ meV. We compare this value and $E_{\text{ss}}^{\text{C}} = 30$ meV from QD A to the 2D harmonic oscillator model of InGaAs quantum dots described in Ref. [9]. In this model $2E_{\text{sp}}^{\text{C}} - E_{\text{sp}}^{\text{x}} = \frac{5}{4}E_{\text{ss}}^{\text{C}}$, $\Delta\varepsilon = \hbar\omega = (\hbar/r_e)^2/m^*$ and the effective radius of the electron wave function is $r_{\text{e}} = \sqrt{\pi/2e^2}/(4\pi\varepsilon_0\varepsilon_r E_{\text{ss}}^{\text{C}})$. For QD A we find $r_e = 4.6$ nm, $\hbar\omega = 61.5$ meV and $m^* = 0.058m_{\text{e}}$. As expected, the effective mass is in rough agreement with $m^* = 0.057m_{\text{e}}$, obtained from magnetic field dispersion data using the same model [9].

We have demonstrated a new technique to study electron tunneling into individual InGaAs self-assembled QDs using an SET. We observe tunneling into QDs at a voltage comparable to that seen in large ensemble $C$–$V$ measurements. An analysis of the steps of the SET feedback signal as a function of applied voltages allows us to identify 3 QDs with different relative capacitances to the gate lead. By analyzing the voltage-dependent tunneling events the electron addition energies for 3 individual quantum dots are extracted. This research demonstrates how a device containing one or a few InGaAs QDs may benefit from a gate that controls the potential of a QD, independent of the bias voltage.

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