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High Inversion Current in Silicon Nanowire Field Effect Transistors

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ABSTRACT

Silicon nanowire (SiNW) field effect transistors (FETs) with channel widths down to 20 nm have been fabricated by a conventional "top-down" approach by using electron-beam lithography. The SiNW device shows higher inversion channel current density than the control devices. The extracted electron inversion mobility of the 20 nm width nanowire channel (≈1000 cm²/Vs) is found to be 2 times higher than that of the reference MOSFET (≈480 cm²/Vs) of large dimension ($W \geq 1$ μm). We attribute this mobility increase to strain-induced changes in the band structure of the SiNW after oxidation.

Recently, semiconductor nanowire (NW) field-effect transistors (FETs) have drawn considerable attention as building blocks for highly downscaled electronic devices with superior performance. FETs have been formed from various semiconducting NWs by both "bottom-up" (assembly) and "top-down" (lithography) approaches. For the case of the bottom-up approach, extensive effort has been devoted to single-walled carbon nanotube FETs[1] and silicon nanowire (SiNW) FETs,[2] which have shown transistor performance exceeding that of FETs fabricated in single-crystalline bulk silicon. For example, carrier mobility values of 20 000 cm^2/Vs and 1350 cm^2/Vs at room temperature have been reported for single-walled carbon nanotubes[1] and silicon SiNWs[2], respectively. In particular, the performance of SiNW FETs is potentially important for mainstream silicon technology as device dimensions approach 10 nm. However, most of the reported mobility values are not for an inversion channel but are bulk channel values in depletion-mode NW FETs. Furthermore, ohmic contact formation is hard to attain in NW structures, and the inversion layer mobility of SiNW still remains poorly understood. To investigate the transport properties of the inversion channel of SiNWs, it is highly desirable to measure NW FETs with n-p-n doping and good ohmic contacts.[3,4] In this work, the inversion channel transport properties of SiNW FETs made by using conventional semiconductor fabrication techniques have been systematically studied and compared to those of reference metal-oxide-semiconductor (MOS) FET channels. The results show that the inversion channel mobility of SiNWs is 1.3 to 2.2 times higher than that extracted from larger dimension reference devices.

The devices used in this study are n-channel SiNW FETs fabricated from a p-type silicon-on-insulator (SOI) wafer with n+ source and drain. Figure 1 shows a schematic top-view of a SiNW FET, which has a [110]-oriented channel on (001) wafer. The FETs have been fabricated by the conventional MOSFET process, where the thickness of the SiNW can be controlled to the nanometer scale.[5,6] The NW channels have been defined by electron beam lithography, and phosphorus-doped polycrystalline Si has been used as the top gate. Al has been used as metal electrodes for the source, drain, gate, and backside gate contacts.

To determine the exact dimensions of the nanowire channels, cross-sectional transmission electron microscopy (TEM) has been used. Figure 1C shows a TEM image of the cross section of the SiNW channel along the line *B-B′*. The SiNW channel is thinner ($W_{S4} \approx 12$ nm) than the center of the SOI bulk channel layer region ($W_{S1,2,3} \approx 28$ nm) because of the enhancement of oxidation near the pattern edge.[5] The gate oxide over the Si wire is approximately 40 nm thick. Figure 2A−D shows the top-view layout of the fabricated FETs with different channel geometries, and the cross-sectional view of the channel region is shown in Figure 2E. The channel width W_4 of the SiNW is 20 or 34 nm, and

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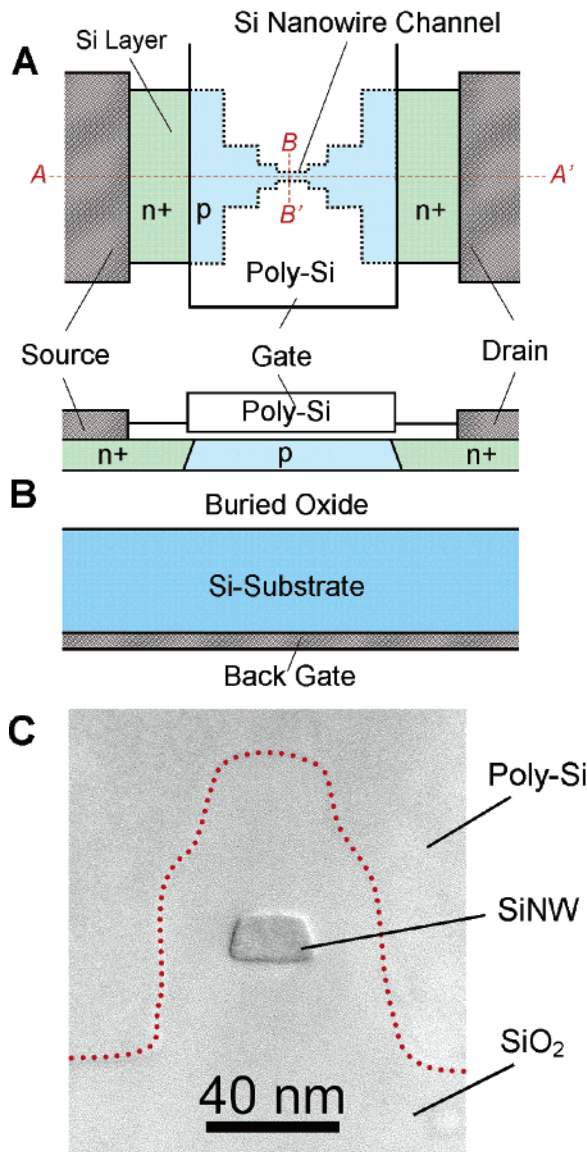

Figure 1. (A) Schematic top view of the silicon nanowire (SiNW) FET. (B) Schematic cross section of the device along line $A-A'$. (C) Transmission−electron microscopy of the cross section along line $B-B'$.

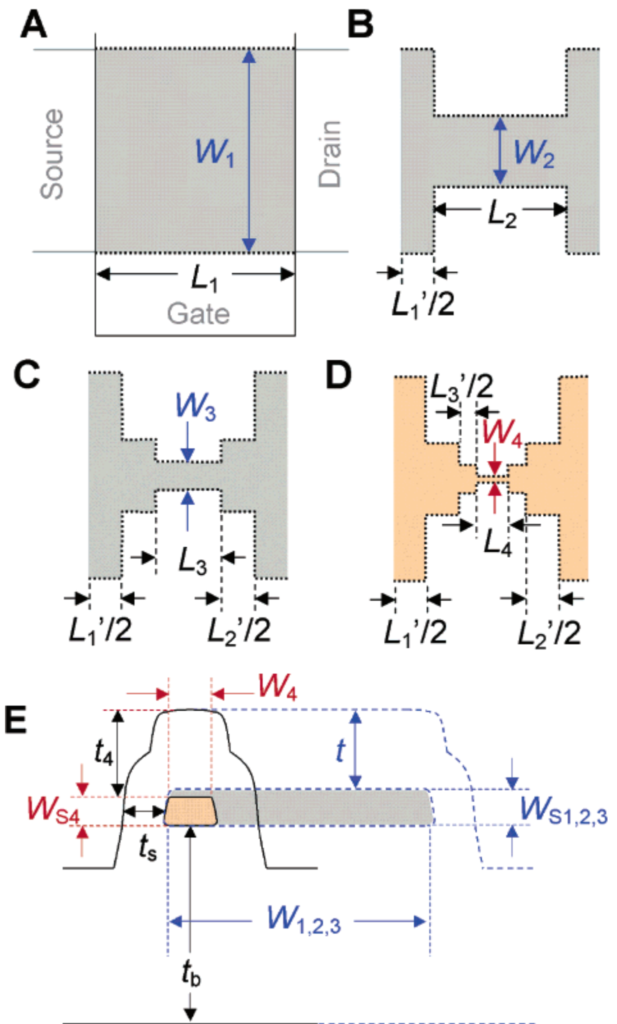

Figure 2. (A−D) Layout of the channel geometries for the different devices (E) Cross-sectional schematic of the silicon channel region. (A) $L_1 = 30$ μm, (B) $L_2 = 6$ μm, (C) $L_3 = 2.2$ μm, (D) $L_4 = 100$ nm, (E) $t_4 = 48$ nm, $t = 40$ nm, $t_S = 20$ nm, $W_{S4} = 12$ nm, $W_4 = 20$ nm.

the length L_4 is 100 nm.[7] SOI channels with various widths ($W_3 = 100$, 200, and 400 nm) are serially connected to the SiNW channel. All the devices studied in this work are basically SOI FETs with different channel geometries (see Table 1).

Figure 3 shows the measured drain current I_D as a function of gate voltage V_G for a SiNW FET and reference FETs at a drain voltage V_D of 50 mV at room temperature. From these curves the extracted subthreshold slopes $S = dV_G/d(\log(I_D))$ were about 65 mV/dec, indicating good interface properties between the oxide and Si substrate.[8] A negative back gate bias V_{BG} efficiently changes V_{th} for all the devices to the positive direction, and the double hump behavior is due to the difference in V_{th} in the edge parts of the 30 μm wide channel. On the other hand, for positive V_{BG}, the negative shift in V_{th} of the NW channel is less compared to that of the reference FETs. Since the top gate covers the SiNW not only from the top surfaces but also from the both sidewalls of the channel, the V_{BG} has less effect on the SiNW devices than on the control devices. For analyzing the mobility, V_{BG} was chosen to be 0 V in order to have the same threshold voltage for both the NW channels and the reference channels.

Figure 4 shows the measured drain current I_D at $V_G = 5$ V, as a function of the channel geometry W/L for NWFETs and reference FETs, in which the inversion channel has been formed by the top gate at $V_D = 50$ mV. The threshold voltage V_{th} was −0.1 V for both NW channels and reference channels at $V_{BG} = 0$ V. In a FET, the channel conductance g_D is proportional to W/L. Thus the total channel conductance is related in a reciprocal manner to the individual channel regions that are serially connected. The nominal W/L ratio of a transistor that has a non-rectangular channel (such as in Figure 2) can be given as

$$\frac{1}{(W/L)_{TOT}} = \frac{1}{(W_1/L_1)} + \frac{1}{(W_2/L_2)} + \cdots + \frac{1}{(W_n/L_n)} \quad (1)$$

Table 1. Summary of FETs with Different Channel Geometries[a]

device	channel width	nominal W/L	effective W/L
A	$W_1 = 30\ \mu$m	2.143	2.1×10^0
B	$W_2 = 10\ \mu$m	1.071	1.1×10^0
C1	$W_3 = 1\ \mu$m	0.343	3.6×10^{-1}
C2	$W_3 = 400$ nm	0.161	1.8×10^{-1}
C3	$W_3 = 200$ nm	0.085	1.1×10^{-1}
C4	$W_3 = 100$ nm	0.044	6.2×10^{-2}
D1	$W_4 = 34$ nm ($W_3 = 400$ nm)	0.112	1.5×10^{-1}
D2	$W_4 = 34$ nm ($W_3 = 200$ nm)	0.071	1.3×10^{-1}
D3	$W_4 = 34$ nm ($W_3 = 100$ nm)	0.041	9.5×10^{-2}
D4	$W_4 = 20$ nm ($W_3 = 400$ nm)	0.091	8.7×10^{-2}
D5	$W_4 = 20$ nm ($W_3 = 200$ nm)	0.062	5.9×10^{-2}
D6	$W_4 = 20$ nm ($W_3 = 100$ nm)	0.037	5.6×10^{-2}

[a] The nominal values are numerical calculations based on the mask dimension. The effective values have been calculated based on the top and the sidewall TEM measurements. Only 2 significant digits are shown. The uncertainty in the measurements of dimensions from TEM is on the order of ±0.5 nm or less, which leads to an uncertainty on the W/L of ±0.001 for the nominally smallest device D6.

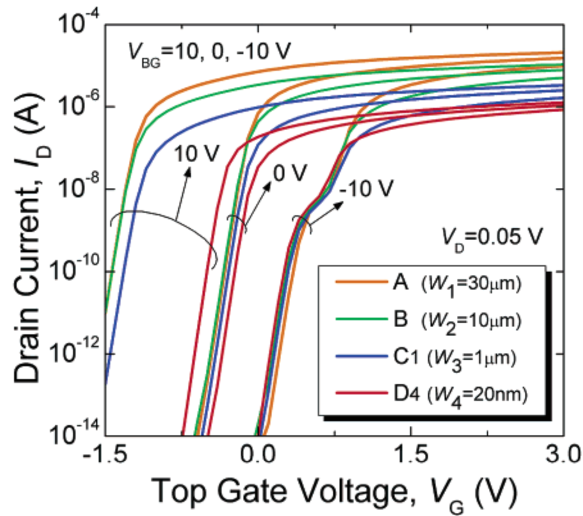

Figure 3. Drain current (I_D) versus gate voltage (V_G) characteristics of reference FETs and NW FETs.

where n is the number of different rectangular-shaped channels connected in series.

However, as the poly-silicon gate and the gate oxide fully cover both top and sidewall of the nanowire channels, the contribution from the sidewall of the channel to the effective W/L may become significant. To take this into account, we have used a modified value of effective W/L, which considers both the channel top surface and the sidewalls as the width of a SiNW channel. For example, for the channel width of W_4, the effective W/L can be obtained by substituting W_4 in eq 1 with $W_{eff,4}$, which is given by

$$W_{eff,4} = \left(\frac{W_4}{t_4} + 2\frac{W_{S4}}{t_s}\right)t \tag{2}$$

where t_s, t_4, and t are the gate oxide thicknesses on the sidewall, over the channel, and over the control device, respectively, and W_{S4} is the thickness of the SiNW channel along the sidewall. Accordingly, the effective channel width values can be obtained for other channels such as $W_{eff,1}$, $W_{eff,2}$, and $W_{eff,3}$ in each device. In eq 2, the denominators of thickness are included in order to account for the difference in the induced surface field due to the variation in the gate oxide thickness. The nominal and effective values of W/L for the FETs studied in the work are summarized in Table 1. The difference between the nominal and effective values increases for smaller W.

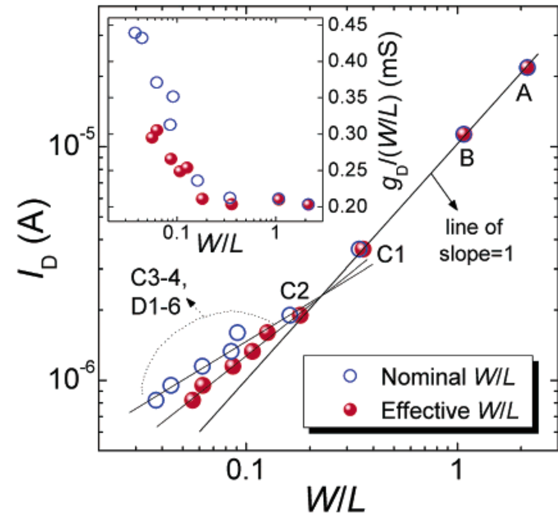

Figure 4. Measured drain current (I_{DS}) as a function of the channel geometry factor (W/L). Inset shows the conductance normalized to the geometry ($g_D/(W/L)$). Open circles show nominal values while solid circles are effective values of W/L. The dashed lines are a guide to the eyes and the slope of the line at large W/L is 1.

The measured drain current I_D of a FET is given as $I_D = \mu(W/L)Q_{inv}\cdot V_D$, where Q_{inv} is the inversion layer charge.[9] I_D should be proportional to the effective channel width and length ratio W/L for all the devices. It is, however, clearly seen in Figure 4 that the SiNW FETs with small W/L (<0.2) show higher current I_D than expected from the line extrapolated from the control FETs with large W/L (>0.2). The results imply that the channels with narrow width ($0.2 > W/L$ and thus $W < 400$ nm) have higher conductances per channel width and thus higher mobilities compared to the control channels ($W \geq 1\ \mu$m). To investigate the high inversion conductance in SiNW FETs, we extracted the mobilities for different channel widths in the following way. The effective mobility for each device was calculated by using $\mu = g_D/[(W/L)Q_{inv}]$. For sufficiently large V_G, Q_{inv} is given by $Q_{inv} = C_{ox}(V_G - V_{th})$, where V_{th} and C_{ox} are the threshold voltage and the gate capacitance, respectively. C_{ox} has been estimated by using the gate oxide thicknesses measured from TEM for both the top and the sidewall of each device. C_{ox} values for device A that were separately measured by a capacitance−voltage ($C-V$) technique confirmed that the calculated capacitance values are reasonable. As the conductance of a serial connection adds inversely, the conductance for device A (g_A) can be used for calculating the conductance for the channel W_2 (g_{W2})

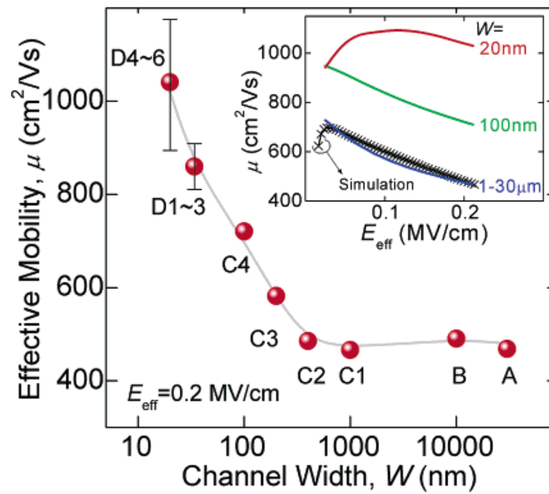

Figure 5. Estimated mobility values for different channel widths (W). Inset shows the extracted mobility for different channels as a function of vertical effective field (E_{eff}). Each error bar for the D-devices represents the standard deviation of 6 different data points, while the data for A-, B-, and C-devices are the average of two. The effective field E_{eff} in the inset has been derived by using $t = 48$ nm for all devices. Note that since E_{eff} is almost proportional to Q_{inv}, and to $1/t_{ox}$, E_{eff} at the sidewall is larger than that at the top by the factor t_4/t_S (48 nm/20 nm) for SiNW at a certain gate voltage, which, however, does not change the general behavior of the plot.

in device B as

$$\frac{1}{g_B} = \frac{1}{g_{W1}} + \frac{1}{g_{W2}} = \frac{1}{g_A(L_1/L_1')} + \frac{1}{g_{W2}} \quad (3)$$

where g_B and g_{W1} are the conductances for device B and for channel W_1 in Figure 2, respectively, and L_1 and L_1' are lengths for W_1 in devices A and B, respectively. In the same way, the conductance for the different channel widths of W_3 and W_4 in Figure 2 can be determined, and therefore the mobility values for each channel width can be extracted as well. Note that it is assumed that the conductivity is uniform in each channel of the same channel width. The electron mobility values that were extracted as a function of channel widths at an effective vertical field[10] E_{eff} of 0.2 MV/cm are shown in Figure 5. The inset in Figure 5 shows the effective mobility versus E_{eff} curves for different channels. The theoretical calculation for the control device[9] follows the slope of the measurements, which provides further indication that the mobility extraction is correct. As the channel width decreases, the inversion layer mobility of the SiNW increases up to approximately twice the mobility (≈1000 cm^2/Vs) of the larger channel-width control FETs (≈480 cm^2/Vs for W >1 μm). Note that there exist uncertainties in the determination of the capacitance in the channel, and the precise calculated values of μ may vary slightly depending on the assumptions. However, they should not influence the relative comparison of the mobility values among the samples. Although the charge−voltage relationship in the SiNW is not clearly understood, the observed enhancement may be attributed to strain in the SiNW after the oxidation process. It has been reported in previous work[11−13] that large mechanical stress is induced in the oxide during the oxidation process to form the SiNW, which consequently affects the electronic states of the SiNW. For example, the band gap is known to decrease by about 130 meV with a 1% oxidation-induced strain.[14−16] The strain can induce an energy splitting between the 2-fold and 4-fold valley associated with the crystal asymmetry of Si and suppress inter-valley phonon scattering, which can cause mobility enhancement of the strained Si channel.[17,18] For example, a typical value of peak electron mobility in a strained Si/$Si_{1-x}G_x$ FET can be as high as 1010 cm^2/Vs,[19] and up to 2.4 times enhancement over control Si FETs has also been reported.[20] While additional studies are required for further understanding of the mobility enhancement mechanism in SiNW, the results demonstrate that SiNW FETs fabricated by a standard top-down approach exhibit substantially enhanced transport performance similar to that observed by Cui et al. in CVD-grown SiNWs.[2]

In summary, the inversion electron transport properties of SiNW with different channel geometries have been systematically studied by considering wider SOI channels in reference MOSFETs. The extracted average inversion channel mobility of a 20 nm-width nanowire channel was found to be approximately twice as large as that of the reference MOSFETs. The enhancement is attributed to the possible suppression of inter-valley phonon scattering due to strain in SiNW caused by the oxidation process. The results suggest that SiNW FETs, which are compatible with Si ULSI technology, can bring about significant performance benefits in nanoscale electronics.

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References

(1) (a) Tans, S. J.; Verschueren, R. M.; Dekker, C. *Nature* **1998**, *393*, 49−52. (b) Durkop, T.; Brintlinger, T.; Fuhrer, M. S. *AIP Conf. Proc.* **2002**, *633*, 242−246.
(2) Cui, Y.; Zhong, Z.; Wang, D.; Wang, W.; Lieber, C. M. *Nano Lett.* **2003**, *3*, 149−152.
(3) Martel, R.; Derycke, V.; Lavoie, C.; Appenzeller, J.; Chan, K. K.; Tersoff, J.; Avouris, Ph. *Phys. Rev. Lett.* **2001**, *87*, 256805/1−4.
(4) Nakanishi, T.; Bachtold, A.; Dekker, C. *Phys. Rev. B*, **2002**, *66*, 073307/1−4.
(5) (a) Fujiwara, A.; Takahashi, Y.; Namatsu, H.; Kurihara, K.; Murase, K. *Jpn. J. Appl. Phys.* **1998**, *37*, 3257−3263. (b) Takahashi, Y.; Ono, Y.; Fujiwara, A.; Inokawa, H.; *J. Phys.: Condens. Matter* **2002**, *14*, R995−R1033.
(6) Fujiwara, A.; Horigushi, S.; Nagase, M.; Takahashi, Y. *Jpn. J. Appl. Phys.* **2003**, *42*, 2429−2433.
(7) Nagase, M.; Fujiwara, A.; Kurihara, K.; Namatsu, H. *Jpn. J. Appl. Phys.* **2003**, *42*, 318−325.
(8) Fossum, J. G.; Yang J.-W.; Trivedi V. P. *IEEE Electron Device Lett.* **2003**, *12*, 745−747.
(9) Hauser, J. R. *IEEE Trans. Electron Devices* **1996**, *43*, 1981−1988.

(10) Sherony, M. J.; Su, L. T.; Chung, J. E.; Antoniadis, D. A. *IEEE Trans. Electron Devices* **1994**, *41*, 276−278.
(11) Liu, H. I.; Maluf, N. I.; Pease, R. F. W.; Biegelsen, D. K.; Johnson N. M.; Ponce, F. A. *J. Vac. Sci. Technol. B* **1992**, *10*, 2846−2850.
(12) Liu, H. I.; Biegelsen, D. K.; Johnson, N. M.; Ponce, F. A.; Pease R. F. W. *J. Vac. Sci. Technol. B* **1993**, *11*, 2532−2537.
(13) Liu, H. I.; Biegelsen, D. K.; Ponce, F. A.; Johnson, N. M.; Pease R. F. W. *Appl. Phys. Lett.* **1994**, *64*, 1383−1385.
(14) Horiguchi, S.; Nagase, M.; Shiraishi K.; Kageshima, H. *Jpn. J. Appl. Phys.* **2001**, *40*, L29−L32.
(15) Shiraishi, K.; Nagase, M.; Horiguchi S.; Kageshima H. *Mater. Res. Soc., Symp. Proc.* **1999**, *586*, 533−538.
(16) Shiraishi, K.; Nagase, M.; Horiguchi S.; Kageshima H.; Uematsu, M.; Takahashi, Y.; Murase K. *Phys. E* **2000**, *7*, 337−341.
(17) Hoyt, J. L.; Nayfeh, H. M.; Eguchi, S.; Aberg, I.; Xia, G.; Drake, T.; Fitzgerald, E. A.; Antoniadis, D. A. *IEDM Technol. Digest* **2002**, 23−26.
(18) Takagi, S.; Koga, J.; Toriumi, A. *Jpn. J. Appl. Phys.* **1998**, *37*, 1289−1294.
(19) Wesler, J.; Hoyt, J. L.; Gibbons, J. F. *IEEE Electron Device Lett.* **1994**, *15*, 100−102.
(20) Rim, K.; Chan, K.; Shi, L.; Boyd, D.; Ott, J.; Klymko, N.; Cardone, F.; Tai, L.; Koester, S.; Cobb, M.; Canaperi, D.; To, B.; Duch, E.; Babich, I.; Carruthers, R.; Saunders: P.; Walker, G.; Zhang, Y.; Steen, M.; Ieong, M. *IEDM Technol. Digest* **2003**, 3.1.1−3.1.4.

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