2.6-V High-Resolution Programmable Josephson Voltage Standard Circuits Using Double-Stacked $MoSi_2$-Barrier Junctions

Yonuk Chong, C.harles J. Burroughs, Jr, Paul. D. Dresselhaus, Nicolas Hadacek, Hirotake Yamamori, and Samuel P. Benz, *Senior Member, IEEE*

***Abstract*—Using a new circuit design and double-stacked junction technology we have demonstrated fully functional high-resolution programmable voltage standard chips with 67 410 junctions that operate up to a maximum output voltage of 2.6 V. The circuit uses double-stacked junctions, where two junctions are fabricated in each stack, in order to increase the output voltage. We have also improved the voltage resolution at fixed frequencies 16-fold by using a circuit optimized for three voltage states and 128-fold below 2 V by oppositely biasing two large arrays whose junction counts differ by a single stack. These circuits operate over a frequency range from 14 GHz to 19 GHz with a 2-mA maximum operating current range.**

***Index Terms*—Josephson arrays, quantization, standards, superconductor-normal-superconductor (SNS).**

I. Introduction

SUPERCONDUCTOR-normal-superconductor (SNS) Josephson junctions have been successfully used in programmable Josephson voltage standards (PJVS) [1]–[3] and in the Josephson arbitrary waveform synthesizer [4]. Other junction types have been employed that have produced larger voltages but with smaller current ranges [5], [6]. Series arrays of junctions are required to increase the output voltage to practical levels. We also wish to increase the linear junction density in these arrays in order to provide higher output voltage, better operating margins in programmable systems, and better broadband frequency response for ac voltage standards [7]. At the National Institute of Standards and Technology (NIST), we have found that $MoSi_2$ provides a stable, reproducible, dry-etchable, normal-metal barrier for stacked junctions [8]. This reproducibility enables precise targeting of the critical-current density and the characteristic voltage $V_c = I_cR$, where I_c is the critical current and R is the normal resistance. Furthermore, the high resistivity of $MoSi_2$ allows physically larger junctions at a given characteristic voltage. One advantage of larger junction area is that, for a given degree of etch anisotropy the critical current uniformity is higher, which is very important for maintaining uniformity in stacked arrays.

Manuscript received July 2, 2004; revised November 2, 2004.

Y. Chong, C. J. Burroughs, P. D. Dresselhaus, N. Hadacek, H. Yamamori, and S. P. Benz are with the National Institute of Standards and Technology (NIST), Boulder, CO 80305 USA (e-mail: benz@boulder.nist.gov).

H. Yamamori is with the National Institute of Advanced Industrial Science and Technology (AIST), Japan.

Digital Object Identifier 10.1109/TIM.2004.843080

In order to increase junction density, we wish to vertically stack as many junctions as possible. In previous work, we found that the dc electrical characteristics of the junctions do not begin to change significantly until the thickness of the middle superconducting electrode between the normal-metal barriers is decreased below 20 nm [9]. We have also previously investigated and optimized the thermal properties of these $MoSi_2$-barrier stacks [10]. In this paper, we demonstrate arrays of $MoSi_2$-barrier junctions of sufficient uniformity that precision voltages are produced in programmable voltage standard circuits at double the previous voltage of our nonstacked, single-junction circuits. In addition to the double-stacked junctions, we also present a new high-resolution circuit that uses a trinary design to increase the voltage resolution.

II. High-Resolution Circuit Design

In all of our previous PJVS circuits we used a binary-logic design in which a 32 768-junction series-connected array was divided into smaller array cells in a binary sequence [1], [11], [12]. Binary logic was used because we typically used only two states of the junctions, the $n = \pm 1$ constant-voltage steps. However, for many years we have microwave-biased these circuits such that the $n = 0$ step is quite large. Thus, we have actually been using three different voltage states for our programmable circuits.

Recently, we redesigned the array cells in order to improve the performance of our circuits and to address a need for higher voltage resolution in existing programmable systems.[1] We chose a trinary-logic design in order to take full advantage of the three usable voltage levels. This allows us to dramatically increase the voltage resolution of our circuits, while keeping the same number of array cells and bias leads (and, thus, the same probes and bias electronics) that we use for the existing binary-array circuits in our systems.

Previous single-junction, nonstacked, binary-logic circuits with 1.1-V maximum output voltage have 4-mV resolution for the same number of bias leads because the smallest array cell has 128 junctions. In our new design, a *single* junction or a single stack defines the smallest voltage increment, depending on the number of junctions in the stack. For the double-stacked arrays in this paper the voltage resolution is 76 μV when biased at 18.5 GHz. Although finer voltage resolution may be

[1]NIST uses PJVS systems in both the primary voltage calibration laboratory and in the watt-balance experiment in Gaithersburg, MD.

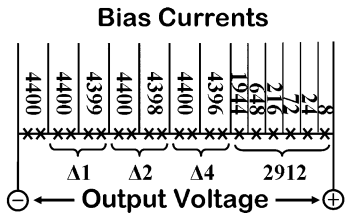

Fig. 1. High-resolution PJVS array sequence showing the number of *stacks* in each of the 13 array cells. The smallest 6 cells are divided in a trinary sequence. Pairs of the largest cells can be combined in opposition to produce the smallest voltage increments based on 1, 2, or 4 total stacks. Note that there are *twice* as many junctions as stacks for the double-junction stacks presented in this paper.

TABLE I
ARRAY CELL CHARACTERISTICS FOR TRINARY-LOGIC HIGH-RESOLUTION CIRCUIT. THERE ARE TWO JUNCTIONS IN EACH STACK

Cell Number	Number of JJs	Critical Current (mA)	Zero Step Range (mA)	±First Step Range (mA)
1	8800	10.96	8.62	2.28
2	8800	10.96	7.44	2.01
3	8798	11.04	8.40	1.96
4	8800	11.04	8.10	2.03
5	8796	11.04	8.64	2.05
6	8800	11.12	7.38	2.21
7	8792	10.96	8.42	2.06
8	3888	11.04	8.86	2.17
9	1296	11.12	9.26	2.07
10	16	11.04	11.39	2.82
11	48	11.16	11.75	2.44
12	144	11.28	11.44	2.76
13	432	11.20	11.60	2.55

achieved in either circuit by fine-tuning the bias frequency, this is not always practical if the circuit has a narrow-frequency microwave response. The trinary weighting allows a simple, more-robust method of increasing the voltage resolution.

Similar to the previous 1-V programmable circuits, the new high-resolution circuit is a large array divided into 13 series-connected cells as shown in Fig. 1 and Table I. However, we have increased the total number of junctions to 67410 by doubling the junctions in each stack and by adding a few additional stacks to each cell. Eight large arrays are microwave-biased in parallel using both off-chip and on-chip splitters. Due to microwave attenuation, only about 8800 junctions can be placed in one array while still achieving uniform microwave bias. Seven of these largest arrays each have about 8800 junctions. The eighth large array contains 5824 junctions and is further divided in a trinary fashion into smaller cells, decreasing threefold for each cell beginning with 3888 junctions and ending with 16 junctions, as shown for cells 8–13 in Table I. Fine resolution is achieved by decreasing the total number of junctions in three of the large cells (cells 3, 5, and 7) so they differ by 2, 4, and 8 junctions from the nominal 8800 total junctions. Fine-resolution voltages defined by these few junctions are achieved by biasing one of these arrays on a nonzero voltage step while simultaneously biasing one of the 8800-junction arrays at the opposite voltage. Because two large arrays in opposition ($1/4$ of all the junctions) produce the fine resolution, this feature can be used only for voltages less than three-quarters of the maximum voltage.

This trinary scheme, coupled with fine resolution from opposite-biased large arrays, provides an efficient design for achieving high resolution within the bias-constraints of our present system. Although we have described the design for double-stacked junctions, the high-resolution circuit works equally well for nonstacked arrays or arrays with taller stacks. For nonstacked arrays, the finest voltage resolution would be the voltage of a single junction instead of the voltage of a single stack.

III. DOUBLE-JUNCTION FABRICATION

The total output voltage of the programmable circuit is doubled compared to our typical 1-V PJVS circuit [1] by using double-stacked $MoSi_2$-barrier junctions [8], [9]. The fabrication process includes electrodes and wiring of superconducting niobium, insulating layers of silicon dioxide, and resistors and contact pads of palladium-gold. The film thicknesses are: 420-nm Nb base electrode, two 22-nm $MoSi_2$ barriers separated by a 50-nm thick Nb middle electrode, 220-nm Nb counter electrode, 300-nm SiO_2, 660-nm Nb wiring, and 130-nm PdAu. The metals were dc sputtered and the oxide was deposited by use of an electron-cyclotron-resonance chemical-vapor-deposition system with backside helium-gas cooling. The vias and wiring were patterned with CHF_3 and SF_6 reactive-ion etching, while the vertical walls of the stacks were patterned in a deep reactive-ion etcher by use of a mixture of etch and passivation gasses.

IV. MEASURED RESULTS

The characteristic voltage for this array was chosen to be 48 μV. We chose a value much larger than the typical 32 μV, because previous $MoSi_2$ circuits with higher I_cR showed better performance, such as larger current range for the steps. We can accurately tune the characteristic voltage of our junctions to within 1 μV by setting the barrier thickness.

The critical currents for the 4 μm $\times$ 8 μm junctions were about 11 mA. Table I summarizes the electrical characteristics of the different cells, including the critical current with no microwave bias applied as well as the current ranges of the zeroth and first constant-voltage steps while biased at 18.5 GHz. The current range represents the bias limits over which the step is at the correct voltage (both positive and negative currents for the zero step) with a 1 μV voltage threshold on the digital voltmeter's 1-V scale. Note that the power was not adjusted to independently maximize the range of individual cells. Instead, the microwave power applied to the chip was increased until the simultaneous current range of every step was approximately 2 mA. The microwave power applied to the SMA connector on our 4 K cryopackage was 50 mW [1].

Current-voltage *IV* characteristics are shown in Fig. 2 for all 13 cells biased at 18.5 GHz. As for the data in Table I, the microwave power was increased to generate a 2-mA minimum current range on the first step of each array cell. The *IV* curve near each cell's first step is shown by plotting the voltage on a log scale. The first six *IV* curves with the lowest voltage are for the smaller arrays and show that the voltage increases by exactly threefold for each consecutively larger cell. The *IV* curves of

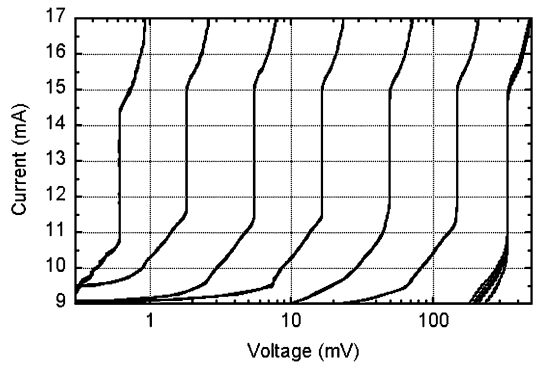

Fig. 2. Current-voltage *IV* characteristics for all 13 array cells from the high-resolution PJVS circuit using $MoSi_2$ double-stacked junction arrays. All *IV*s were measured with the same power at 18.5 GHz. The multiple *IV*'s with the largest voltage step correspond to the seven largest arrays with about 8800 junctions each, while the smallest step is for the cell with only 16 junctions.

the seven largest arrays overlap quite well, indicating good uniformity of both the junction characteristics across the chip and the microwave power distribution to the arrays at this frequency. Note that the current range of each cell appears to be about 4 mA on this coarse voltage scale, whereas the precision voltage measurements shown in Table I demonstrate that the steps are truly flat over only a smaller 2-mA current range. Nevertheless, the *IV* curves in Fig. 2 show the voltage programmability of the cells and provide a coarse measurement of the array uniformity.

A good method to determine full functionality for the chip with a high-resolution measurement is to bias half of the junctions on the positive step and the other half on the negative step. This generates a small combined voltage so that operating margins for the entire circuit can be determined with high resolution on a lower range of the voltmeter. In Fig. 3, we show this measurement for one of the chips where the first four cells with 35198 junctions are biased on the positive step and the remaining 32 208 junctions are biased on the negative step. (Four junctions were missing from cell 8 due to a niobium wiring short.) The resulting difference voltage is around 114 mV ($+1.342\,858$ V $- 1.228\,785$ V $= 0.114\,073$ V), allowing measurement on the 100 mV range of a digital voltmeter. The cell bias currents range from 12.9 mA to 13.5 mA. Fig. 3, therefore, shows the resulting current range when all cells are biased at the center of a nonzero voltage step, a stringent test of the operating margins.

We show in Fig. 3 the measured current-voltage characteristic of the entire circuit in operation. The combined voltage step for all 13 arrays is flat over a total operating current range of nearly 2 mA, within the 40 nV noise of the measurement. The voltage is offset from zero at 114.073 mV as expected for the 2990 net positively biased junctions. The small 150 nV deviation from the expected value is primarily due to a -1.5 μV/V gain error in the digital voltmeter, combined with a small thermal voltage contribution. In previous experiments, we reduced the thermal voltages by using copper-block connectors in a thermally isolated box [11].

For all data presented so far in this paper, the circuit was biased at a single frequency, 18.5 GHz, where the arrays produce the largest operating current range. We have also characterized

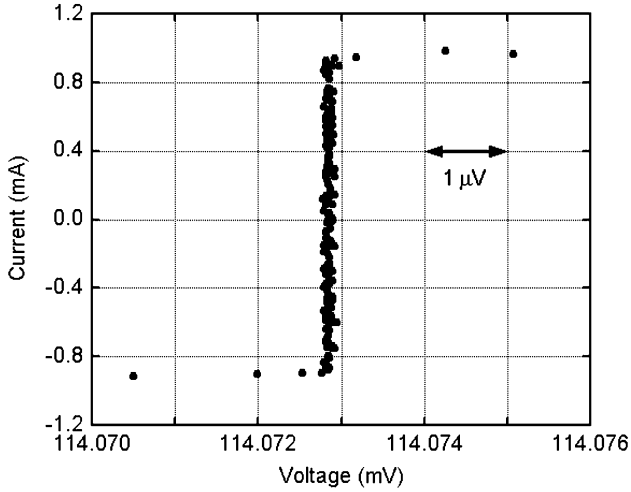

Fig. 3. High-resolution step flatness measurement showing a current range of about 2 mA measured on the 100 mV scale of a digital voltmeter. About half of the junctions (35198 JJ's) were biased on the positive voltage step and the other half (32208 JJ's) were biased on the negative voltage step, producing a smaller voltage ($+1.342\,858$ V $- 1.228\,785$ V $= 0.114\,073$ V) that can be measured with high resolution.

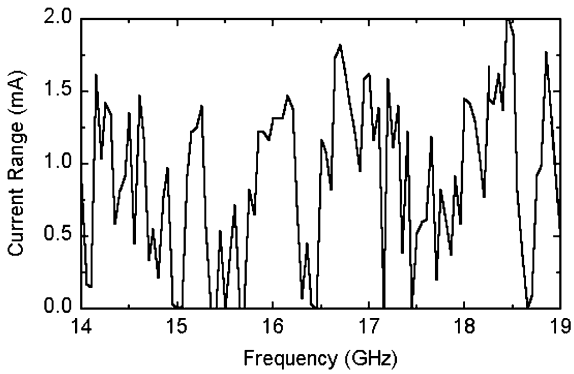

Fig. 4. Frequency dependence of the operating current range over which all junctions on the high-resolution chip produce a flat step. The power is adjusted at each frequency to maximize the current range for the entire circuit.

the circuit at other frequencies, including the 16 GHz design frequency. The design frequency is determined by the center frequency of the on-chip quarter-wave filters and impedance transformers [1]. Nevertheless, the filters are reasonably broadband and allow the bias taps to behave as high impedances to the coplanar waveguide transmission line over a frequency range of a few gigahertz [13]. Using our automated test system, we adjusted the power at each frequency to maximize the current range for all the cells. The cell with the smallest current range determines the operating current range for the entire chip. Fig. 4 plots this operating current range over a frequency range from 14 GHz to 19 GHz, which is a few gigahertz on either side of the 16 GHz design frequency.

The circuit demonstrated useful operating margins greater than 1 mA at many frequencies over this band. As can be seen from Fig. 4, useful operating ranges for all cells did not exist at all frequencies. Current range data from individual cells (not shown) helps explain the zero-range features in this figure. The zero current range around 18.7 GHz is common for all cells, suggesting that insufficient microwave power arrives at the cells.

The remaining zero-range features result from individual cells having zero current range. For example, the nearly zero current range near 14.2 GHz is caused by the small margins of cell 1, while the zero range near 15 GHz is caused by cell 6.

Even though the $MoSi_2$ arrays are quite uniform, we observe strongly varying frequency dependence of the operating margins for the entire chip. This is probably caused by nonuniform distribution of microwave power within the on-chip superconducting microwave integrated circuit as well as the off-chip splitters and microwave launches. Since this is the first detailed measurement of operating margins as a function of frequency, more measurements with other circuits are required to interpret this unexpected behavior. This plot also shows the difficulty in using frequency to tune the output voltage over wide ranges. Nevertheless, fine-tuning over a small frequency band is easy and straightforward, particularly around the 16 GHz design frequency.

At both the highest and lowest frequencies tested, our amplifier had insufficient microwave power to drive the arrays. For future measurements we plan to use a higher-power amplifier with a higher frequency range. This may allow the observation of larger margins at 18 GHz as well as margins above 19 GHz, where the frequency more closely matches the 24 GHz characteristic frequency of the junctions. At these higher frequencies the current range of the constant voltage steps should be larger and, thus, produce larger operating current ranges for every cell. In future circuit designs, we may also increase the microwave design frequency to 20 GHz, where the $MoSi_2$ junctions appear to work well.

V. Conclusion

These results show that double-stacked SNS junctions can produce precision output voltages with large (greater than 1 mA) operating current range. We are optimistic that circuits using even taller stacks can provide even higher voltages for SNS programmable voltage standard circuits. If we can demonstrate PJVS circuits with 10-V output while still maintaining a large operating current range, the PJVS system design could be greatly simplified. This would make it possible to produce a practical quantum voltage standard reference that is a turn-key system that would not require an expert operator or computer-controlled optimization.

References

[1] S. P. Benz, C. A. Hamilton, C. J. Burroughs, T. E. Harvey, and L. A. Christian, "Stable 1-volt programmable voltage standard," *Appl. Phys. Lett.*, vol. 71, pp. 1866–1868, Sep. 1997.

[2] R. Pöpel, D. Hagedorn, T. Weimann, F.-I. Buchholz, and J. Niemeyer, "Superconductor-normal metal-superconductor process development for the fabrication of small Josephson junctions in ramp-type configuration," *Supercond. Sci. Technol.*, vol. 13, pp. 148–153, 2000.

[3] H. Yamamori, M. Itoh, H. Sasaki, A. Shoji, S. P. Benz, and P. D. Dresselhaus, "All-NbN digital-to-analog converters for a programmable voltage standard," *Supercond. Sci. Technol.*, vol. 14, pp. 1048–1051, Nov. 2001.

[4] S. P. Benz, C. J. Burroughs, and P. D. Dresselhaus, "AC coupling technique for Josephson waveform synthesis," *IEEE Trans. Appl. Supercond.*, vol. 11, no. 2, pp. 612–616, Jun. 2001.

[5] J. Kohlmann, H. Schulze, R. Behr, F. Müller, and J. Niemeyer, "10 V SINIS Josephson junction series arrays for programmable voltage standards," *IEEE Trans. Instrum. Meas.*, vol. 50, no. 2, pp. 192–194, Apr. 2001.

[6] J. Hassel, H. Seppa, L. Gronberg, and I. Suni, "Optimization of a Josephson voltage array based on frequency dependently damped superconductor-insulator-superconductor junctions," *Rev. Sci. Instrum.*, vol. 74, pp. 3510–3515, Jul. 2003.

[7] S. P. Benz, P. D. Dresselhaus, and C. J. Burroughs, "Nanotechnology for next generation Josephson voltage standards," *IEEE Trans. Instrum. Meas.*, vol. 50, no. 6, pp. 1513–1518, Dec. 2001.

[8] P. D. Dresselhaus, Y. Chong, J. H. Plantenberg, and S. P. Benz, "Stacked SNS Josephson junction arrays for quantum voltage standards," *IEEE Trans. Appl. Supercond.*, vol. 13, no. 2, pp. 930–933, Jun. 2003.

[9] Y. Chong, P. D. Dresselhaus, S. P. Benz, and J. E. Bonevich, "Effects of interlayer electrode thickness in $Nb(MoSi_2/Nb)_N$ stacked Josephson junctions," *Appl. Phys. Lett.*, vol. 82, pp. 2467–2469, Apr. 2003.

[10] Y. Chong, P. D. Dresselhaus, and S. P. Benz, "Thermal transport in stacked superconductor-normal metal-superconductor Josephson junctions," *Appl. Phys. Lett.*, vol. 83, pp. 1794–1796, Sep. 2003.

[11] C. J. Burroughs, S. P. Benz, C. A. Hamilton, and T. E. Harvey, "1 volt dc programmable voltage standard system," *IEEE Trans. Appl. Supercond.*, vol. 9, no. 2, pp. 4145–4149, Jun. 1999.

[12] Y. Chong, C. J. Burroughs, P. D. Dresselhaus, N. Hadacek, H. Yamamori, and S. P. Benz, "Double-stacked $MoSi_2$-barrier junctions for programmable Josephson voltage standards," in *Proc. CPEM Conf. Dig.*, Jun.–Jul. 2004, pp. 6–7.

[13] S. P. Benz and C. J. Burroughs, "Constant-voltage steps in arrays of Nb-PdAu-Nb Josephson junctions," *IEEE Trans. Appl. Supercond.*, vol. 7, no. 2, pp. 2434–2436, Jun. 1997.