

## Flat-Spot Measurements for an AC Josephson Voltage Standard

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### Abstract

Recent advances in circuit design and fabrication of superconducting integrated circuits have enabled us to demonstrate for the first time an ac Josephson voltage standard (ACJVS) that generates both ac and dc waveforms up to 242 mV peak voltage. Using a FFT (fast Fourier transform) spectrum analyzer and an ac/dc transfer standard, we characterize ACJVS operating margins by performing “flat-spot” measurements at the level of a part in  $10^6$  for all eight bias parameters.

### Introduction

For a number of years, NIST has been developing a Josephson arbitrary waveform synthesizer and utilizing this technology to create an ACJVS system. This system can generate a variety of precision voltage waveforms, including single-tone ac sinewaves and dc voltages so that it can be used as a quantum-based voltage source for ac metrology. The present system uses a chip with two Josephson arrays (8200 junctions total) and digital-to-analog conversion using delta-sigma modulation [1], where a digital data stream at 10 Gbit/s is combined with a 15 GHz sinusoidal drive signal for a maximum bipolar pulse-repetition frequency of  $1.5 \times 10^{10}$  pulses/s. This combined signal is fed to the Josephson junctions, which precisely quantize the pulses, thus producing a nearly ideal delta-sigma pulse train and a precisely known output waveform. The unprecedented accuracy of this technique for generating ac and dc waveforms for voltage metrology has been discussed previously [2, 3].

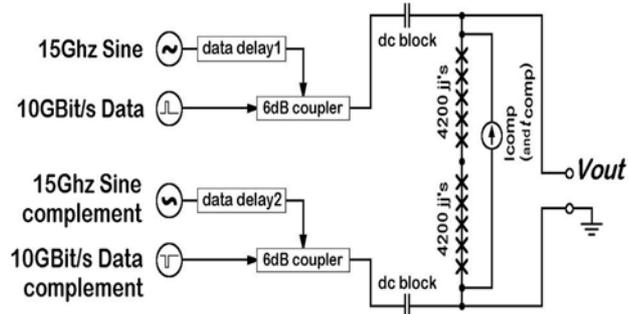


Figure 1. Diagram of the ACJVS dual-array system configuration consisting of eight adjustable bias parameters.

The latest dual-array ACJVS chips produce voltages up to 242 mV (zero-to-peak) for ac waveforms, and  $\pm 254$  mV for dc voltages. Figure 1 shows the bias configuration for the chip, where the broadband digital pulse drive to each array is split into a high-frequency component (10 MHz to 30 GHz) and a low-frequency component (dc to 10 MHz). These separated signals are delivered independently to the arrays by use of 10 MHz high-pass filters on both digital drive signal lines that transmit only the high-frequency component, and a separate sinusoidal current at the fundamental frequency applied to the arrays. The two arrays are connected in series on-chip so their low-frequency output voltages

add. This configuration allows either end of the dual-array circuit to be connected directly to ground, an essential feature for connecting the ACJVS output to spectrum analyzers, ac/dc transfer standards, thermal voltage converters (TVC), and other ac and dc voltage metrology instruments. A number of circuit innovations on the chip make this configuration possible, and those details have been presented elsewhere [4].

The eight independent bias parameters in Fig. 1 must all be set correctly for the ACJVS to produce the correct output voltage. There are two 10 Gbit/s digital data amplitudes (one for each array), two 15 GHz sinusoidal drive amplitudes (one for each array), and two data delays that shift the phase between the microwave sinusoidal drives and the digital data signals. The compensation current  $I_{\text{comp}}$  provides the low-frequency bias at the fundamental frequency. Compensation delay,  $t_{\text{comp}}$ , is the adjustment of the phase of  $I_{\text{comp}}$  with respect to the digital data signals.

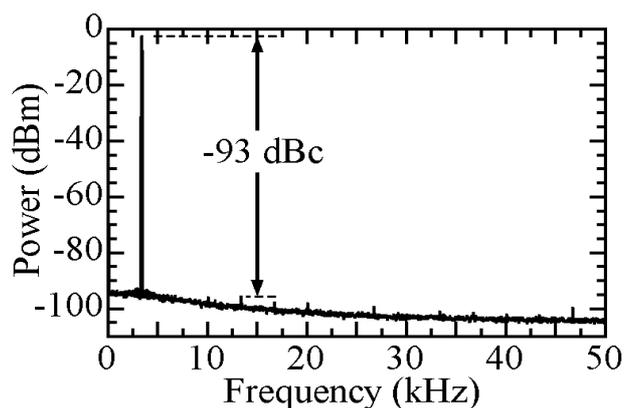


Figure 2. Spectrum analyzer measurement demonstrating  $-93$  dBc low distortion of the ACJVS with two Josephson arrays generating a 242 mV (zero-to-peak) sinewave at 3.3 kHz using 8200 junctions at 10 Gbit/s. The spectrum measurement used 100 Hz resolution bandwidth and 100 averages.

### Operating Margin Measurements

We use the term “operating margins” to designate the region in the 8-bias parameter space where each junction in each array is generating precisely one quantized pulse for every input pulse. To determine the midpoint and range for each of these bias parameters, we use a spectrum analyzer to examine the synthesized waveforms in the frequency domain and tune the biases by observing the fundamental and minimizing the first few harmonics. If any of the junctions are not within their operating margins, distortion harmonics will appear and the precision amplitude of the fundamental may be compromised. Figure 2 shows a measured spectrum of the ACJVS after the operating margins have been optimized. Notice that the largest distortion harmonic is  $-93$  dBc (i.e., 93 dB below the fundamental tone). At that level, the effect of such a harmonic on the total rms voltage output is negligible ( $<1$  nV/V) because it combines as a root-sum-squares (RSS) contribution.

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### Precision “Flat-Spot” Measurements

In order for the ACJVS system to meet the definition of an “intrinsic” ac and dc standard, its output must be independent of every parameter except the digital code, the clock frequency, and the number of junctions in the array. In other words, there must be a finite range for each bias parameter over which the output voltage does not measurably change [3]. This flat spot in the operating margins needs to be confirmed every time the ACJVS system is used for precision measurements. Spectrum analyzers are not well suited for this task because they have limited ability to detect tiny error signals occurring at the fundamental frequency. For full characterization of the ACJVS we need to be able to verify that a flat spot exists with respect to in-phase error sources at the fundamental, because they will add directly to the output rms value (not as an RSS contribution as in the case of distortion harmonics) [5]. For example, a very small distortion or error signal of -100 dBc in the ACJVS output *at the fundamental* (with a relative phase of 0° or 180°) would be undetected by the spectrum analyzer, but would still produce an error in the rms voltage of 10 parts in 10<sup>6</sup>. Thus, in order to perform the final high-precision ACJVS “flat-spot” tests, we use an ac/dc transfer standard.

The transfer standard measures the total rms voltage delivered to its input over a wide bandwidth (dc to many MHz), so everything that the ACJVS generates in that band is included in the rms voltage measurement. We use the instrument on its 220 mV full-scale, range where it has a high-impedance buffer amplifier on its input and the ACJVS supplies a minimal load current. The transfer standard allows us to determine the range for each bias parameter over which the ACJVS output signal remains constant to better than a part in 10<sup>6</sup>. Figure 3 illustrates the flatness results obtained with this method for the four most critical ACJVS parameters at 8 Gbit/s. This was the fastest data rate for which all eight parameters exhibited a “flat-spot.” At that data rate, the peak sinewave amplitude synthesized by the ACJVS is 193 mV (zero-to-peak) at 2.7 kHz using the 8200 Josephson junction dual-array configuration and a 12 GHz microwave drive.

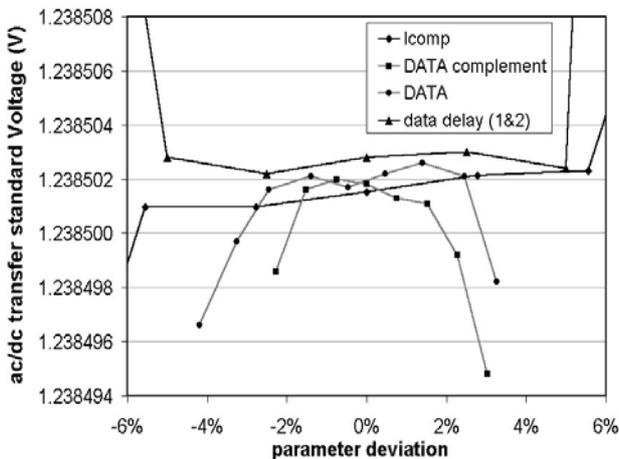


Figure 3. Operating margins obtained for a 193 mV (peak) 2.7 kHz sine wave measured by an ac/dc transfer standard and illustrating the “flat spots” for the four tightest parameters: amplitude (data and data complement), data delay (both 1 & 2 moved together), and  $I_{comp}$ . One vertical division in this graph represents about 1.6 parts in 10<sup>6</sup>.

We also performed these measurements at the maximum data rate for our system of 10 Gbit/s, which produces an ac waveform with a 242 mV peak voltage (the same conditions as for the spectrum data in Fig. 2). However, at this higher data rate we were unable to find a completely flat region for all bias parameters. Thus, we need to further improve the operating margins to fully utilize the ACJVS at this highest data-rate.

Table 1 –ACJVS operating margins at 8 Gbit/s, 2-array configuration.

| Parameter                       | Setpoint | Margin  |
|---------------------------------|----------|---------|
| Amplitude (data)                | 1.07 V   | ±2.5%   |
| Amplitude (data complement)     | 1.32 V   | ±1.5%   |
| RF Power (sine)                 | -2 dBm   | ±17%    |
| RF Power (sine complement)      | -1 dBm   | ±13%    |
| Data Delay (data)               | -46 ps   | ±5%     |
| Data Delay (data complement)    | -46 ps   | ±5%     |
| $I_{comp}$                      | 8.8 mA   | ±5.5%   |
| $t_{comp}$ (compensation delay) | 0°       | ±200ns° |

The details of all eight bias parameters, setpoints, and margins for the dual-array configuration are shown in Table 1, which includes the data from Fig. 3. We define the “operating margin” to be the range over which each parameter was adjusted where the deviation in the ACJVS output measured by the ac/dc transfer standard was below the noise level (about a part in 10<sup>6</sup>). As the table suggests, the smallest margins are the amplitudes of data and data complement. Nevertheless, the stability and resolution of the data-generator outputs allow us to easily maintain those parameters within the required limits.

### Latest Developments

The above “flat-spot” results demonstrate the feasibility of higher-voltage ACJVS systems utilizing multiple arrays. We have also just measured our first ACJVS circuit using stacked MoSi<sub>2</sub>-barrier Josephson arrays in which 2000 stacks of three junctions each were fabricated for a total of 6000 junctions. The operating margins were not perfectly flat on this device, but we are encouraged that we found a flat spot on the data-delay parameter at the part in 10<sup>6</sup> level. With further circuit optimization, we hope to reach higher voltages and improved operating margins with these stacked arrays.

### References

- [1] J.C. Candy, “An Overview of Basic Concepts,” in *Delta-Sigma Data Converters: Theory, Design, and Simulation*, S.R. Norsworthy, R. Schreier, and G.C. Temes, Eds. Piscataway, NJ: IEEE Press, 1997.
- [2] S.P. Benz, F.L. Walls, P.D. Dresselhaus, C.J. Burroughs, “Low-distortion Waveform Synthesis with Josephson Junction Arrays,” *IEEE Trans. Electron.*, vol. E85-C, no. 3, pp. 608-611, Mar. 2002.
- [3] S.P. Benz, C.J. Burroughs, P.D. Dresselhaus, L.A. Christian, “AC and DC Voltages from a Josephson Arbitrary Waveform Synthesizer,” *IEEE Trans. Instrum. Meas.*, vol. 50, pp. 181-184, Apr. 2001.
- [4] S.P. Benz, C.J. Burroughs, P.D. Dresselhaus, “AC Coupling Technique for Josephson Waveform Synthesis,” *IEEE Trans. Appl. Supercond.*, vol. 11, pp. 612-616, Jun. 2001.
- [5] C.J. Burroughs, S.P. Benz, P.D. Dresselhaus, “AC Josephson Voltage Standard Error Measurements and Analysis,” *IEEE Trans. Instrum. Meas.*, vol. 52, no. 2, pp. 542-544, Apr. 2003.