

## ELECTROSTATIC DISCHARGE PROTECTION FOR EMBEDDED-SENSOR SYSTEMS-ON-A-CHIP

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**Abstract-** The MEMS microhotplate-based gas sensor is an emerging technology that has cost and performance advantage compared to existing commercial gas sensing technologies. Microhotplate devices can be fabricated in standard CMOS technology enabling the use of low cost commercial foundries and monolithic integration of electronic circuits [1]-[2]. The MEMS-based gas sensor platform, heater power amplifier, signal conditioning, and control circuitry have recently been formulated as a virtual component (VC) conforming to the SoC design automation methodology facilitating design reuse and enabling the development of single chip gas sensing and classification solutions.

The robustness of Embedded-Sensor (ES) System-on-a-Chip (SoC) devices involve several design constraints that require a unique assessment. For instance, space-efficient electrostatic discharge (ESD) protection must be provided to protect the CMOS devices during the sensor micromachining processes in addition to the protection provided during normal operation and handling. In the post processing of the microhotplate-based gas sensor, there is a potential for an ESD event to occur at the sensing film electrodes prior to sensing film deposition. Fig. 1 depicts an SEM micrograph of a microhotplate-based gas-sensor showing ESD protected nodes. For such a gas-sensor SoC, ESD protection needs to be included not only in all the I/O pads but also in the electrodes of the sensor. Fig. 2 shows a schematic representation of an ESD protection scheme for a gas-sensor SoC.

In this abstract, a reliable and space-optimized on-chip ESD protection scheme for a gas-sensor VC is demonstrated. This ESD protection solution involves design of novel thyristor-type devices [3] implemented in the standard CMOS technology. The novel ESD protection scheme developed in this work includes ground referenced thyristor-type devices for 1) pad-level protection, 2) supply clamp, and 3) sensing electrodes. The I-V characteristics of the thyristor are designed to meet the constraints of the different components of the VC ESD protection by the proper selection of the internal dimensions ( $D$ ,  $D_2$ ,  $L$ ) shown in the cross-sectional view presented in Fig. 3. This property of the designed cell is illustrated by the TLP results for two thyristor devices with different dimension  $D$  presented in Fig. 4.

### References

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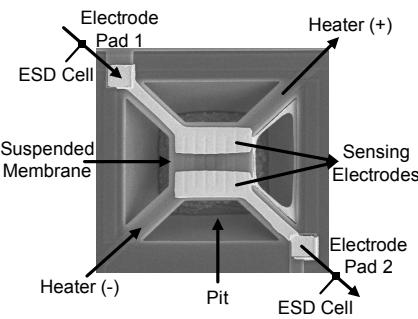


Fig. 1 An SEM micrograph of microhotplate showing sensor electrodes and ESD protection points.

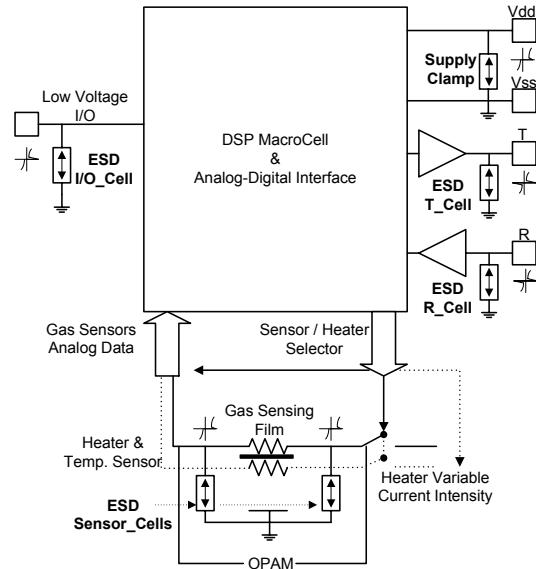


Fig. 2 Schematic representation of the SoC and complete ESD protection structure.

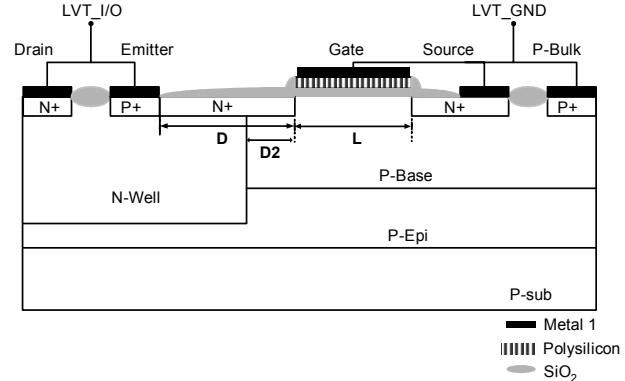


Fig. 3. Cross section view of thyristor-type protection cell.

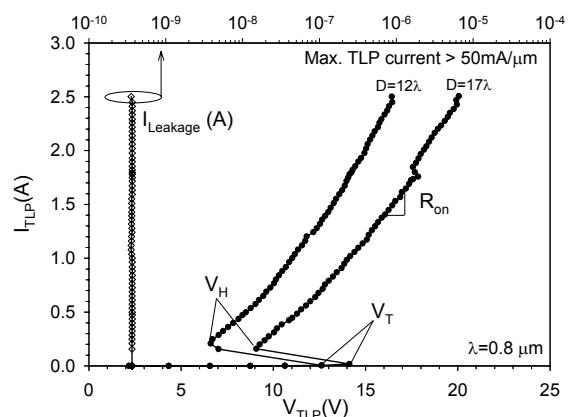


Fig. 4. Transmission Line Pulsing (TLP) I-V Characteristics of Thyristor-Type Cells.