# DOUBLE-STACKED $MoSi_2$-BARRIER JUNCTIONS FOR PROGRAMMABLE JOSEPHSON VOLTAGE STANDARDS[†]

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## Abstract

We are developing $MoSi_2$-barrier stacked-junction arrays for Josephson voltage standards in order to increase the output voltage, operating bandwidth, and operating margins. In this paper we present measurements of a programmable voltage standard circuit with double-stacked arrays, where two junctions are fabricated in each stack. Although a mask defect prevented operation of one-eighth of the fabricated junctions, the remaining circuit, with a total of 57 344 junctions, succeeded in producing an output of 1.93 V with a range of operating current greater than 1 mA for the combined 13 subarrays.

## Introduction

Superconductor-normal-superconductor (SNS) Joseph-son junctions have been successfully used in programmable Josephson voltage standards [1-3] and in the Josephson arbitrary waveform synthesizer [4]. Series arrays of junctions are required to increase the output voltage to practical levels. We also wish to increase the linear junction density in these arrays because this will provide higher output voltage, better operating margins in programmable systems, and better broadband frequency response for ac voltage standards [5]. At NIST we have found that $MoSi_2$ provides a stable, reproducible, dry-etchable, normal-metal barrier for stacked junctions [6]. This reproducibility enables precise targeting of the critical-current density and the characteristic voltage $V_c=I_cR$, where $I_c$ is the critical current and $R$ is the normal resistance. Furthermore, the high resistivity of $MoSi_2$ allows physically larger junctions at a given characteristic voltage. One advantage of larger junctions is that for a given degree of etch anisotropy uniformity of critical current is higher, which is very important for maintaining uniformity in stacked arrays.

In order to increase junction density, we wish to stack as many junctions as possible. In previous work we found that the dc electrical characteristics of the junctions do not begin to change significantly until the thick-ness of the middle superconducting electrode between the normal-metal barriers is decreased below 20 nm [7]. We have also previously investigated and optimized the thermal properties of these $MoSi_2$–barrier stacks [8]. In this paper, we demonstrate arrays of $MoSi_2$–barrier junctions of sufficient uniformity that precision voltages are produced in programmable voltage standard circuits.

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## Fabrication

In order to double the output of our typical 1 V programmable Josephson voltage standard (PJVS) circuit [1] to 2 V, we doubled the number of junctions in the circuit by using double-stacked $MoSi_2$-barrier junctions. There are 65 536 total junctions divided into 8 series-connected arrays of 8192 junctions (4096 double-junction stacks). Each of these arrays is biased in parallel by a 16 GHz microwave drive through splitters and dc blocks. In order to create the smaller voltages and achieve a programmable source, one of these arrays is divided in consecutive binary sequence (4096, 2048,…etc.) into 6 smaller arrays, for a total of 13 arrays, as shown in Fig. 1. The two least significant bits each have 256 junctions.

The fabrication process includes electrodes and wiring niobium superconductor, insulating layers of silicon dioxide, and resistors and contact pads of palladium-gold. The film thicknesses were: 420 nm Nb base electrode, two 22 nm $MoSi_2$ barriers separated by a 44 nm thick Nb middle electrode, 220 nm Nb counter electrode, 300 nm $SiO_2$, 660 nm Nb wiring, and 125 nm PdAu. The metals were dc sputtered and the oxide was deposited using an electron-cyclotron resonance system with backside helium-gas cooling. The vias and wiring were patterned with $CHF_3$ and $SF_6$ reactive ion etching, while the vertical walls of the stacks were patterned in a deep reactive ion etcher by use of a mixture of etch and passivation gasses.

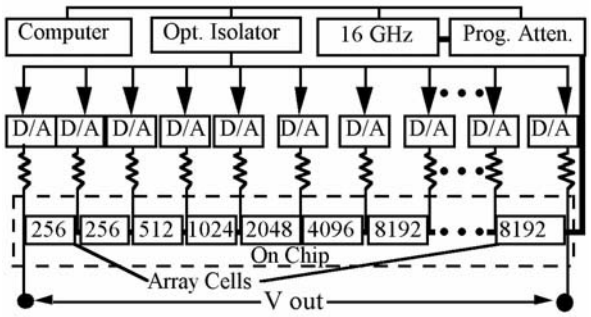


Fig. 1. PJVS schematic for double-stacked arrays showing computer control, dc and microwave bias, and binary division of the 13 arrays cells. Only two of the seven largest cells with 8192 junctions are displayed.

## Measured Results

The characteristic voltage for this array was about 45 μV, while the critical currents for the 4 μm-square junctions were about 6.5 mA. Table I summarizes the electrical characteristics of the different cells, including the critical current when no microwaves are applied as well as the current range of the first constant-voltage step. Similar current ranges were found for the opposite polarity step. Cell 7 does not have a flat step, as indicated by its zero current range, which prevents the

circuit from operating at its maximum output voltage of 2.2 V. The microwave power was increased until the current range of all the operating steps exceeded 1 mA. Current-voltage *IV* characteristics are shown in Fig. 2 for six cells having different numbers of junctions. Since the *IV* curves are symmetric, the zero-voltage step range is greater than 3 mA for all the circuits shown. However, as a result of variation in power delivered to the arrays, one of the 8192-junction cells (not shown) has a zero-step range of only 1.6 mA.

Table I. Electrical characteristics of the array cells.

| Cell Number | Number of JJs | $I_c$ (mA) | First Step Range (mA) |
|---|---|---|---|
| 1 | 8192 | 6.72 | 1.11 |
| 2 | 8192 | 6.64 | 1.18 |
| 3 | 8192 | 6.64 | 1.04 |
| 4 | 8192 | 6.64 | 1.17 |
| 5 | 8192 | 6.56 | 1.00 |
| 6 | 8192 | 6.56 | 1.33 |
| 7 | 8192 | 6.52 | 0.00 |
| 8 | 4096 | 6.40 | 1.20 |
| 9 | 2048 | 6.32 | 1.52 |
| 10 | 256 | 6.32 | 1.60 |
| 11 | 256 | 6.40 | 1.94 |
| 12 | 512 | 6.32 | 1.61 |
| 13 | 1024 | 6.36 | 1.46 |

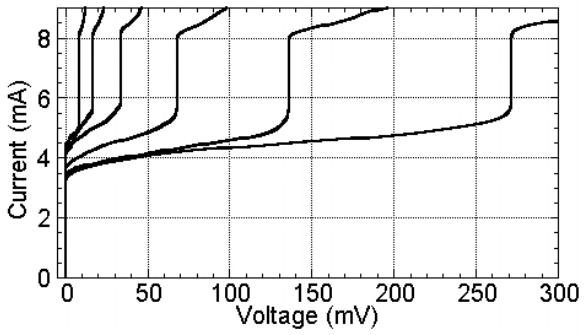


Fig. 2. Current-voltage characteristics for different array cell sizes from the PJVS circuit with $MoSi_2$ double-stacked junction arrays. The smallest voltage step corresponds to a 256-junction array and the largest voltage step is from cell 1, one of the seven 8192-junction cells.

In order to make a high-resolution measurement of the operating margins for this circuit (excluding cell 7), we biased half of the junctions on the positive step (+0.96 V) and half of the junctions on the negative step (−0.96 V). This yields zero net voltage across the circuit, allowing us to measure the operating current range for the circuit on the highest sensitivity (1 mV) range of our nanovolt-meter. The current-voltage characteristic of this measure-ment is shown in Fig. 3. The total operating current range for the combined voltage step from all 12 arrays is about 1 mA. The voltage of the combined step is flat within the 40 nV noise of the measurement. The voltage is offset from zero due to a 480 nV thermal voltage from the non-metrology grade leads and contacts used for this measurement. We have removed these thermal voltages in previous experiments by using copper-block connectors in a thermally isolated box [9].

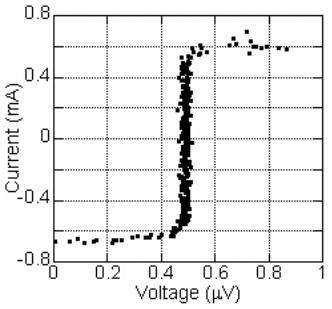


Fig. 2. High-resolution measurement of step flatness showing current range of about 1 mA measured on the 1 mV scale of a nanovoltmeter. Half of the junctions are biased on the positive voltage step and half are on the negative voltage step.

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