Precision Measurements of AC Josephson Voltage Standard Operating Margins

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***Abstract*—Recent advances in circuit design and fabrication of superconducting integrated circuits have enabled us to demonstrate an ac Josephson voltage standard (ACJVS) that generates both ac and dc waveforms up to 242-mV peak voltage. Using a Fast Fourier Transform spectrum analyzer and an ac-dc transfer standard, we characterize ACJVS operating margins by performing "flat-spot" measurements at the level of a part in 10^6 for all eight bias parameters. By verifying that every bias parameter has a "flat-spot" (i.e., a range of bias values over which the measured ACJVS output is precisely constant), we demonstrate that all Josephson junctions on the chip are operating properly.**

***Index Terms*—AC measurements, AC voltage standard, Josephson arrays, Josephson devices.**

I. Introduction

FOR A NUMBER of years, NIST has been developing a Josephson arbitrary waveform synthesizer and utilizing this technology to create an ac Josephson voltage standard (ACJVS) system. This system can generate a variety of precision voltage waveforms, including single-tone ac sinewaves and dc voltages so that it can be used as a quantum-based voltage standard for ac metrology. The present system uses a chip with two Josephson arrays (8200 junctions total) and digital-to-analog conversion using delta-sigma modulation [1], where a digital data stream at 10 Gbit/s is combined with a 15 GHz sinusoidal drive signal for a maximum bipolar pulse-repetition frequency of 1.5×10^{10} pulses/s. This combined signal is fed to the Josephson junctions, which precisely quantize the pulses, thus, producing a nearly ideal delta-sigma pulse train and a precisely known output waveform. The unprecedented accuracy of this technique for generating ac and dc waveforms for voltage metrology has been discussed previously [2], [3].

The latest dual-array ACJVS chips produce voltages up to 242 mV (zero-to-peak) for ac waveforms, and ± 254 mV for dc voltages. This allows us to perform practical metrology measurements with rms amplitudes up to 170 mV. Fig. 1 shows the bias configuration for the chip, where the broadband digital pulse drive to each array is split into a high-frequency component (10 MHz to 30 GHz) and a low-frequency component (dc to 10 MHz). These separated signals are independently delivered to the arrays by use of 10 MHz high-pass filters on both digital drive signal lines that transmit only the high-frequency component, and a separate sinusoidal current ($I_{\rm comp}$) at the fundamental frequency applied to both arrays. The two arrays are connected in series on-chip so that their low-frequency output voltages add. This configuration allows either end of the dual-array circuit to be connected directly to ground, an essential feature for connecting the ACJVS output to spectrum analyzers, ac–dc transfer standards, thermal voltage converters (TVCs), and other ac and dc voltage metrology instruments. A number of circuit innovations on the chip make this configuration possible, and those details have been presented elsewhere [4].

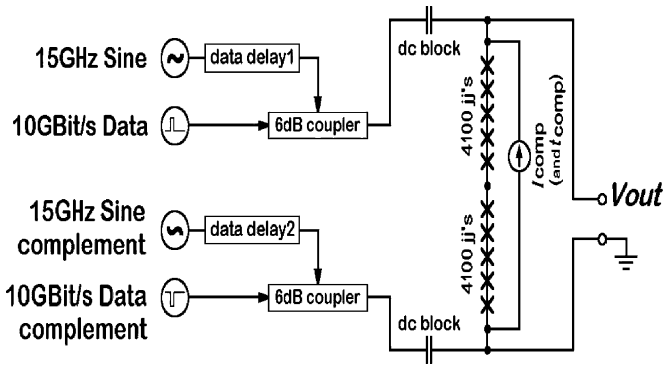

Fig. 1. Diagram of the ACJVS dual-array system configuration consisting of eight adjustable bias parameters.

In order for the ACJVS to produce the correct output voltage, the eight independent bias parameters in Fig. 1 must all be set correctly. There are two 10 Gbit/s digital data amplitudes (one for each array), two 15 GHz sinusoidal drive amplitudes (one for each array), and two data delays that shift the phase between the microwave sinusoidal drives and the digital data signals. The digital bit-stream to the top array is the logical complement of the bit-stream to the bottom array. (This is because our present microwave design connects the two Josephson arrays together end-to-end at the microwave terminations which requires us to invert the sign of one array so that their output voltages add instead of subtract). The compensation current $I_{\rm comp}$ provides the low-frequency bias at the fundamental frequency of the ACJVS. This current flows through the 8200 series-connected junctions only, and does not provide any load current for $V_{\rm out}$. (An additional output current would be used in order to connect $V_{\rm out}$ to a device that required significant load current). The compensation delay $t_{\rm comp}$ is the adjustment of the phase of $I_{\rm comp}$ with respect to the digital data signals.

II. Operating Margin Measurements

We use the term "operating margins" to designate the region in the 8-dimensional space of the bias parameters where each junction in each array is generating precisely one quantized

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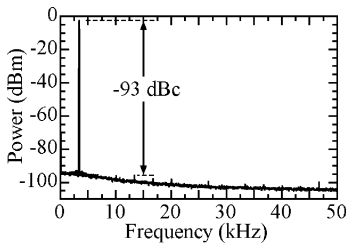

Fig. 2. Spectrum analyzer measurement demonstrating -93 dBc low distortion of the ACJVS with two Josephson arrays generating a 242-mV (zero-to-peak) sinewave at 3.3 kHz using 8200 junctions at the 10 Gbit/s data-rate of our system. The spectrum measurement uses 100 Hz resolution bandwidth and 100 averages.

pulse for every input pulse. To determine the midpoint and range for each of these bias parameters, we use a spectrum analyzer to examine the synthesized waveforms in the frequency domain and tune the biases by observing the fundamental frequency and minimizing the first few harmonics. If any of the junctions are not within their operating margins, distortion harmonics will appear and the precise amplitude of the fundamental may be compromised. Fig. 2 shows a typical measured spectrum of the ACJVS after the operating margins have been optimized. Notice that the power of the largest distortion harmonic is -93 dBc (i.e., 93 dB below the fundamental tone). At that level, the effect of such a harmonic on the total rms voltage output is negligible (< 1 nV/V) because it combines as a square root of the sum of the squares (RSS) contribution [5].

The spectrum analyzer is the most convenient tool we presently have for optimizing the bias parameters because it performs many spectrum measurements per second, and quickly displays changes to the distortion harmonics when the bias parameters are adjusted. The noise floor in Fig. 2 is the lowest we can attain with standard settings for our spectrum analyzer. We can lower the noise floor an additional 10 dB by increasing the gain of the input amplifier by a factor of 10, which lights the over-limit indicator and causes a second harmonic to appear. As illustrated in Fig. 3, this technique allows us to determine the ACJVS bias set-points with 10 dB better resolution for the harmonics, but it adds the additional step of checking each array separately to verify that the second harmonic observed during simultaneous array operation is not real. The individual 4100 junction arrays measured separately with lower amplitudes do not show a measurable second harmonic. The spectrum measurement was performed with 3 Hz resolution bandwidth and no averaging. Tones appearing above the noise floor for frequencies greater than 20 kHz are spurious signals detected even when the array signal is turned off, (i.e., except for the second harmonic, none of the tones above the noise floor are distortion harmonics).

The spectrum analyzer is also well suited to directly measure error voltages caused by the large-magnitude current (roughly 10 mA) of the low-frequency compensation current, $I_{\rm comp}$. We refer to these error terms as $V_{\rm induc}$, which is the voltage generated at the fundamental frequency by $I_{\rm comp}$ flowing through the on-chip inductance, and $V_{\rm io}$, which represents the input–output coupling from $I_{\rm comp}$ to the ACJVS output leads. The sum of these error voltages can be measured directly by turning off the

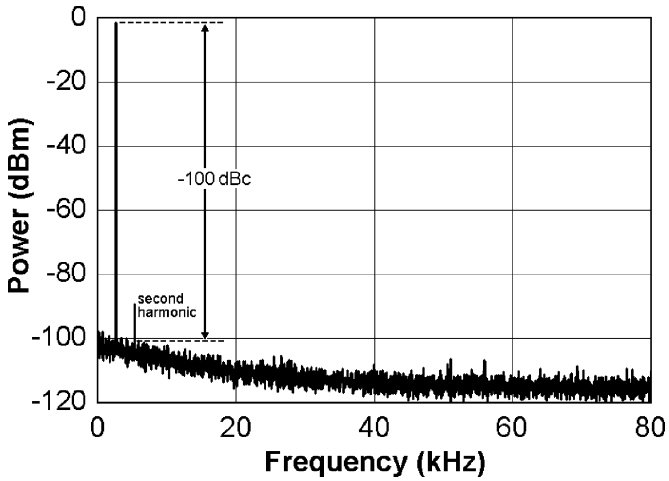

Fig. 3. Spectrum analyzer measurement demonstrating -100 dBc low distortion of the ACJVS with two Josephson arrays generating a 193-mV (zero-to-peak) sinewave at 2.7 kHz using 8200 junctions at 8 Gbit/s (same digital bit-stream as Fig. 2, but at a lower data rate).

digital data and rf sinewaves to the chip, so that only the compensation bias current flows though the 8200 Josephson junctions. The spectrum analyzer can then directly measure the combined error voltages, $V_{\rm induc}$ and $V_{\rm io}$, provided that $I_{\rm comp}$ is less than the critical current of the arrays ($I_{\rm c}$). If $I_{\rm comp}$ is larger than the critical current, then we make the measurement by decreasing $I_{\rm comp}$ below $I_{\rm c}$ and appropriately scaling the measured error voltage.

The magnitude of the combined error voltages $V_{\rm induc}$ and $V_{\rm io}$ for the chip and system configuration presented in Fig. 2 was -80.1 dBc. This result is for our latest generation cryoprobe, which shows an improvement in $V_{\rm io}$ of roughly 17 dB compared to previous models. The magnitude and phase of this measured error voltage can be used in two different ways. The first method would be to include the measured error in our final calculation of rms value and uncertainty for the ACJVS output voltage. The other method is to use an "error correction signal" that adds a small series voltage at the fundamental frequency to the ACJVS output. Using the spectrum analyzer display, the amplitude and phase of the correction signal can be tuned to exactly cancel the undesired peak observed for $V_{\rm induc}$ and $V_{\rm io}$. This technique has been demonstrated to provide significantly improved accuracy of the ACJVS system at audio frequencies [5], but was not necessary for the measurements presented in this paper.

III. Precision "Flat-Spot" Measurements

In order for the ACJVS system to meet the definition of an "intrinsic" ac and dc standard, its output must be independent of every parameter except the digital data stream, the clock frequency, and the number of junctions in the array. In other words, there must be a finite range for each bias parameter over which the output voltage does not measurably change [3]. This flat spot in the operating margins needs to be confirmed every time the ACJVS system is used for precision measurements. Spectrum analyzers are not well suited for this task because they have limited ability to detect tiny error signals occurring at the fundamental frequency. For full characterization of the ACJVS we

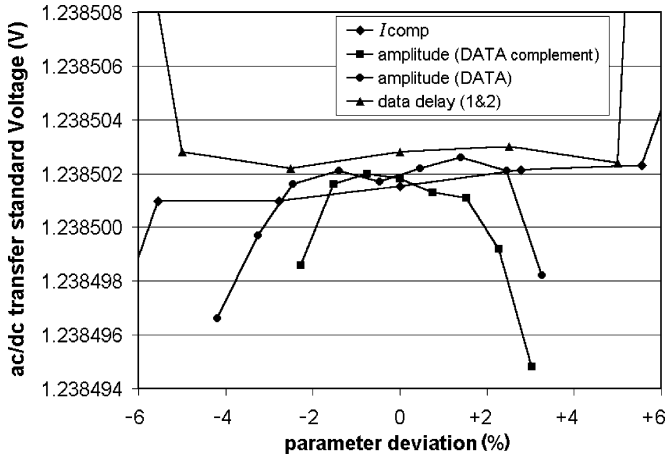

Fig. 4. Operating margins for our 12E design obtained for a 193-mV (peak) 2.7-kHz sine wave measured by an ac-dc transfer standard and illustrating the "flat spots" for the four parameters with the smallest range: amplitude (data and data complement), data delay (both 1 and 2 moved together), and $I_{\rm comp}$. One vertical division in this graph represents about 1.6 parts in 10^6.

need to be able to verify that a flat spot exists with respect to in-phase error sources at the fundamental, because they will add directly to the output rms value (not as a RSS contribution as in the case of distortion harmonics) [5]. For example, a very small distortion or error signal of -100 dBc in the ACJVS output *at the fundamental* (with a relative phase of 0° or 180°) would be undetected by the spectrum analyzer, but would still produce an error of 10 parts in 10^6 in the rms voltage. Thus, in order to perform the final high-precision ACJVS "flat-spot" tests, we use an ac-dc transfer standard.

The transfer standard measures the total rms voltage delivered to its input over a wide bandwidth (dc to many MHz), so everything that the ACJVS generates in that band is included in the rms voltage measurement. We use the instrument on its 220-mV full-scale range where it has a high-impedance buffer amplifier on its input and the ACJVS supplies a minimal load current. The transfer standard produces a 0 Volt to 2 Volt output voltage that is linearly proportional to the ratio of the input rms voltage to the full-scale input range. The low noise of the instrument allows us to determine the margin for each bias parameter over which the ACJVS output signal remains constant to better than a part in 10^6. Fig. 4 illustrates the flatness results obtained with this method for the four most critical ACJVS parameters at 8 Gbit/s. This was the fastest data rate for which all eight parameters exhibited a "flat-spot" using both Josephson arrays simultaneously. At that data rate, the peak sinewave amplitude synthesized by the ACJVS was 193 mV (zero-to-peak) at 2.7 kHz with the 8200 Josephson junction dual-array configuration and a 12 GHz microwave drive (the same conditions as for the spectrum data in Fig. 3).

We also performed these measurements at the highest data rate of 10 Gbit/s, which produced an ac waveform with a 242-mV peak voltage (the same conditions as for the spectrum data in Fig. 2). However, at this higher data rate we were unable to find a completely flat region for all bias parameters. Thus, we need to further improve the operating margins of the Josephson arrays to fully utilize the ACJVS at this highest data rate.

TABLE I
ACJVS OPERATING MARGINS AT 8 GBIT/S, DUAL-ARRAY CONFIGURATION

Parameter	Setpoint	Margin
Amplitude (data)	1.07 V	±2.5%
Amplitude (data complement)	1.32 V	±1.5%
RF Power (sine)	-2 dBm	±17%
RF Power (sine complement)	-1 dBm	±13%
Data Delay (data)	-46 ps	±5%
Data Delay (data complement)	-46 ps	±5%
$I_{\rm comp}$	8.8 mA	±5.5%
$t_{\rm comp}$ (compensation delay)	0°	±200ns

The details of all eight bias parameters, set-points, and margins for the dual-array configuration are shown in Table I, which includes the data from Fig. 4. We define the "operating margin" to be the range over which each parameter was adjusted where the deviation in the ACJVS output measured by the ac-dc transfer standard was below the noise level (about a part in 10^6). During the 15 minutes over which the measurements in Table I were recorded, the median output voltage of the transfer standard was 1.238 502 V with a small amount of noise and drift that scattered the measurements by no more than ± 1 part in 10^6. As the table suggests, the smallest margins occur for the amplitudes of data and data complement. Nevertheless, the stability and resolution of the data-generator outputs allow us to easily maintain those parameters within the required limits.

IV. RECENT DEVELOPMENTS

We have fabricated and measured a number of different chip designs with 8200-junction dual-array circuits. The objective of these efforts is to improve the operating margins by creating better on-chip filters for the low-frequency bias lines so that these low-speed connections have minimal effect on the uniformity of the high-frequency data stream. The previous data were for our 12E design, which has six small inductive coils in series. Another design that shows some promise is our 14D design, in which each bias line has ten coils of various sizes to increase the filter inductance over a wider frequency band. This latter design requires the use of bias tees to inject the low-frequency $I_{\rm comp}$ into the high-speed coaxes following the dc blocks. This bias scheme avoids large unwanted signals that would be induced by the compensation current in the higher-inductance filters.

Fig. 5 shows the critical operating margins for this newer circuit design. We use this example to discuss some of the difficulties in producing these devices. These results are for a 193-mV (zero-to-peak) sinewave generated by the ACJVS at 2.7 kHz using the 8200 junction dual-array configuration with an 8 Gbit/s data-rate and a 12 GHz microwave drive. Ideally, all four curves would be superimposed at 0%, but during this particular measurement the curves are spread apart because the transfer standard value at 0% drifted five parts in 10^6, from 1.237 460 V to 1.237 465 V. These measurements were taken over the course of an hour in the exact order suggested by the drift in the graph: data, data-complement, data delay, and finally $I_{\rm comp}$. Notice that an acceptable flat-spot exists for every parameter in Fig. 5 except $I_{\rm comp}$, which clearly has a small slope. Further investigation of the individual array segments is shown in Fig. 6, where we discovered that the slope was caused

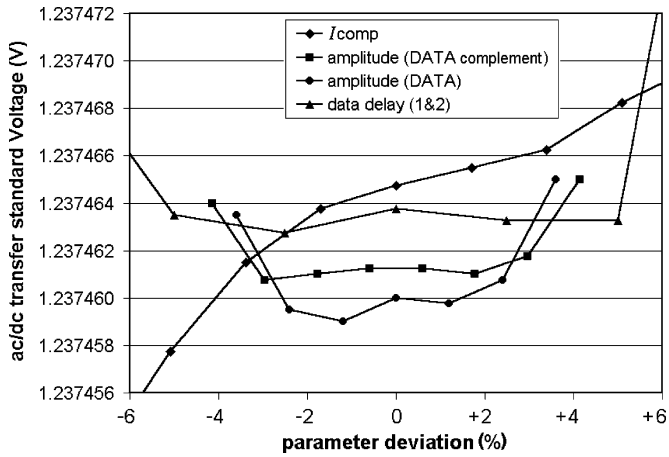

Fig. 5. Operating margins for our 14D design obtained for a 193-mV (peak) 2.7-kHz sine wave measured by an ac-dc transfer standard and illustrating the "flat spots" for the four parameters with smallest range: amplitude (data and data complement), data delay (both 1 and 2 moved together), and $I_{\rm comp}$. One vertical division in this graph represents about 1.6 parts in 10^6.

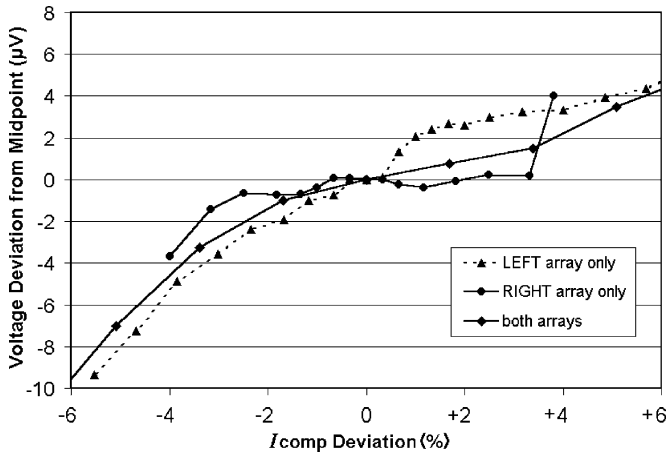

Fig. 6. Measured margins for compensation current $I_{\rm comp}$ obtained for a 193-mV (peak) 2.7-kHz sine wave measured by an ac-dc transfer standard. The compensation current of the right array has a significantly better "flat-spot" than that of the left array. One vertical division in this graph represents about 1.6 parts in 10^6 of the total voltage measured by the transfer standard.

primarily by the left array. The right array shows a clear flat spot, suggesting that the slope from the compensation current in the left array was not an inherent problem in the 14D design.

Another unexpected feature of the data is the difference between the mean voltages at 0% offset for Fig. 5 (1.238 502 V) and Fig. 6 (1.237 462 V). These values were taken about 1 year apart, and the source of the $\sim$ 1 mV inconsistency requires further investigation. One possible explanation is that the manufacturer of the transfer standard gives a specification for the full-scale output value as 2 V with a 5% tolerance. The sinewaves used in the measurements of Figs. 5 and 6 both have a calculated rms voltage of 136.685 mV, so with this rms input applied to the 220-mV range we expect a transfer standard output within 5% of 1.243 V. Our measured rms voltages are approximately 0.4% lower than the nominal value, so this is well within the manufacturer's specification. It is also possible that the discrepancy between the data sets is related to differences in the ACJVS on-chip filters, cryoprobe output wiring, or grounding configurations. A detailed evaluation will be required in the future to characterize and minimize these effects in order to create a calculable ACJVS system.

With regard to future work, we have developed a new fabrication technology based on arrays of stacked junctions that dramatically increases the number of junctions we can place in a single transmission line, thus, increasing the total output voltage [6], [7]. These devices use $\rm MoSi_2$ barriers that have larger area than our PdAu devices, and consequently have better junction uniformity and larger operating margins [8]. We have measured our first ACJVS circuit using stacked $\rm MoSi_2$-barrier Josephson arrays in which 1000 stacks of two junctions each were fabricated for a total of 2000 junctions. The operating margins were not perfectly flat for the 73-mV (zero-to-peak) voltage synthesized with this stacked-junction array, but we are encouraged that we found a flat spot on the data-delay parameter at the part in 10^6 level. With further circuit optimization, we hope to reach higher voltages and improved operating margins with stacked arrays.

V. Conclusion

The "flat-spot" results reported here demonstrate the feasibility of higher-voltage ACJVS systems utilizing multiple arrays, and lay the groundwork for a practical ACJVS based upon a quantum voltage source that delivers precisely calculable dc and ac voltages. Future efforts will be aimed at improving the operating margins and increasing the output voltage using stacked arrays combined with careful construction and characterization of the filters, chip packages, and cryo-probes that make up the output path so that potential sources of error and uncertainty can be either minimized or well-understood.

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