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SILICON-BASED, TUNABLE-BARRIER SINGLE CHARGE SOURCES

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Abstract

We have demonstrated the operation of, and are assessing theoretically and experimentally the error rates of, silicon-based single-electron turnstiles, pumps, and CCDs. These devices are conceptually very similar to the metal-based pumps which have already proven to have a very low error rate; potentially, the Si-based devices have several substantial advantages, including higher current value, higher temperature of operation, and simpler operation.

Introduction

For some years, several metrology laboratories around the world have been pursuing standards of charge based on the charge of the electron e, using the Coulomb blockade. At present, the major application of this has been for a capacitance standard[1], by using metal-based tunnel junctions as the basis of the SET pump. These pumps have been shown[2] to have a relative error rate of less than 10^{-8}, for a maximum cycle frequency of about 20 MHz. An obvious application of such charge sources is a current standard, with a value of I = ef; however, the maximum frequency corresponds to a value of about 3 pA, which is too small to be directly useful. Other laboratories have been pursuing other possible routes to a current standard, which have not yet come to fruition.

We have recently been pursuing Coulomb blockade-based charge sources based on CMOS-compatible Si-based devices. These devices have several potential advantages with respect to the metal-based ones:

1) Higher temperature of operation: the metal-based devices have a maximum temperature of operation of about 0.1 K; this is set by the minimum value of capacitance. The Si-based devices have about a factor of 10 smaller capacitance; thus, we expect that the maximum temperature of operation will be concomitantly higher.

2) Higher current value: because of the smaller capacitance value, we also expect the maximum frequency of operation to be concomitantly higher. We show some preliminary results demonstrating this below.

3) Ease of operation: one of the common features to the various types of Si-based charge sources which we have developed is the tunable barriers. This feature minimizes the effect of cotunneling, which in the metal-based devices makes it necessary to use six time-dependent gate voltages[2]. In contrast, for all three classes of devices which we have demonstrated[3,4,5] (turnstiles, pumps, and CCD's), we may only need two gates.

4) Lack of charge offset drift: a common feature of the metal-based devices is the drift in the charge offset on the islands by large fractions of 1 e. In a continuously operating current standard, this would require periodic retuning of the gates to avoid a large error rate. In contrast, the Si-based devices appear to have a much smaller rate of drift[6], thus avoiding this problem.

5) By parallelizing many Si devices, we hope to reach much higher total currents. CMOS-compatible Si devices may afford all the inherent industrial advantages necessary to make tens, hundreds or thousands of devices.

Results

Fabrication: We have made two different classes of devices. The first, which resulted in the pump[3] and turnstile[4] devices, were based on our special technique for making non-gated tunnel barriers by using pattern-dependent oxidation (PADOX) [7]. The second class[5], which uses a turnstile which resembles a CCD in its geometry, uses a single Si wire with overlaid gates to form electrostatically-controlled barriers. In the first class, there are separate MOSFET gates just outside the fixed tunnel barriers which, by the series resistance of the MOSFET, can turn off conduction through each of the tunnel junctions independently. Thus, a common feature of all these devices is the tunability of the resistance of the barrier (where we now define the barrier to include the MOSFET in series).

Basic Operation: As an example, we show in Fig. 1 a schematic diagram of the CCD-type device (a), along with the basic operation of the gates (note that of the three "lower" gates, one is unused in this process). In part (b), we show the most basic time dependence of the two gates: simple on-off pulses. In part (c), we schematically indicate the state of the electrostatic barriers and the island, for each of the steps in part (b). Note that in this case, we have assumed the voltages are set such that the

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stable number of electrons on the island is two when it is in contact with the source, and one when in contact with the drain; thus, in operation, we would expect one net electron would be transferred in each cycle of the device.

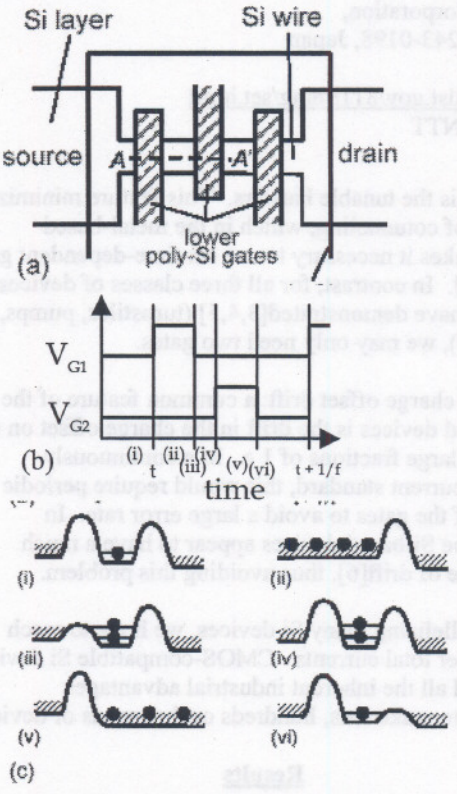
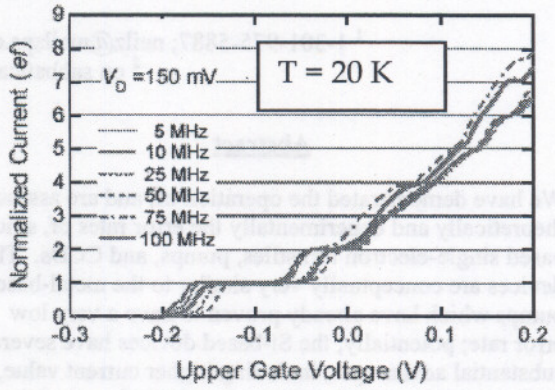


Fig. 1 a) Schematic layout of the CCD-type device, with a Si nanowire covered by three gates, which form the tunable barriers. The upper gate, which covers the area of the rectangle with three sides, is coupled to the island sandwiched by two of the lower gates. When the barriers are high, the resistance can be at least as large as $10^{19}\Omega$. b) Schematic of time dependence of the voltages applied to two of the gates (the third is unused). c) Schematic of electrostatic potential as a function of position along the wire. The two peaks correspond to positions underneath the two gates. (i), …, (vi) correspond to the times in (b). When both barriers are high [(i) and (iv)], the number of electrons on the island is quantized due to the Coulomb blockade. One interesting time regime is (iii) or (vi), where the barrier is rising, but the number of electrons is indeterminate. In this region, if the barrier is raised too fast, the wrong number of electrons may be locked in on the island, resulting in the "dynamical" error.

Operation as turnstile: We have demonstrated transfer of single electrons in all three device; we show one result, from the CCD-type device, in Fig. 2. Here we show the normalized current I/ef for frequencies f up to 100 MHz, at a temperature of 20 K. Note that the first plateau as a function of the upper gate is as wide at 100 MHz as any of the lower frequencies; the plateau has a non-flatness of less than 1 % (the uncertainty of the current meter).

We hope and expect to have detailed measurements of the error rate as a function of frequency and temperature for discussion in London.



Theory: We have developed a theoretical model for the various error mechanisms. This model includes the "dynamical" error which considers the quantum mechanics of how electrons respond when barriers are raised (i.e., how do electrons move when a switch is opened?). Our estimate from many error mechanisms is that an acceptable error rate should be achievable well above 1 K, and at hundreds of MHz.

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