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Compact models for silicon carbide power devices

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Abstract

Compact silicon carbide (SiC) power semiconductor device models for circuit simulation have been developed for power Schottky, merged-PiN-Schottky, PiN diodes, and MOSFETs. In these models, the static and dynamic performance of the power SiC devices requires specific attention to the low-doped, voltage blocking drift region; the channel transconductance in MOS devices; the relatively low-intrinsic carrier concentration; the incomplete ionization of dopants; and the temperature dependent material properties. The modeling techniques required to account for each of these characteristics are described.

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1. Introduction

Silicon carbide (SiC) power devices have recently emerged with performance that is superior to that of silicon (Si) power devices. Prototype devices have already demonstrated improvements over Si technology for various current and voltage ratings [1,2], and SiC Schottky diodes have already become commercially available [3,4].

In order for circuit designers to fully utilize the advantages of the new SiC power device technologies, compact models are needed in circuit and system simulation tools. Physics-based models are preferred over empirical or semi-empirical models since physics-based models provide a better fit to measured data over a wide range of application conditions, and provide known and extractable parameters, such as dopant density, base width, device area, and mobility. The substantially different material parameters of SiC, as compared to Si, require new and novel power device structures with different modes of operation. Therefore, SiC power device models must describe device characteristics not considered by traditional device descriptions used for Si microelectronic and power device models.

2. Modeling silicon carbide power device characteristics

Silicon carbide, specifically, 4H–SiC, has an order of magnitude higher breakdown electric field (2.2×10^6 V/cm) than silicon, thus leading to the design of SiC power devices with thinner (0.1 times Si devices) and more highly doped (10 times higher) voltage-blocking layers [1,5]. The device characteristics as a result of the thinner, more highly doped blocking layer must be considered when modeling SiC devices.

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2.1. SiC power MOSFET model

Fig. 1 shows the topology of a physics-based model for a vertical power MOSFET superimposed on the device structure. In Fig. 1, MOS represents the MOSFET channel, R_b is the undepleted base or drift region resistance (Ω), R_s is the constant series drain resistance (Ω), C_{dsj} is the non-linear drain–source junction capacitance (F), C_{gdj} is the non-linear gate–drain overlap depletion capacitance (F), C_{oxd} is the constant gate–drain overlap oxide capacitance (F), C_{oxs} is the constant gate–source overlap oxide capacitance (F), and C_m is the constant gate–source metallization capacitance (F). For majority carrier power devices such as power MOSFETs, the combination of a 10 times higher drift region dopant density along with a 10 times thinner drift layer yields a SiC device with a factor of 100 advantage in drift region resistance R_b compared to that of Si device.

The measured (solid) and simulated (dashed) output characteristics for a 2 kV, 5 A SiC double-implanted MOSFET (DiMOSFET) [2] and a 400 V, 5 A Si double-diffused MOSFET (DMOSFET) are shown at 25 °C in Fig. 2. For a typical Si MOSFET the output curves are linear in the on-state region and have a pronounced change in curvature as the pinch-off region is approached. This occurs because the Si power DMOSFET has a large epitaxial layer resistance in series with the MOSFET channel, and the channel has a very high transconductance. The SiC curves in Fig. 2 on the other hand, gradually transition from the linear region to the saturation region. In SiC DiMOSFETs, the epitaxial layer resistance is much smaller and the channel resistance is higher due to the low-channel surface mobility, thus making the MOSFET channel a more significant contributor to the on-state voltage.

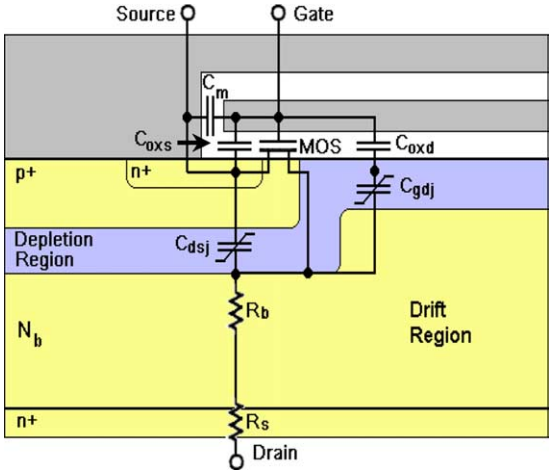

Fig. 1. Topology of physics-based model of a VDMOSFET superimposed on device structure.

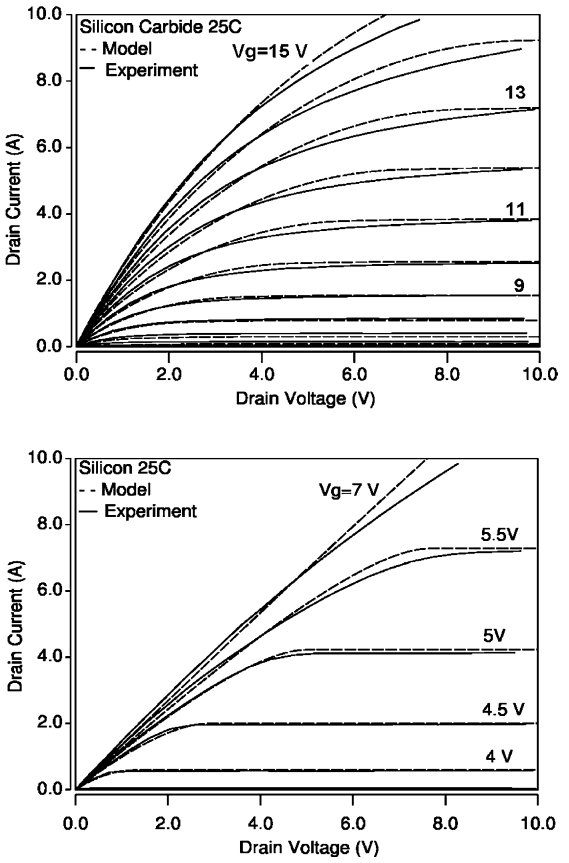

Fig. 2. Measured (solid) and simulated (dashed) output characteristics of a SiC 2 kV, 5 A DiMOSFET (top) and a Si 400 V, 5 A DMOSFET (bottom).

Because the SiC curves have less resistance in series with the MOSFET channel, an enhanced linear region transconductance model is essential, where unique transconductances are extracted for both the linear and saturation regions of operation [6]. The transconductances are defined as the saturation region transconductance K_p (A/V^2) and the linear region transconductance factor K_f, where the channel current equations are given by [7]

$$I_{mos} = \frac{K_f K_p \left[(V_{gs} - V_T) V_{ds} - P_{vf}^{y-1} V_{ds}^{y} (V_{gs} - V_T)^{2-y/y} \right]}{(1 + \theta(V_{gs} - V_T))} \quad (1)$$

for $V_{ds} \leqslant \frac{V_{gs} - V_T}{P_{vf}}$ and $y = \frac{K_f}{K_f - \frac{P_{vf}}{2}}$ is valid for the linear region, while

$$I_{mos} = \frac{K_p (V_{gs} - V_T)^2}{2(1 + \theta(V_{gs} - V_T))} \quad \text{for } V_{ds} > \frac{V_{gs} - V_T}{P_{vf}} \quad (2)$$

is valid in the saturation region of operation. In these equations, I_{mos} is the MOSFET channel current (A), V_{ds} is the MOSFET channel voltage (V), V_{gs} is the gate–

source voltage (V), V_T is the MOSFET channel threshold voltage (V), y is the pinch-off voltage exponent, P_{vf} is the pinch-off voltage factor, and θ is the transverse electric field parameter (V^{-1}). Note, the model is formulated such that (1) reduces to a set of equations that describe the characteristics of the Si DMOSFET, as demonstrated in Fig. 2. Model parameters for the SiC and Si MOSFETs are listed in [6].

Fig. 3 shows both simulated (dashed) and measured (solid) SiC DiMOSFET turn-on waveforms versus gate resistance under resistive load conditions. The turn-on process begins with the driver circuit ramping to 15 V. Gate current immediately begins to flow as the gate capacitances C_{gs} and C_{gd} are charged. Once V_{gs} increases to the threshold voltage V_T, current begins to increase through the drain and the drain voltage begins to fall. As the drain voltage drops, the gate current charges the gate–drain capacitance. The charging of the gate–drain capacitance occurs in two phases: in the first phase for high drain voltages, the drain voltage falls more rapidly because C_{gd} is dominated by the depletion capacitance C_{gdj} and is relatively small, then in the second phase when V_{gd} becomes less than the gate–drain overlap inversion threshold voltage [6], the drain voltage falls more slowly because C_{gd} is equal to C_{oxd} and is much larger. As the drain voltage begins to approach the on-state voltage, C_{gd} is not being charged and the gate voltage begins to rise again toward the gate supply voltage as C_{gs} and C_{oxd} are charged.

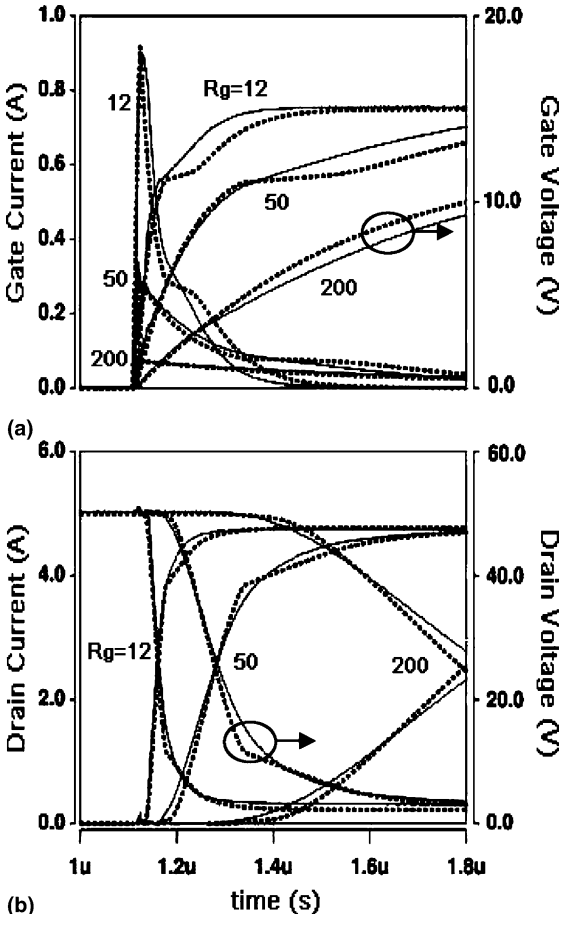

Fig. 3. Measured (solid) and simulated (dashed) switching characteristics vs. gate resistance of a SiC 2 kV, 5 A DiMOSFET.

The temperature dependence of model parameters and material properties are also important when using physics-based models to predict the terminal characteristics of devices [7]. There are two types of temperature dependencies used in compact device models: First, there are the temperature-dependence of the model parameters, such as threshold voltage, which depends on the device structure (e.g. gate thickness or dopant density). Model parameter expressions are generally a lumped set of structural and material properties that can vary between processes, therefore the associated temperature-dependent expressions that describe the model parameters require extraction of coefficients over a range of temperatures. Second, there are the temperature-dependent material properties of the semiconductor, such as the temperature dependence of the intrinsic carrier concentration n_i used to calculate the built-in potential, or the bulk carrier mobility expression that is used to describe the temperature dependence of the undepleted base resistance R_b in Fig. 1. The undepleted base resistance takes the form

$$R_b = W/qAN_b\mu_n, \tag{3}$$

where W is the undepleted base width (cm), q is the fundamental electronic charge (C), A is the device active area (cm^2), N_b is the base dopant density (cm^{-3}), and μ_n is the temperature-dependent bulk carrier mobility ($cm^2/V\,s$).

2.2. SiC power diode model

For minority carrier conductivity modulated devices such as the PiN diode, a blocking layer of 0.1 times the thickness of a Si device can result in a factor of 100 faster switching speed. This is possible because the diffusion length, L (cm), required to modulate the conductivity of the blocking layer can also be reduced to 1/10th the value required for Si, thus permitting the reduction of the lifetime, τ (seconds, s), by a factor of 100 according to $L = \sqrt{D\tau}$, where D is the diffusion coefficient (cm^2/s).

The SiC PiN diode exhibits different characteristics due to its thinner, more highly doped base, as compared to Si PiN diodes. The higher doping in the base region, along with the lower activated doping in the emitter (due

to deeper impurity levels in SiC) results in emitter-recombination current dominating forward conduction at lower current densities than in Si devices. The net effect of the increased emitter-recombination current is a saturation of the amount of stored charge in the voltage-blocking layer for high currents. The result of the emitter-recombination current can be seen in Fig. 4, where the total charge in the base (designated by the area under the current-time curve) stops increasing with increasing forward current. The lack of increase in base charge with increasing forward current indicates that the emitter-recombination current dominates forward conduction above 2 A in Fig. 4. The SiC diode model utilizes separately extractable diode model parameters for each region of forward conduction to predict the end region effects [8–10], i.e., a saturation current I_S, and ideality factor N, for depletion region recombination, low-level injection, high-level injection, and emitter-recombination currents. Each of these four regions of operation i_{reg} can then be described with unique I_S and N values in a diode equation of the form

$$i_{reg} = I_S(e^{V_j/NV_t} - 1), \quad (4)$$

where V_t is the thermal voltage and V_j is the junction voltage. Model parameters are listed in [8] for different SiC power diode technologies.

Fig. 5 shows the measured on-state characteristics for a PiN diode, and the model output with the high-level injection current i_o and the emitter-recombination current i_e combining to comprise the total diode model current i_d. The combination of i_o and i_e provide the correct reverse recovery response to the forward conduction characteristics.

The larger band gap in SiC (3.26 eV for 4H–SiC [5] versus 1.1 eV for Si) results in lower values of the intrinsic carrier concentration and hence lower saturation current values I_S as compared to Si. Depending on the respective ideality factors N, values of SiC diode saturation currents can be approximately 36 orders of magnitude smaller than those found in Si diodes. For compact modeling, the extraction of the ideality factor and bounding methods must be such that the simulator is able to converge utilizing such small values.

The larger bandgap also yields devices that have the potential to operate reliably at much higher temperatures than their Si counterparts (300 °C for SiC versus 150 °C for Si). To ensure that the on-state characteristics are valid over the increased range of operating temperatures, the temperature dependence of the saturation currents in the SiC power diode model must be properly described to model the reduction in on-state voltage with increasing temperature. To describe the diode

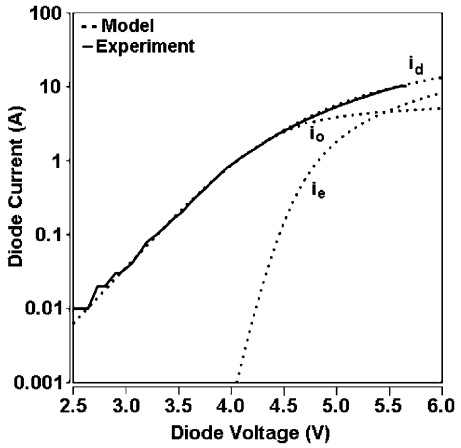

Fig. 5. Measured (solid) and simulated (dashed) SiC 5 kV, 5 A PiN diode on-state curves at 25 C demonstrating the forward diode current i_d, the high-level injection base current i_o, and the emitter-recombination current i_e.

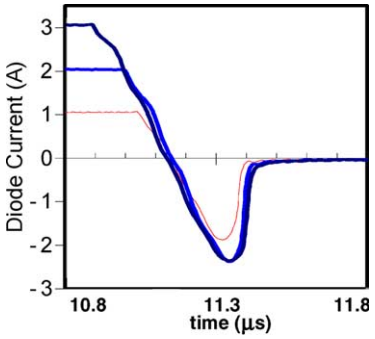

Fig. 4. SiC 10 kV, 20 A PiN measured diode reverse recovery waveforms versus forward current demonstrating emitter-recombination effects on reverse recovery.

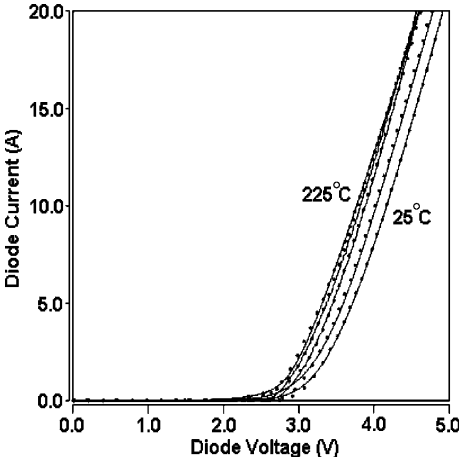

Fig. 6. SiC 5 kV, 5 A PiN diode measured (solid) and simulated (dashed) on-state characteristics from 25 to 225 °C in 50 °C increments.

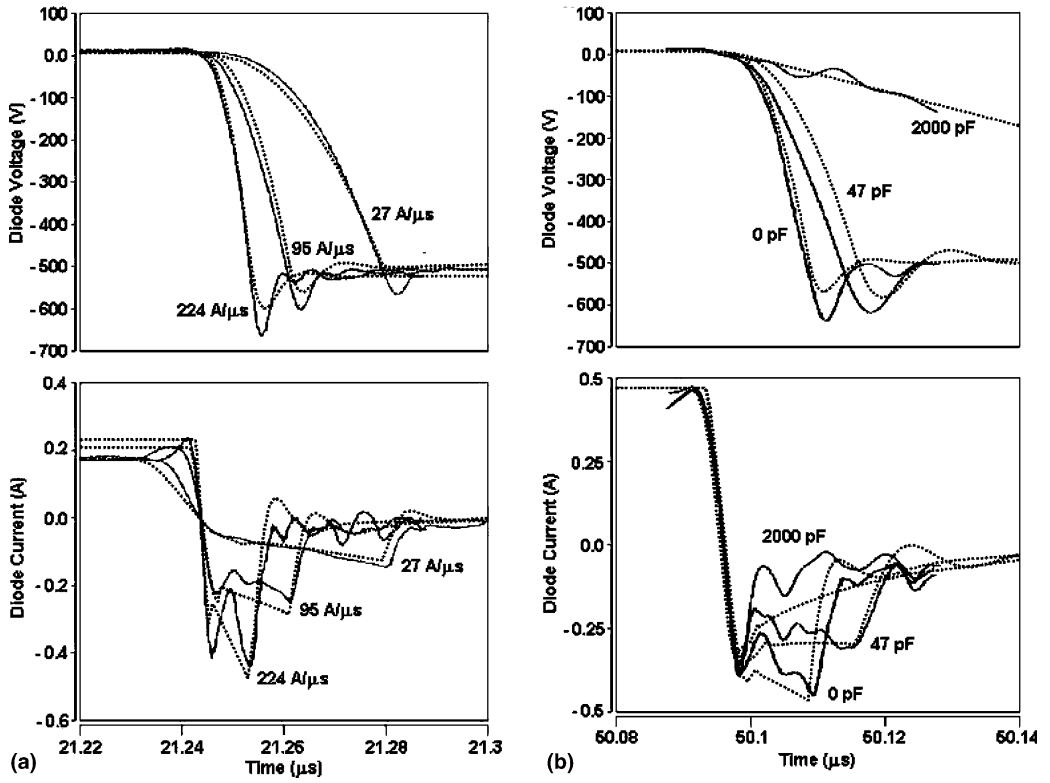

Fig. 7. SiC 5 kV, 0.4 A PiN diode measured (solid) and simulated (dashed) switching waveforms for (a) various d/d*t*'s and (b) d*v*/d*t*'s.

saturation current over a wide range of temperatures, the temperature-dependent intrinsic carrier concentration and bandgap expressions are combined to form one expression for the saturation current as a function of temperature. The expression is implemented to describe the temperature dependence of SiC PiN, Schottky, and merged-PiN-Schottky (MPS) diodes [8]. The results of using the temperature-dependent expression for a SiC 5 kV, 5 A PiN diode are shown in Fig. 6.

Fig. 7 demonstrates the transient operation of the diode model for a SiC 5 kV, 0.25 A PiN diode under various d*i*/d*t* and d*v*/d*t* conditions at turn-off. In the reverse recovery measurements of Fig. 7, an initial forward current is applied to the diode, then it is switched by applying a constant negative d*i*/d*t* [8].

3. Conclusion

In order to accurately predict device characteristics over a wide range of application conditions, a physics-based modeling approach is used to model SiC power devices. Different structural properties, such as a thinner and more highly doped base region, or material properties, such as carrier mobility and bandgap, result in different compact model expressions as compared to silicon technology.

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References

[1] Hefner AR, Singh R, Lai JS, Berning DW, Bouche S, Chapuy C. SiC power diodes provide breakthrough performance for a wide range of applications. IEEE Trans Power Electron 2001;16:273–80.
[2] Ryu SH, Agarwal A, Richmond J, Palmour J, Saks N, Williams J. 27 mΩ cm^2, 1.6 kV power DiMOSFETs in 4H–SiC. In: Proc of the Int Symp on Power Semiconductor Devices (ISPSD). Santa Fe, NM, June 2002.
[3] Cree, Inc., 4600 Silicon Dr., Durham, NC, 27703. part # CSD20060, datasheet CSD20060. rev. D.
[4] Infineon Technologies AG. P.O. Box 80 09 49, D-81609 Muenchen, Germany, part # SDD04S60, datasheet 2001-12-04.

[5] Wright NG, Morrison DJ, Johnson CM, O'Neill AG. Electrothermal simulation of 4H–SiC power devices. Mater Sci Forum 1998;264–268:917–20.
[6] McNutt T, Hefner A, Mantooth A, Berning D, Ryu SH. Silicon carbide power MOSFET model and parameter extraction sequence. In: Proc IEEE Power Electronics Specialists Conf (PESC). Acapulco, Mexico. June 2003. p. 217–26.
[7] Hefner A. An investigation of the drive circuit requirements for the power insulated gate bipolar transistor (IGBT). IEEE Trans Power Electron 1991;6(2):208–19.
[8] McNutt T, Hefner A, Mantooth A, Duliere J, Berning D, Singh R. SiC PiN, Schottky, and MPS power diode models implemented in the Saber circuit simulator. IEEE Trans Power Electron 2004;19(3).
[9] McNutt T, Hefner A, Mantooth A, Duliere J, Berning D, Singh R. Parameter extraction sequence for SiC Schottky, merged PiN Schottky, and PiN power diode models. IEEE Power Electronics Specialists Conf (PESC). Cairns, Australia, June 2002. p. 1269–76.
[10] Mantooth A, Duliere J. A unified diode model for circuit simulation. IEEE Trans Power Electron 1997;12(5):816–23.