Silicon Carbide PiN and Merged PiN Schottky Power Diode Models Implemented in the Saber Circuit Simulator

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***Abstract*—Dynamic electrothermal circuit simulator models are developed for silicon carbide power diodes. The models accurately describe the temperature dependence of on-state characteristics and reverse-recovery switching waveforms. The models are verified for the temperature dependence of the on-state characteristics, and the di/dt, dv/dt, and temperature dependence of the reverse-recovery characteristics. The model results are presented for 1500 V SiC Merged PiN Schottky (MPS) diodes, 600 V Schottky diodes, and 5000 V SiC PiN diodes. The devices studied have current ratings from 0.25 A to 5 A and have different lifetimes resulting in different switching energy versus on-state voltage tradeoffs. The devices are characterized using a previously reported test system specifically designed to emulate a wide range of application conditions by independently controlling the applied diode voltage, forward diode current, di/dt, and dv/dt at turn-off. A behavioral model of the test system is implemented to simulate and validate the models. The models are validated for a wide range of application conditions for which the diode could be used.**

***Index Terms*—Circuit simulation, diode model, merged PiN Schottky, PiN, power diode, reverse recovery, Schottky, SiC.**

I. Introduction

ALMOST ALL circuit simulators contain library parts for various commercially available silicon (Si) devices, but there has yet to be a commercially available silicon carbide (SiC) device library component. This is largely due to the fact that SiC devices are just beginning to emerge. The first generation of these new SiC devices includes Merged PiN Schottky (MPS), Schottky, and PiN power diodes. These devices have been compared to similarly rated silicon devices and proved to provide significant performance advantages for on-state characteristics, reverse recovery characteristics, temperature dependence, power converter efficiency, and electromagnetic interference [1].

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In this paper, dynamic electrothermal circuit simulator models are developed based on the Mantooth unified diode model available in the Saber® circuit simulator [2], [3]. These models are used to describe the characteristics of several prototype 4H-SiC power diodes. Model results will be presented here for:

a) a 0.5 A (0.0045 cm^2), 1500 V SiC MPS diode;
b) a 0.25 A (0.002 cm^2), 5 kV SiC PiN;
c) a 1 A (0.009 cm^2), 600 V SiC Schottky diode;
d) a 5 A (0.04 cm^2), 5 kV SiC PiN diode.

The models are validated against the on-state characteristics versus temperature as well as a wide range of switching conditions that could occur in various applications.

II. Background

SiC power devices are expected to show superior performance compared to devices made with other semiconductors. This is primarily because 4H-SiC has an order of magnitude higher breakdown electric field ($\sim 2.2 \times 10^6$ V/cm) to (4×10^6 V/cm) and higher temperature capability than conventional Si materials [1]. The higher breakdown electric field allows the design of SiC power devices with thinner (0.1 times that of silicon devices) and more highly doped (more than 10 times higher) voltage-blocking layers. For majority carrier power devices such as power Schottky diodes, the combination of 0.1 times the blocking layer thickness with 10 times the doping concentration can yield a SiC device with a factor of 100 advantage in resistance compared to that of Si majority carrier devices. For minority carrier conductivity modulated devices such as the PiN diode, a blocking layer of 0.1 times the thickness of a Si device can result in a factor of 100 faster switching speed. This is possible because the diffusion length, L, required to modulate the conductivity of the blocking layer can also be reduced to $1/10$th the value required for Si, thus permitting the reduction of the lifetime, τ, by a factor of 100 according to $L = \sqrt{D\tau}$, where D is the diffusion coefficient. Because SiC has a larger band gap (3.26 eV for 4H-SiC [4] versus 1.1 eV for Si), SiC devices have the potential to operate reliably at much higher temperatures than their Si counterparts (300 °C for SiC versus 150 °C for Si).

Recently, new power semiconductor devices have begun to emerge that utilize the advantages of SiC. Because power rectifiers are more easily produced than three terminal

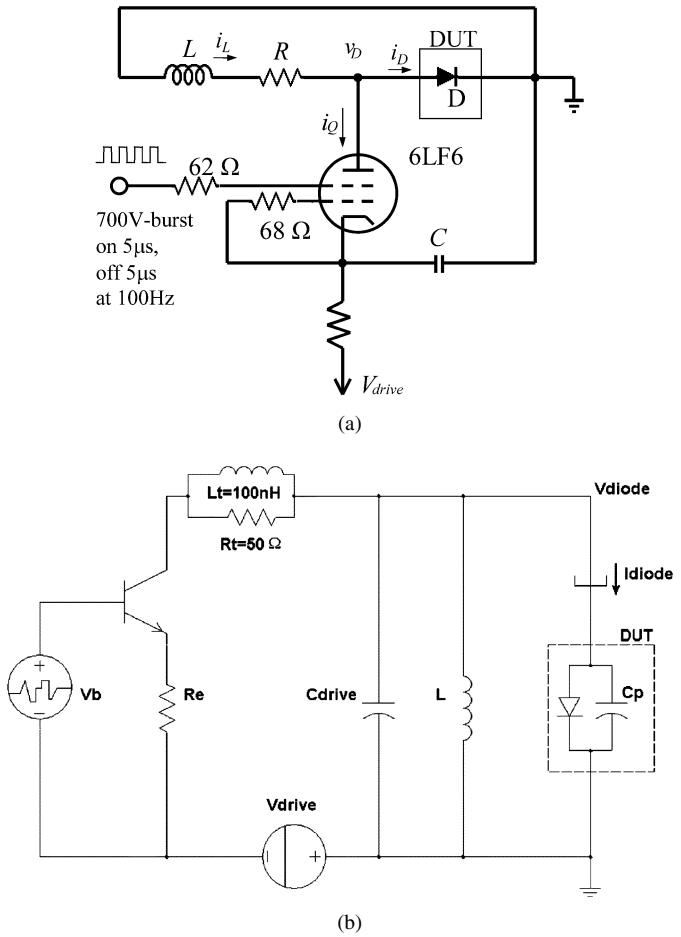

Fig. 1 (a) Circuit diagram for the high-speed diode reverse recovery test system. (b) Behavioral equivalent circuit used to emulate the test system of Fig. 1(a).

power-switching devices, they are the first SiC electronic components available for commercial application [5], [6]. Generally speaking, there are three classes of SiC power rectifiers:

a) Schottky diodes, which offer extremely high switching speed but have higher leakage current and higher blocking layer resistance than SiC p-n junction diodes;
b) PiN diodes, which offer low leakage current but show reverse recovery charge during switching and have a large junction forward voltage drop due to the wide band gap of SiC;
c) Merged PiN Schottky (MPS) diodes, which offer Schottky-like on-state and switching characteristics, and PiN-like off-state characteristics [7].

It has been shown that a 1500 V SiC MPS diode provides superior performance over Si diodes with voltage ratings of 600 V to 1500 V [8], and that a SiC PiN diode has superior performance compared to Si diodes with voltage ratings from 1200 V to 5000 V [1].

III. Reverse Recovery Test System

Fig. 1(a) shows the test circuit used for characterizing the diodes for reverse recovery, and Fig. 1(b) shows the behavioral representation including parasitic elements used for diode model validation. It is important to note that the test circuit in Fig. 1(a) is well-characterized, meaning that the values of all circuit components and parasitic elements are known. To operate the test circuit in Fig. 1(a), first the vacuum tube is turned on to establish the test current i_L in the inductor L. Once the test current is reached, the tube is ramped off and the inductor current is commutated to the Device Under Test (DUT). To initiate the reverse recovery test, the tube is ramped on with a well-controlled di_Q/dt at the tube anode. This results in a negative di_D/dt being applied to the DUT. As the diode begins to recover the diode voltage v_D rises toward the power supply voltage $V_{\rm drive}$ completing the recovery test.

The circuit of Fig. 1(a) uses a 6LF6 vacuum tube as a driver device in place of the usual MOSFET to achieve low parasitic capacitance at the DUT anode and an extremely fast switching speed. The 51 Ω resistor R isolates the DUT from the parasitic capacitance of the 30 mH inductor L and is also used to quickly reset the inductor current to zero after each test. The dv/dt of the square wave applied to the tube screen is varied to achieve different di_D/dt values for the DUT. With a 700-V peak drive to the screen grid of the tube, the circuit can test over 12 A of combined forward and reverse DUT current, and the applied voltage to the DUT can be up to 2000 V. For higher current drive capability, a similar 50-A, 5000-V reverse recovery test system is used.

The reverse recovery tests are performed for various values of forward diode current i_D, diode reverse bias power supply voltage $V_{\rm drive}, di_D/dt$, and dv_D/dt, where dv_D/dt is controlled by placing various driver capacitors across the DUT. By independently controlling $V_{\rm drive}, di_D/dt, dv_D/dt$, and the forward diode current at turn-off the test circuit enables testing of SiC diodes for the full range of conditions that occur for various application conditions. Varying the value of $V_{\rm drive}$ emulates the application conditions for circuits with different DC bus voltages, varying the value of di_D/dt emulates the application conditions of different speed anti-parallel switching devices, and varying the value of dv_D/dt emulates the application conditions of using anti-parallel switching devices of different output capacitance. Also, varying the value of dv_D/dt aids in the determination of the portion of the diode reverse recovery due to charge storage and the portion due to device capacitance. Varying the value of the forward diode current at turn-off aids in the determination of the portion of current that is due to emitter recombination and the portion that contributes to charge storage.

The behavioral representation of the test circuit, Fig. 1(b), uses an ideal bipolar transistor model with an emitter follower resistor, R_e, to emulate the di_D/dt applied by the tube. The bipolar transistor model capacitance parameters are set to zero and replaced by the 40 pF output capacitance of the tube [combined with $C_{\rm drive}$ in Fig. 1(b)]. The next most important parasitic elements of the test circuit are the 100 nH tube inductance L_t and the 50 Ω tube resistance R_t that result in a small voltage overshoot near the end of the diode current recovery waveform. The inductor L remains at 30 mH as in Fig. 1(a). The pulse width of the signal generator V_b is varied to determine the forward current for the reverse recovery test, and the rise time of V_b determines the di_D/dt applied to the DUT at turn off.

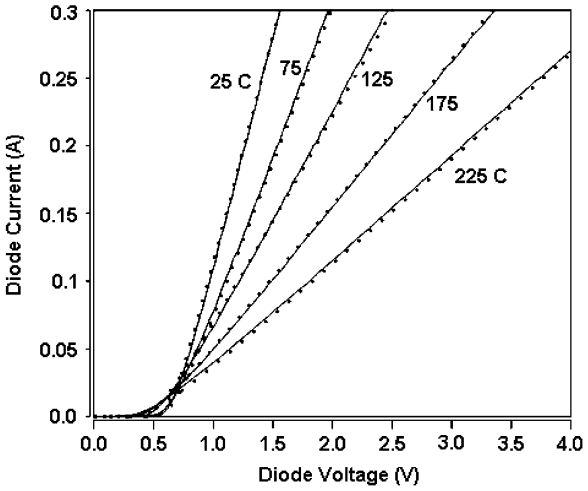

Fig. 2. Simulated (dashed) and measured (solid) on-state characteristics for the 1500 V, 0.5 A SiC MPS diode.

IV. SiC Compact Model for Circuit Simulation

In this section, a new model is presented for SiC PiN and Schottky diodes. The model is capable of describing PiN, Schottky, and Merged-PiN-Schottky (MPS) diodes for a wide range of device types and circuit conditions including forward-bias, reverse recovery, and temperature dependence. The SiC diode model is based on the Mantooth unified diode model available in the Saber circuit simulator, which was modified to include SiC material parameters and to represent unique features of SiC diodes.

To accurately describe the on-state and transient characteristics of the power diodes, the model uses two forms of the diode equation. First, the most widely known form

$$i = \mathrm{IS}(e^{V_j/N\cdot V_T} - 1) \tag{1}$$

where IS is the saturation current, V_j is the forward diode junction voltage, N is the emission coefficient, and V_T is the thermal voltage, is used for depletion region recombination (ISR, NR) and emitter or end region recombination (ISE, NE). Equations similar to (1) are also used for the high- and low-level base injection currents, unless both conditions apply, then the equations are coupled to provide better continuity and flexibility in characterization

$$i_0 = \frac{2i_L}{1 + \left[1 + \left(2\frac{\mathrm{ISL}}{\mathrm{ISH}}\right)^{N_{\mathrm{eff}}} e^{V_j/V_T}\right]^{1/N_{\mathrm{eff}}}} \tag{2}$$

where

$$N_{\mathrm{eff}} = \frac{1}{\frac{1}{\mathrm{NL}} - \frac{1}{\mathrm{NH}}}. \tag{3}$$

In (2), i_L is the low level injection current that takes the form of (1), and ISL, ISH, NL, and NH are the saturation currents for the low- and high-level injection regions and the corresponding emission coefficients, respectively. The value of i_0 is the current value used in calculating the total injected charge, q_0. The injected charge is calculated using

$$q_0 = \mathrm{TT}\cdot i_0 \tag{4}$$

where TT is base charge decay parameter. This implementation accounts for the fact that the stored charge in the base results from the base charge injection current i_0 and not from the depletion region, end region, or emitter region recombination currents. The charge, q_0, is then distributed to constitute a two time constant response or *double-tau model*: Q_{SW0}, the portion that is removed via sweep-out effects, and Q_{R0}, the portion that recombines or diffuses out of the drift zone. To divide the charge, the model parameter *ALPH*0 is invoked as

$$Q_{\mathrm{SW0}} = \mathrm{ALPH0}\cdot q_0 \quad \text{and} \tag{5}$$

$$Q_{R0} = (1 - \mathrm{ALPH0})\cdot q_0. \tag{6}$$

The model parameters TSW and TM control the nonquasistatic charge sweep out effect and the nonquasistatic diffusion effect, respectively.

TT, TSW, and TM can be varied according to temperature through relationships of the form

$$\mathrm{TT}(T) = \mathrm{TT}(T_{\mathrm{nom}})\cdot\left(\frac{T}{T_{\mathrm{nom}}}\right)^{\beta} \tag{7}$$

where each time constant possesses a unique β and the model parameters are defined at a nominal temperature, T_{nom}. The forward-biased saturation currents available in the model are also a function of temperature. Their relationships have the following form:

$$\mathrm{IS}(T) = \mathrm{IS}(T_{\mathrm{nom}})\cdot\left(\frac{T}{T_{\mathrm{nom}}}\right)^{\mathrm{XTI}}\cdot e^{[(T/T_{\mathrm{nom}})-1]\cdot(\mathrm{EG}/\mathrm{NT}\cdot V_T)} \tag{8}$$

where XTI is the saturation current temperature exponent, EG is the temperature dependent barrier height or energy gap, NT is the technology-dependent thermal multiplication factor, and V_T is the temperature dependent thermal voltage. For Schottky diode technologies, EG is set to the barrier height, but for p-n junction devices EG is set to the semiconductor energy gap.

The temperature dependence of the forward series contact resistance, RS, implemented to provide greater flexibility in describing the series resistance due to the device and package effects, is given by

$$\mathrm{RS}(T) = \mathrm{RS}(T_{\mathrm{nom}})\cdot((1/T_{\mathrm{nom}})^{\gamma}T^{\gamma} + \mathrm{TRS1}(T - T_{\mathrm{nom}}) + \mathrm{TRS2}(T - T_{\mathrm{nom}})^2) \tag{9}$$

where γ is the exponential temperature parameter, TRS1 is the linear temperature parameter, and TRS2 is the quadratic temperature parameter.

In order to properly model SiC devices over a wide range of temperatures, it is necessary to incorporate the temperature dependence of the bandgap and carrier mobilities. The temperature dependence of the bandgap is of the form [9]

$$\mathrm{EG}(T) = \mathrm{EG}(T_{\mathrm{nom}}) - 3.3\cdot 10^{-3}\cdot(T - 300K) \tag{10}$$

and the temperature dependence of the carrier mobilities are of the following form:

$$\mu_n(T) = \frac{\mathrm{MUN}}{1 + \left(\frac{N_A+N_D}{1.94\cdot 10^{17}}\right)^{0.61}}\cdot\left(\frac{T}{T_{\mathrm{nom}}}\right)^{-2.15} \quad \text{and} \tag{11}$$

$$\mu_p(T) = 15.9 + \frac{\mathrm{MUP}}{1 + \left(\frac{N_A+N_D}{1.76\cdot 10^{19}}\right)^{0.34}}\cdot\left(\frac{T}{T_{\mathrm{nom}}}\right)^{-2.15} \tag{12}$$

TABLE I
SiC POWER DIODE MODEL PARAMETERS

Parameter	Parameter Name	0.25 A PiN	0.5 A MPS	5 A PiN	1 A Schottky
EG	Bandgap / Barrier Height	3.2	1.6	3.2	1.6
VJ	Built-in junction potential	2.8	1.2	2.8	1.2
CJ0	Zero-bias junction capacitance	$15 \cdot 10^{-12}$	$30 \cdot 10^{-12}$	$300 \cdot 10^{-12}$	$35 \cdot 10^{-12}$
M	P-N grading coeff.	0.5	0.5	0.5	0.5
FC	Forward-bias depletion capacitance coeff.	0.5	0.5	0.5	0.5
RS	Forward series contact resistance	7	2.85	$67 \cdot 10^{-3}$	0.32
ISR	Low-level recombination saturation current	$4.6 \cdot 10^{-7}$	$4.26 \cdot 10^{-13}$		$4 \cdot 10^{-18}$
NR	Low-level recombination emission coeff.	15	1		1
ISH	High-level injection saturation current	$3 \cdot 10^{-43}$		$3.4 \cdot 10^{-7}$	
NH	High-level injection emission coeff.	2		8	
ISE	Emitter recombination saturation current			$1.5 \cdot 10^{-30}$	
NE	Emitter recombination emission coeff.			2	
TT	Base charge decay parameter	$20 \cdot 10^{-9}$		$150 \cdot 10^{-9}$	
ALPH0	Initial value for voltage dependency of reverse recovery model				
TSW	Charge sweep out time				
TM	Mid-region recombination time	$5 \cdot 10^{-6}$		$100 \cdot 10^{-9}$	
XTIR	*ISR* temperature exponent	0.1	11.1		16
XTIH	*ISH* temperature exponent	11.4		0.1	
XTIE	*ISE* temperature exponent			17	
NTR	*ISR* thermal multiplication factor	23	2.1		1.5
NTH	*ISH* thermal multiplication factor	1		6.2	
NTE	*ISE* thermal multiplication factor			1.5	
TNR1	Linear *NR* temperature coeff.	$-2 \cdot 10^{-3}$			
TNR2	Quadratic *NR* temperature coeff.				
TRS1	Linear *RS* temperature coeff.	$-7.42 \cdot 10^{-3}$	$1.45 \cdot 10^{-3}$	$-10 \cdot 10^{-3}$	$-3.6 \cdot 10^{-3}$
TRS2	Quadratic *RS* temperature coeff.	$-17.9 \cdot 10^{-6}$	$46.7 \cdot 10^{-6}$	$-41.3 \cdot 10^{-6}$	$-12.4 \cdot 10^{-6}$
GAMMA	*RS* temperature exponent	2.21	2.93	3.11	1.61
BETA	*TT* temperature exponent	2.5		2.9	

where $N_{A,D}$ is the acceptor (A) and donor (D) concentration, and MUN and MUP default to their values given in [9], 947 cm^2/Vs and 108.9 cm^2/Vs, respectively.

V. SiC SCHOTTKY AND MPS DIODE RESULTS

The SiC MPS diodes studied in this work are designed such that the PiN diode does not turn on in normal forward bias operation. This type of operation is typically referred to as the Junction–Barrier–Schottky (JBS) diode mode. The PN junctions serve only to shield the Schottky barrier from high electric fields, thus preventing Schottky barrier lowering to reduce leakage current.

Fig. 2 shows the simulated (dashed) and measured (solid) on-state characteristics for the 1500-V, 0.5-A (0.0045-cm^2) SiC MPS diode for different temperatures in the range of 25 °C to 225 °C. In these curves, the built-in potential (on-voltage at low current) decreases with increasing temperature because the increasing thermal energy of electrons in the metal surmounts the Schottky barrier height at a lower forward voltage. The increase in current at a lower on-voltage results in a larger saturation current ISR at higher temperatures, thus requiring extraction of NTR, and XTIR over the temperature range of interest. The decrease in slope of the on-state curves with increasing temperature is indicative of the reduction of mobility with temperature for a majority carrier device. The temperature dependence of the series resistance requires extracting the model parameters γ, TRS1, and TRS2 in order to provide an accurate fit for the temperature dependence of the diode's forward series resistance. The extracted model parameters for each diode model are listed in Table I. The blank entries in Table I correspond to default parameter values.

For Figs. 3–5, the initial measured forward current is 0.6 A and the diode is switched by applying a constant negative di/dt with the tube. The tube current increases linearly until the voltage reaches the voltage supply value, $\mathrm{V_{drive}}$. In general, the negative tube current is supplied by the device minority carrier charge reverse recovery current, such as in the PiN diode, such as in the PiN diode, the capacitive current through the DUT junction capacitance, the DUT package capacitance $\mathrm{C_p}$, and the external driver capacitance $\mathrm{C_{drive}}$ (parasitic tube capacitance, plus added driver capacitance).

The voltage waveforms in Figs. 3 and 4 are determined by the rate that the tube current charges the driver capacitance and the DUT capacitance. In Fig. 3, the dv/dt is faster for the higher di/dt curve because the tube current reaches a larger negative value

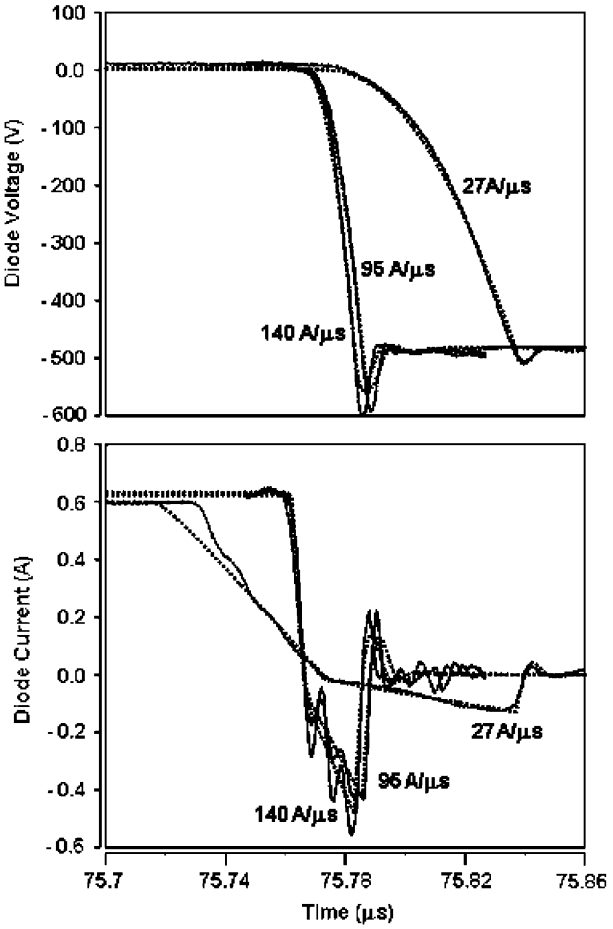

Fig. 3. Measured (solid) and simulated (dashed) reverse recovery waveforms of the 1500 V SiC MPS diode for three different di/dt values and no external driver capacitance.

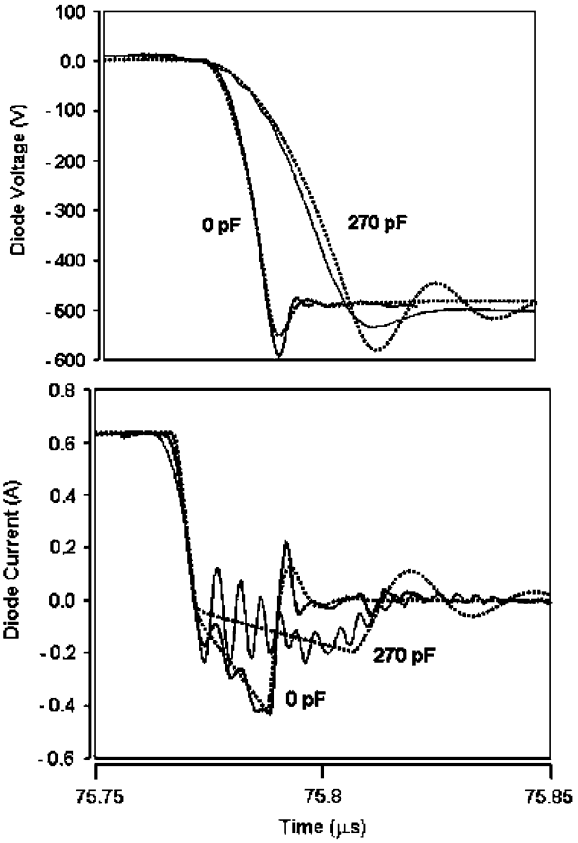

Fig. 4. Measured (solid) and simulated (dashed) reverse recovery waveforms of the 1500 V SiC MPS diode for two different values of external driver capacitance C_{drive}.

during the voltage rise phase and thus charges the capacitance faster. In Fig. 4, the added driver capacitance reduces the diode dv/dt since the tube current charges the additional external driver capacitance.

The instantaneous diode capacitance can be calculated from these waveforms by dividing the instantaneous reverse current by the dv/dt value. For example, the high di/dt curve in Fig. 3 (di/dt equal to 95 A/μs) has a maximum dv/dt equal to 60 V/ns and the maximum reverse current is 0.2 A at this point. Using these values, the capacitance is calculated to be 3.3 pF when the reverse voltage is equal to several hundred volts. This value is a combination of the junction depletion capacitance and the package parasitic capacitance.

The results of Figs. 3–5 show reverse recovery waveforms that demonstrate the wide range of applications for which the new SiC power diode model can be applied. Fig. 3 shows the measured (solid) and simulated (dashed) reverse recovery waveforms of the MPS diode for three different di/dt values and no external driver capacitance. Fig. 4 shows the measured (solid) and simulated (dashed) reverse recovery waveforms for the same di/dt but with two different values of external driver capacitance, C_{drive}. Fig. 5 shows the measured (solid) and simulated (dashed) reverse recovery waveforms versus temperature for a di/dt of 95 A/μs and no external driver capacitance.

From Figs. 3–5 one can conclude that the MPS reverse recovery is capacitive in nature and does not have a minority carrier charge storage time. This conclusion is reached by observing that the reverse voltage rise occurs during the entire reverse current period and the reverse recovery waveforms do not vary with temperature. In the MPS diode model, the above on-state characteristics are modeled with the depletion region recombination current component (ISR, NR) that does not contribute to the calculation of stored base charge q_0, since the MPS diode operates in the JBS mode. Thus, the MPS model provides the correct reverse recovery response, one that is capacitive in nature with no minority carrier charge storage. The diode junction capacitance is modeled using the typical diode junction capacitance parameters CJO, FC, and M as shown in [10].

The SiC Schottky model scales well with device area. Fig. 6 shows the measured (solid) and simulated (dashed) on-state characteristics for the 600-V, 1-A SiC Schottky diode for different temperatures in the range of 25 °C to 175 °C. Again, the built-in potential decreases with increasing temperature because the increasing thermal energy of electrons in the metal surmounts the Schottky barrier height at a lower forward voltage. The decrease in slope of the on-state voltage curves with increasing temperature is indicative of the reduction of mobility with temperature for a majority carrier device. Fig. 7 shows the measured (solid) and simulated (dashed) reverse recovery waveforms of the 600-V, 1-A SiC Schottky diode for two different di/dt values and no external driver capacitance.

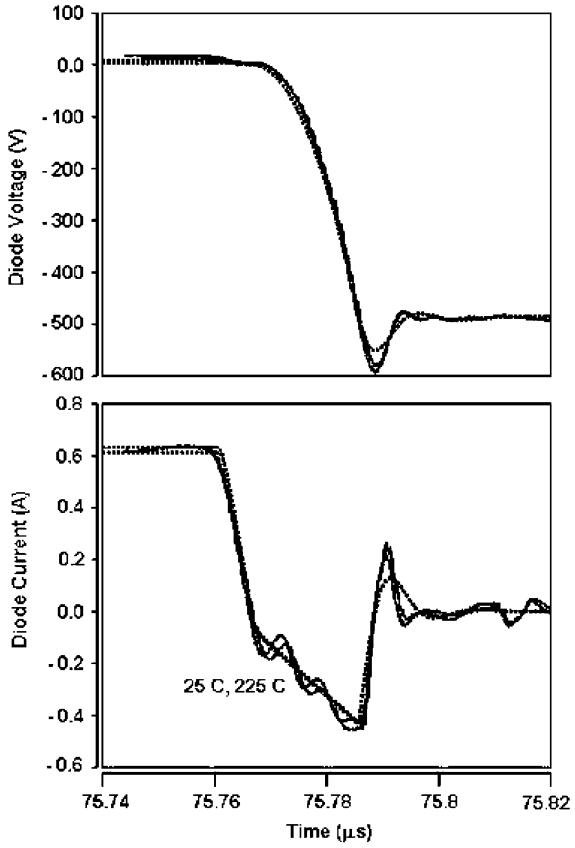

Fig. 5. Measured (solid) and simulated (dashed) reverse recovery waveforms at 25 C and 225 C for a di/dt of 95 A/μs and no external driver capacitance.

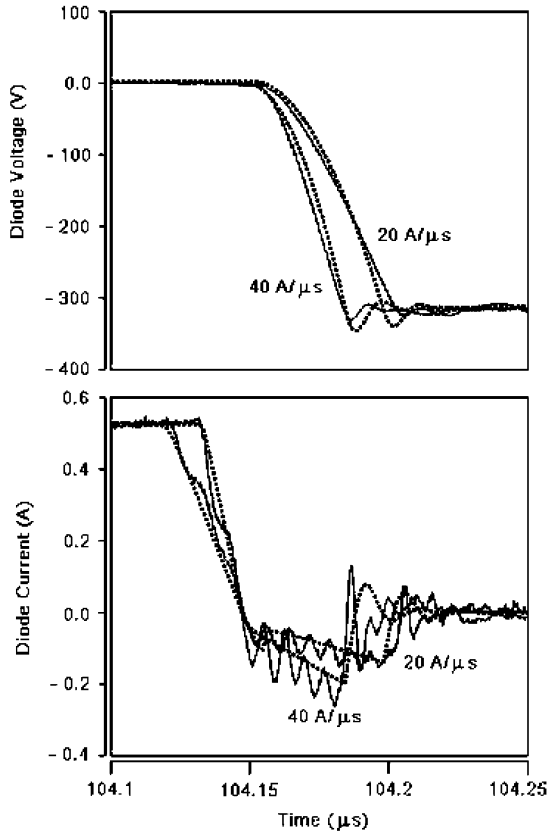

Fig. 7. Measured (solid) and simulated (dashed) reverse recovery waveforms of the 600 V, 1 A SiC Schottky diode for two different di/dt values and no external driver capacitance.

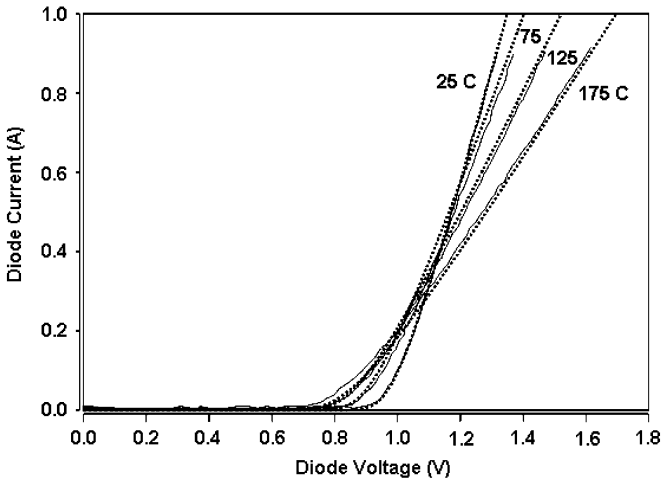

Fig. 6. Measured (solid) and simulated (dashed) on-state characteristics for the 600 V, 1 A SiC Schottky diode.

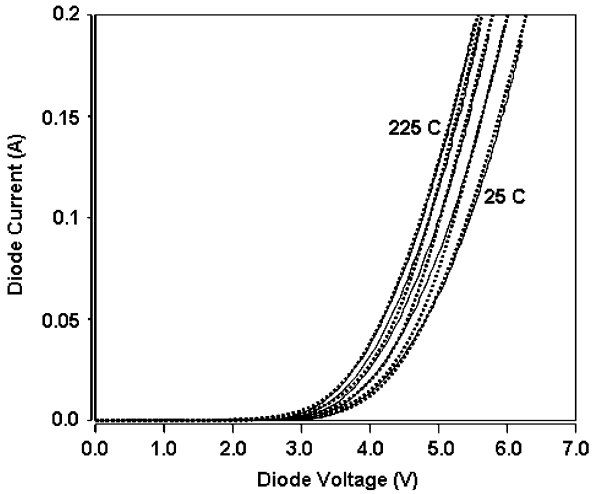

Fig. 8. Measured (solid) and simulated (dashed) on-state characteristics for the 5 kV, 0.25 A SiC PiN diode.

VI. SiC PiN Diode Results

Fig. 8 shows the simulated (dashed) and measured (solid) on-state characteristics for the 5000-V, 0.25-A SiC PiN diode for different temperatures in the range of 25 to 225 °C. Because the bandgap for 4H-SiC is 3.26 eV, the built-in potential for the SiC PiN diode is nearly 3 V. The decrease in on-state voltage with temperature is indicative of the decrease in built-in potential with increasing temperature and the increase in lifetime with temperature for conductivity modulated devices.

The SiC PiN model is capable of modeling both the decrease in built-in potential and the increase in lifetime by providing the user with temperature parameters for carrier lifetimes (BETA)

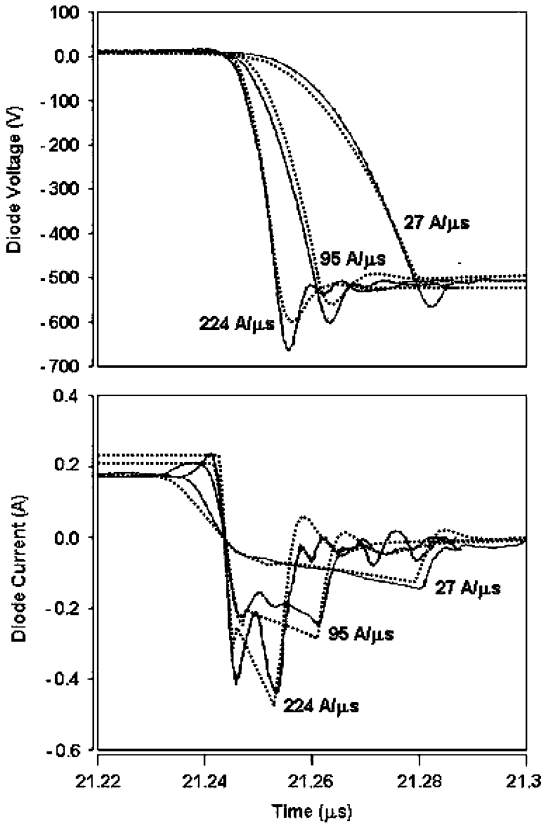

Fig. 9. Measured (solid) and simulated (dashed) reverse recovery waveforms of the 5 kV SiC PiN diode for three different di/dt values and no external driver capacitance.

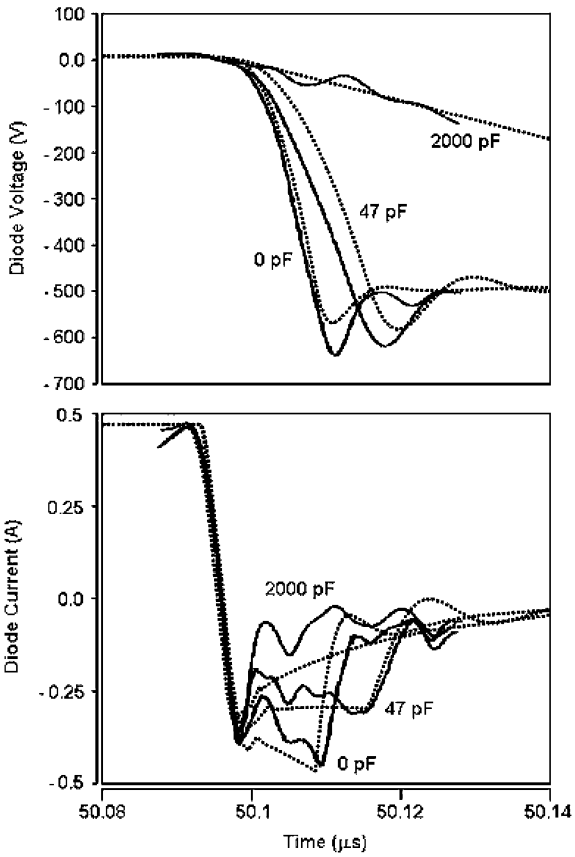

Fig. 10. Measured (solid) and simulated (dashed) reverse recovery waveforms for the same di/dt but with three different values of external driver capacitance C_{drive}.

and saturation currents (XTI). The model also accounts for depletion region, end region, and emitter region recombination effects. For the PiN diode on-state curves shown in Fig. 8, the depletion region recombination current component (ISR, NR) was utilized to model the low current region of operation (below 0.05 A) and the high-level injection current component (ISH, NH) was utilized to model the high current region of operation. The emitter recombination component (ISE, NE) was not utilized to model the PiN diode on-state in Fig. 8, as the emitter recombination effect did not dominate forward conduction until over 0.8 A.

The reverse recovery switching tests are performed using the same techniques for controlling di/dt and dv/dt as discussed in the previous section. Fig. 9 shows the measured (solid) and simulated (dashed) reverse recovery waveforms of the 5000 V SiC PiN diode for three different di/dt values and no external driver capacitance. For the lowest value of di/dt (27 A/μs), the reverse recovery current is determined by the device capacitance, whereas a stored charge recovery peak becomes more evident as the di/dt is increased (i.e., 95 A/μs and 224 A/μs curves).

Fig. 10 shows the measured (solid) and simulated (dashed) reverse recovery waveforms for the same di/dt, but with three different values of external driver capacitance C_{drive}. As the driver capacitance is increased from 0 pF to 2000 pF, the voltage rate of rise is decreased and the internal diode capacitance current is reduced. For the case where no driver capacitance was added, the reverse current waveform consists of a stored charge recovery portion followed by the capacitive portion. For the case of the highest driver capacitor value ($C_{drive} = 2000$ pF), dv/dt is substantially reduced and the current required to charge the internal diode capacitance is minimal. Thus, the waveforms consist of a

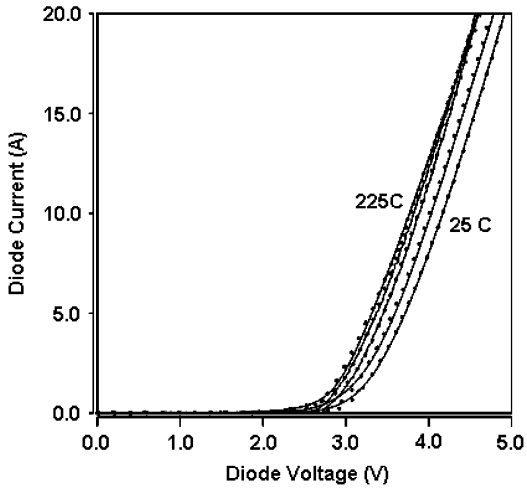

Fig. 11. Measured (solid) and simulated (dashed) on-state characteristics for the 5 kV, 5 A SiC PiN diode.

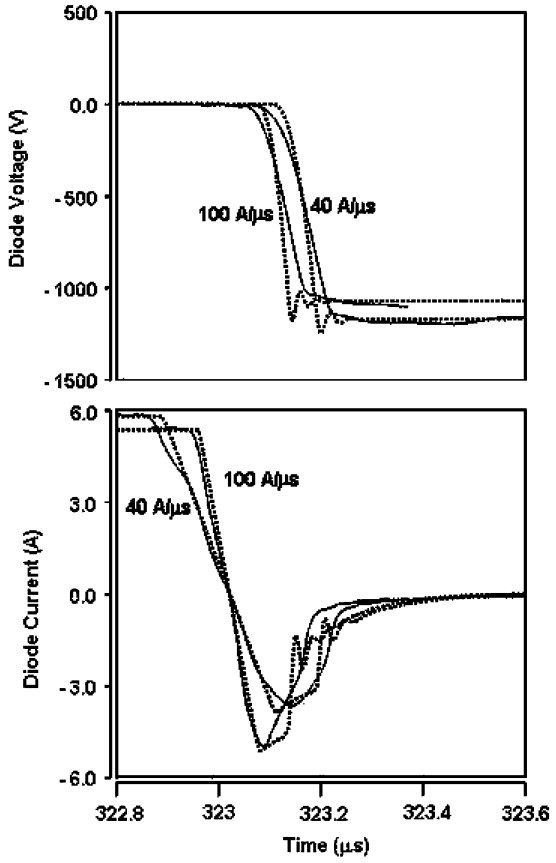

Fig. 12. Measured (solid) and simulated (dashed) reverse recovery waveforms of the 5 kV, 5 A SiC PiN diode for two different di/dt values and no external driver capacitance.

stored charge recovery portion followed by a small current tail due to the decay of the remaining stored charge.

The SiC PiN model scales well with device area and current rating. The measured temperature dependence of the on-state characteristics for the 5–kV, 5–A (0.04–cm^2) rated SiC PiN diode is shown in Fig. 11. Fig. 12 shows the measured (solid) and simulated (dashed) reverse recovery waveforms of the 5 kV, 5 A SiC PiN diode for two different di/dt values and no external driver capacitance. The decrease in on-state voltage of Fig. 11 with temperature is indicative of the increase in lifetime with temperature for a conductivity modulated device, and a decrease in bandgap of the PN junction. However, at a high temperature of 225 °C, a reduction in carrier mobility starts to increase the differential on-resistance across the drift layer. This leads to a crossover in the I-V characteristics at a high current density of 20 A (500 A/cm^2) between the 175 °C and the 225 °C curves. In the entire 25 °C to 225 °C range, the on-state voltage drop changes by less than 0.4 V range. This small change with temperature demonstrates that the SiC diodes are stable with temperature and are easily paralleled.

For the PiN diode on-state curves shown in Fig. 11, the high-level injection current component (ISH, NH) was utilized to model the low and mid-current regions (below 6 A) of operation, while the emitter recombination component (ISE, NE) was utilized to model the high current regions of operation of the PiN diode. The emitter recombination effects dominated conduction at 6 A of forward current.

VII. Conclusion

A new compact circuit simulator model has been developed for 4H silicon carbide PiN, Schottky, and Merged-PiN-Schottky (MPS) power diodes. The model has been validated against the on-state characteristics' temperature dependence and reverse recovery characteristics' di/dt, dv/dt, and temperature dependence. The validation was performed using a well-characterized test system that enables independent variation of each of the test circuit conditions. The model accurately describes the SiC MPS, PiN, and Schottky diodes for a wide range of test circuit conditions and device areas.

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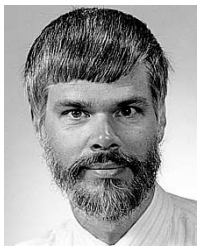

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Dr. Singh has served on the Technical committee of the International Symposium on Power Semiconductor Devices and IC's (ISPSD) in 2002 and 2003, and was part of a panel to develop a roadmap for the insertion of SiC based power devices into commercial applications.