Application of the Josephson Effect to Voltage Metrology

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Invited Paper

The unique ability of a Josephson junction to control the flow of magnetic flux quanta leads to a perfect relationship between frequency and voltage. Over the last 30 years, metrology laboratories have used this effect to greatly improve the accuracy of dc voltage standards. More recent research is focused on combining the ideas of digital signal processing with quantum voltage pulses to achieve similar gains in ac voltage metrology. The integrated circuits that implement these ideas are the only complex superconducting electronic devices that have found wide commercial application.

Keywords—*Digital–analog conversion, Josephson arrays, quantization, standards.*

I. INTRODUCTION

In 1962, B. Josephson, a graduate student at Cambridge University, Cambridge, U.K., derived equations for the current and voltage across a junction consisting of two superconductors separated by a thin insulating barrier [1]. His equations predicted that the current–voltage (*I–V*) curve for a junction that is current biased at frequency f will develop regions of constant voltage at the values $nhf/2e$, where n is an integer and e/h is the ratio of the elementary charge e to the Planck constant h. This prediction was verified experimentally by Shapiro [2] in 1963 and is now one of the foundations of metrology because it relates the volt to the second through a proportionality involving only fundamental constants.

Before proceeding with a review of Josephson standards, it is useful to review the International System of units (abbreviated SI) and the definitions of electrical quantities in that system [3]. The SI was established by the 11th General Conference on Weights and Measures (CGPM) in 1960. The CGPM is one of the international bodies created by the Treaty of the Meter in 1875. The SI meets the need for a worldwide set of units that is uniform and coherent. The ampere is the only electrical unit belonging to the seven base units of the SI. The ampere is defined as "*that constant current which, if maintained in two parallel straight conductors of infinite length, of negligible circular cross section, and placed 1 meter apart in vacuum, would produce between these conductors a force equal to* 2×10^{-7} *newtons per meter of length.*"

The volt, which is not a base unit, is defined through coherency of electrical power (current times voltage) and mechanical power (force times distance divided by time): "*The volt is that electromotive force between two points on a conductor carrying a constant current of 1 ampere when the power dissipated between the two points is 1 watt.*" Realization of the SI volt, therefore, depends on experiments that relate the ampere and the volt to the mechanical units of length, force, and power.

Modern instrumentation requires voltage measurements with a reproducibility that exceeds the uncertainty of the realization of the SI volt (currently 0.4 parts in 10^6). To meet this need, metrologists have developed artifacts and experiments that generate voltages that are stable and reproducible to a level approaching 0.001 parts in 10^6. These standards are said to *represent* the SI volt and serve as a kind of flywheel to remember the result of the realization of the SI volt. Before 1972, representations of the volt were made by assigning values to carefully stabilized banks of Weston cells. Drift and transportability problems with these electrochemical artifact standards limited the uniformity of voltage standards around the world to about 1 part in 10^6. This uniformity was dramatically improved when new standards based on Josephson's discovery were developed.

Josephson's equation for the supercurrent through a superconductive tunnel junction, now called the *dc Josephson effect*, is given by

$$I = I_c \sin\left[(4\pi e/h)\int V\,dt\right] \tag{1}$$

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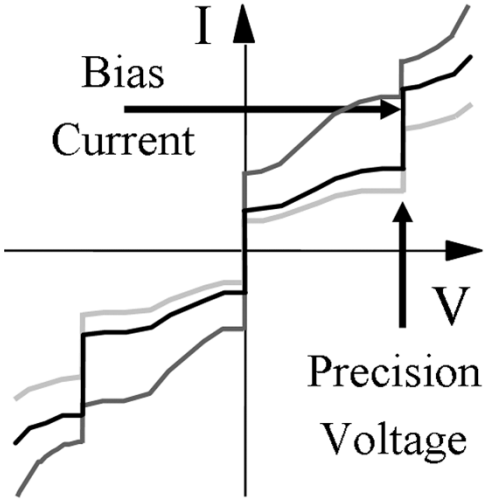

Fig. 1. *I–V* characteristics for three different junctions showing the same $n = 1$ constant-voltage step when biased with a common microwave frequency. The differences between these curves could occur from variations in microwave amplitude, the junction resistance, or the junction critical current, while the voltage step remains constant.

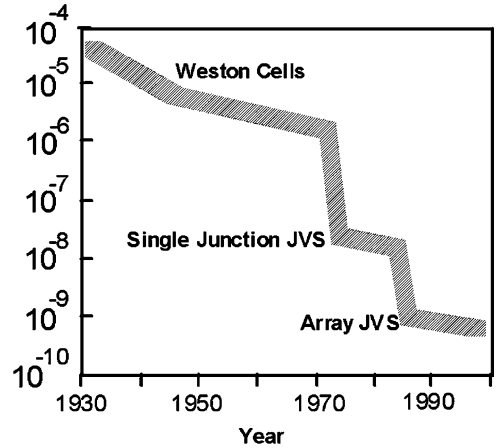

Fig. 2. The approximate level of agreement in dc voltage measurements among standards laboratories through the years 1930–2000.

where I is the junction current, I_c is the critical current, and V is the junction voltage. I_c is a function of the junction geometry, the temperature, and any magnetic field inside the junction. When a dc voltage is applied across the junction, (1) shows that the current will oscillate at a frequency $f_J = 2eV/h$, where $2e/h \approx 484$ GHz/mV. During each cycle of the oscillation, a single quantum of magnetic flux $(h/2e)$ passes through the junction. It is difficult to directly measure the small oscillation. However, if an ac current at frequency f is applied to the junction, there is a range of bias current for which the flow of flux quanta will phase lock to the applied frequency. Under this phase lock, the average voltage across the junction is precisely $hf/2e$. This effect, known as the *ac Josephson* effect, is observed as a constant voltage step at $V = hf/2e$ in the *I–V* curve of the junction, as shown in Fig. 1. It is also possible for the junction to phase lock to harmonics of f, which results in a series of steps at voltages $V = nf(h/2e)$, where n is an integer.

The Josephson effect was first used with existing Weston-cell voltage standards to improve the measurement of the constant $2e/h$. The uncertainty of these measurements was limited by the uncertainty of the SI volt realization and the stability of the Weston cells [4], [5]. The stability of the Josephson volt depends only on the stability of f, which can easily be one part in 10^{12}, and is much better than the stability of Weston cells. Thus, in the early 1970s, many national standards laboratories adopted a value for the Josephson constant $K_J = 2e/h$ and began using the ac Josephson effect as the practical standard of voltage [6], [7]. Owing to small differences in existing national standards, different values of K_J were adopted in different countries. This inconsistency was corrected in 1990 when, by international agreement, the constant $K_{\mathrm{J}-90}$ was assigned the value 483 597.9 GHz/V and adopted by all standards laboratories [8]. The assigned value is based on a weighted average of volt realization measurements made prior to 1990 at many national measurement institutions. The uncertainty in $K_{\mathrm{J}-90}$ is 0.4 parts in 10^6. Standards such as the Josephson volt and the quantum Hall resistance that depend on fundamental constants rather than physical artifacts are known as *intrinsic standards*.

Fig. 2 is a semilog plot that illustrates how the agreement in comparisons of dc voltage among National Measurement Institutes (NMIs) has improved over the last 70 years. The two major improvements coincide with the introduction of single-junction Josephson standards in the early 1970s and the introduction of series-array Josephson standards beginning in 1984. The first single-junction Josephson voltage standards (JVSs) generated very small voltages (1–10 mV). The output voltages were first increased by connecting up to about 20 junctions in series [9]. Larger series arrays were impractical at the time because junction nonuniformity required each junction to be individually biased. Fig. 1 shows how a variation in the electrical characteristics of three junctions requires individually adjusted bias currents to ensure that each junction is on a constant voltage step. Only in the last ten years has junction technology advanced to the point where series arrays of junctions with characteristics like that shown in Fig. 1 can produce practical output voltages (1–10 V) with a common bias current.

In 1977, Levinson *et al.* [10] made a suggestion that offered a solution to the junction-uniformity problem prevalent at that time. Levinson pointed out the importance of the parameter $\beta_c = 4\pi e I_c R^2 C/h$ in determining the characteristics of RF-induced Josephson steps. β_c is a measure of the damping of Josephson oscillations by the junction shunting resistance R. In particular, he showed that junctions with a large capacitance C and a large $R(\beta_c > 100)$ could generate a hysteretic *I–V* curve with constant-voltage steps like those shown in Fig. 3.

These steps are known as *zero-crossing steps* because they cross the zero-current axis of the *I–V* curve. The lack of stable regions between the first few steps means that, for small dc bias currents, the junction voltage must be quantized. With a common bias current at or near zero, the voltage across a large array of these junctions must also be quantized. A joint

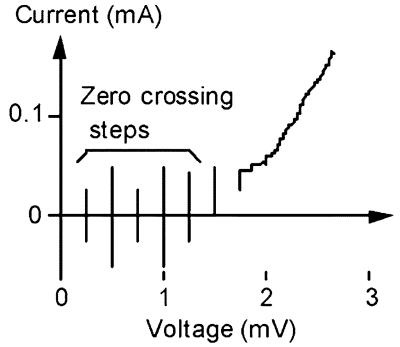

Fig. 3. *I–V* curve showing the zero-crossing steps of a high capacitance underdamped junction (large β_c). This curve is symmetric in I and V.

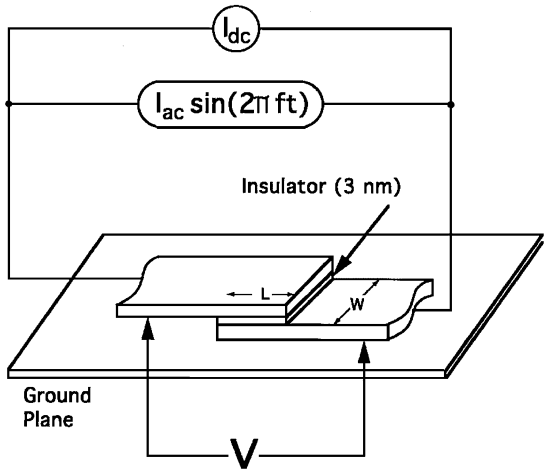

Fig. 4. Thin-film structure of a superconductor–insulator–superconductor Josephson junction typically used in conventional dc voltage standards.

effort in 1984 between the National Bureau of Standards in the United States and the Physikalisch-Technische Bundesanstalt in Germany resolved the problems of junction stability and microwave distribution and created the first large Josephson array based on Levinson's idea [11]. Further design improvements and system development produced the first practical 1-V Josephson standards in 1985 [12], [13]. Advances in superconductive integrated circuit technology, driven largely by the quest for a Josephson-junction computer, soon made much larger arrays possible. In 1987, the design was extended to a chip with 14 484 junctions that generated about 150 000 quantized voltages spanning the range from -10 to $+10$ V [14]. By 1989, all of the hardware and software for a complete voltage metrology system was commercially available. Today, with installations in more than 50 national, industrial, and military standards laboratories around the world, this *conventional* JVS is the only widely used application of a large-scale superconducting integrated circuit.

While zero-crossing steps have been the enabling technology for conventional voltage standards, they have two inherent and undesirable features: it is difficult to quickly select specific voltage steps, and noise can induce spontaneous transitions in the step number n. In the following sections, we shall see that overcoming these disadvantages has been a major occupation of metrologists over the last 15 years. We describe how new junction technologies have been developed that are capable of producing uniform junction characteristics for large arrays. This has enabled the *programmable* voltage standard with digitally selectable and stable output voltages, and the *pulse-driven* voltage standard that can synthesize arbitrary waveforms with fundamental accuracy. In this paper we focus on the essential technology that was developed for the conventional Josephson standard, and for the newer systems under development. For a more detailed review of the practical aspects of Josephson standards see Hamilton [15]. A more physics-oriented view of electrical metrology and Josephson standards, can be found in reviews by Niemeyer [16] and Kautz [17], [18].

II. Conventional Josephson Array Design

Fig. 4 illustrates the basic structure of one junction in a large series array. The junction is an overlap between two superconductive thin films that are separated by a thin oxide barrier. The junction sits above a ground plane and is separated from it by a few micrometers of insulation. A dc current $I_{\rm dc}$ and a microwave current $I_{\rm ac}$ are driven through the junction. The design parameters for the junction are its length L, width W, critical-current density J (critical current per unit area), and the microwave drive frequency f.

Stable operation requires that four conditions be satisfied.

1) L must be small enough that the flux induced through the junction area by the microwave magnetic field is much less than the flux quantum $h/2e$.
2) Both W and L must be small enough that the lowest resonant cavity mode of the junction is greater than f.
3) To avoid chaotic behavior, the junction plasma frequency f_p, which is proportional to $J^{0.5}$, must be less than about one-third f.
4) To prevent noise-induced quantum step transitions, the junction's critical current $I_c = WLJ$ should be as large as possible.

If any of these conditions is violated, the junction voltage is likely to switch randomly among several steps, making measurements impossible [17], [18]. Fig. 5 illustrates the region of stable behavior in the three-dimensional space of L, J, and W. The margin of stable operation, represented by the shaded volume in Fig. 5, increases with f and is ultimately set by a tradeoff between stability and the economics of providing a very high frequency microwave source. Most practical standards operate in the range 70–96 GHz.

The *I–V* curve shown in Fig. 3 shows steps covering the range from about -1 mV to $+1$ mV and is for a junction driven by a nearly optimum amplitude of microwave current. At lower amplitude the steps cover a smaller range of voltage, and at higher amplitude the steps are small and do not cross the zero-current axis. In a large array, every junction must generate a large zero-crossing step and, thus, the

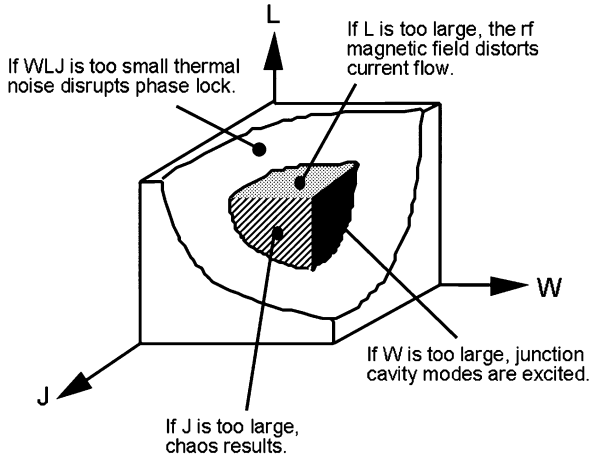

Fig. 5. Three-dimensional visualization of the region of stable voltage operation as a function of junction length L, width W, and critical-current density J.

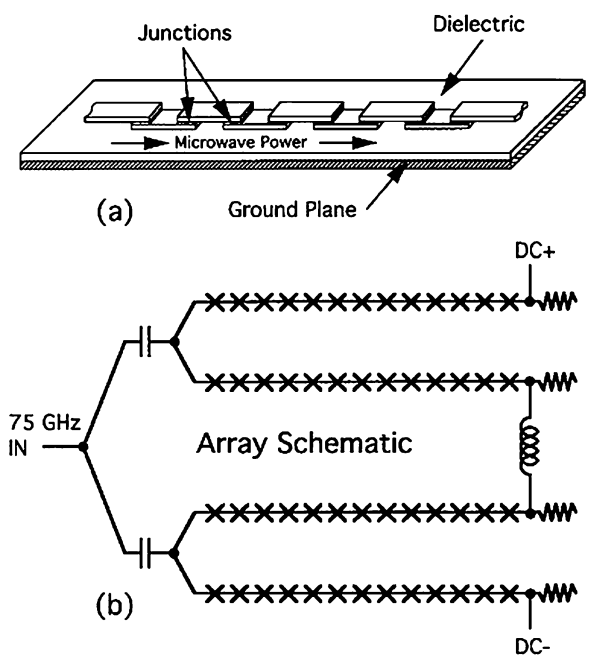

Fig. 6. (a) Series of Josephson junctions arranged to form a microstrip transmission line. (b) Electrical circuit of a typical JVS.

microwave power must be adjusted to a value low enough to accommodate the one junction receiving the largest microwave drive. In order to obtain the largest voltage from the smallest number of junctions, the circuit design must deliver nearly uniform microwave power to many thousands of junctions, all of which are connected in series. The solution to this problem is a simple extension of Fig. 4 to a series array of junctions in a line over a ground plane as shown in Fig. 6(a). The capacitive impedance of these underdamped junctions is so small (approximately 1 mΩ at the drive frequency) relative to the stripline impedance (approximately 3 Ω) that each junction has a very minor effect on the propagation of microwave power in the strip line. This junction stripline can propagate microwave power through 1000 or more junctions with relatively low loss [11].

A series/parallel circuit similar to that shown in Fig. 6(b) is used to make the arrays of 15 000+ junctions that are required to reach operation at 10 V. A network of low- and high-pass filters allows the microwave power to be split into multiple parallel paths while maintaining a dc path in which all junctions are connected in series.

A typical integrated-circuit layout for an array of 20 208 junctions is shown in Fig. 7. The microwave drive power is collected from a waveguide by a finline antenna, split 16 ways and injected into 16 microstrip lines, each containing 1263 junctions. Microwave power is applied by inserting the finline end of the chip into a slot parallel to the E-field in a WR-12 waveguide.

III. Conventional Voltage Standard Systems

A block diagram of a modern JVS system is shown in Fig. 8. The Josephson-array chip is mounted inside a high-permeability magnetic shield at the end of a cryoprobe that makes the transition between a liquid-helium dewar and the room-temperature environment. Three pairs of thermocouple-grade copper wires are connected to the array. One pair supplies bias current, a second pair monitors the array voltage with an oscilloscope, and the third pair delivers the array voltage to the calibration system. All of the wires pass through multiple levels of RF interference filtering. Microwave power is delivered through an overmoded circular waveguide consisting of a 12-mm-diameter tube with WR-12 launching horns on each end. This waveguide simultaneously achieves low thermal loss (<0.5 L of liquid He per day) and low microwave loss (as low as 0.7 dB/m at 75 GHz). A phase-locked oscillator (PLO) operating at a frequency near 75 GHz provides the microwave power to the chip. The reference frequency for the PLO is typically obtained from a cesium clock or a global positioning system (GPS) receiver.

As discussed previously, the zero-crossing steps of Fig. 3 allow a single-bias current while ensuring that every junction in a large array is on a constant-voltage step. Fig. 9(a) illustrates a simplified diagram of the bias circuit. In this circuit, a computer sets the bias voltage V_s with one digital-to-analog converter (DAC) and uses a second DAC to control the bias impedance R_s via optically modulated resistors. Fig. 9(b) shows a graphical solution for the stable operating points of the array and illustrates how control of both the bias voltage and the bias impedance is used to select a particular quantum voltage step [19]. The load line plots the range of voltage and current that is defined by the bias supply. The intersections of this load line with the *I–V* curve of the array (vertical lines) are possible stable bias points. Changes to V_s shift the load line left and right, whereas changes to R_s change its slope. To select a step at a given voltage V_a, the source voltage V_s is set to about V_a and the source impedance is set to about $f/K_J I_s \approx 10\Omega$, where I_s is the step height. This makes the load line steep enough to intersect only one or two steps and forces the array to a step at or very near V_a. Applying a damped oscillation to V_s helps move the array to the step closest to V_a. After a step is selected, the source impedance

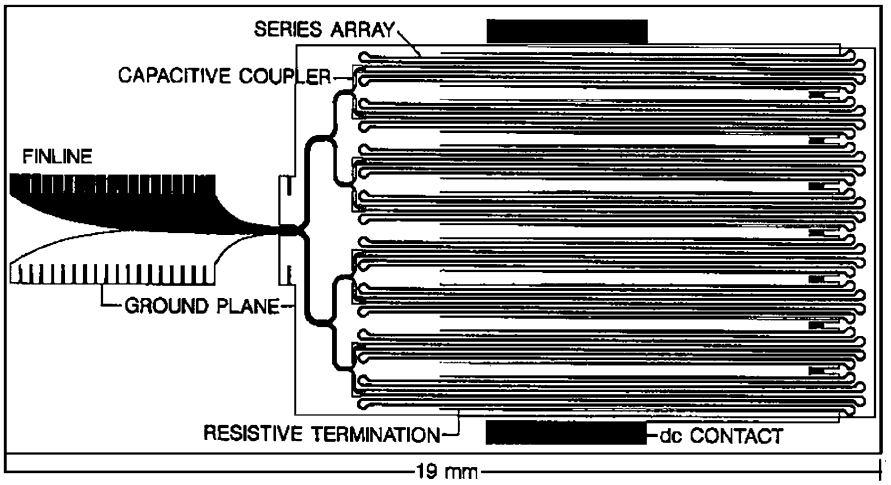

Fig. 7. Layout of a 20 208 junction 10-V Josephson array voltage standard chip.

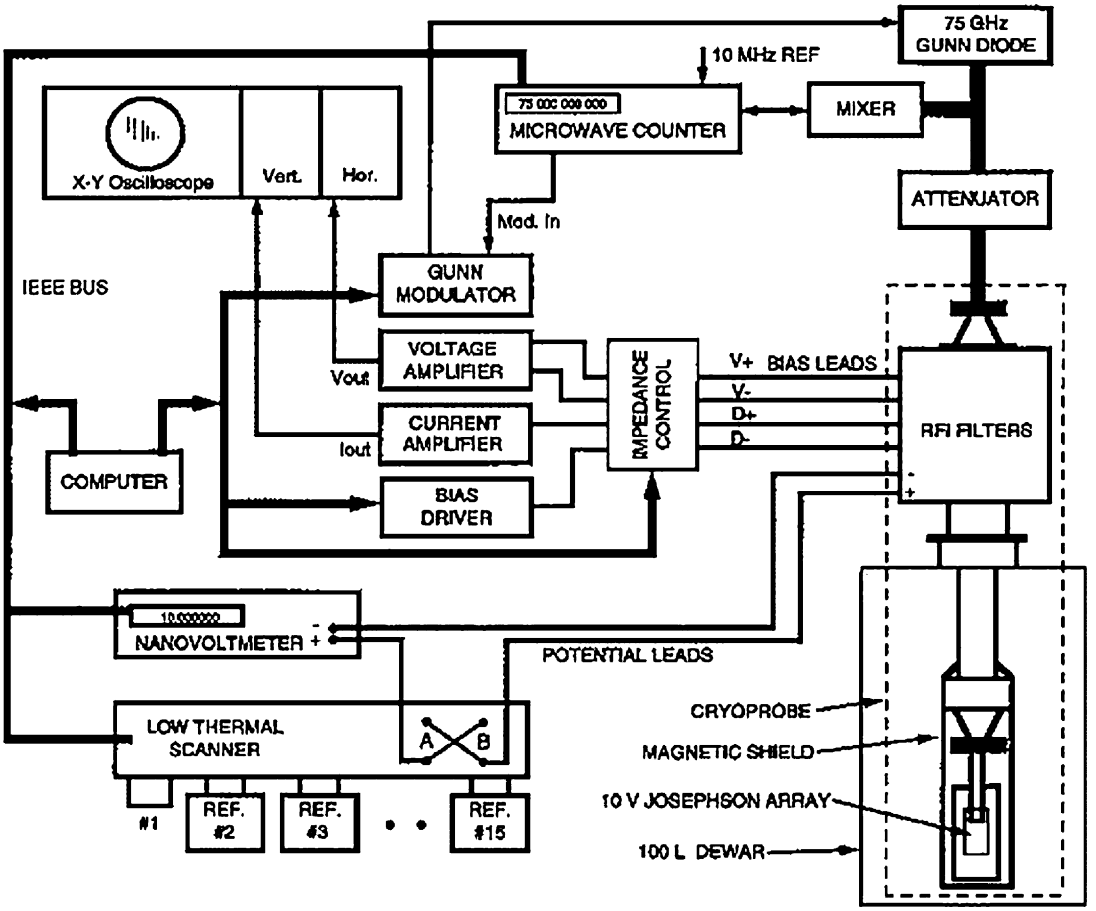

Fig. 8. Block diagram of a modern conventional voltage standard system.

is smoothly increased on all four bias connections (load line becomes horizontal) until the array current goes to zero and the array is effectively disconnected from the bias source. This open-bias condition is the most stable state for the array and eliminates the possibility of any errors resulting from bias current flowing through a small series resistance in the array—an occasional array defect. Computer control of this three-step process enables the system to find and stabilize the array voltage on a particular step within a few seconds. High-quality Josephson arrays will remain on a selected step for many hours.

Fig. 8 illustrates the basic method of measuring an unknown voltage relative to a Josephson voltage by placing the Josephson array and the unknown signals in series opposition across the input terminals of a sensitive digital voltmeter (DVM). Accuracy is improved by reversing the measurement leads and by averaging the DVM measurements for several minutes. The DVM measurements, reversals, and array step

Table 1
Potential Sources of Error and Uncertainty for a Josephson Standard

1. Reference frequency offset and noise.
2. Voltage drops in the measurement loop caused by leakage currents.
3. Null-meter gain error, bias current, offset, input impedance, nonlinearity, and noise.
4. Uncorrected thermal voltages in the measurement loop.
5. Offset due to rectification of the reference frequency current in array defects.
6. Any effect of electromagnetic interference.
7. Defective junctions or connections leading to a bias-dependent voltage.
8. The product of series resistance in the array and any residual bias current.

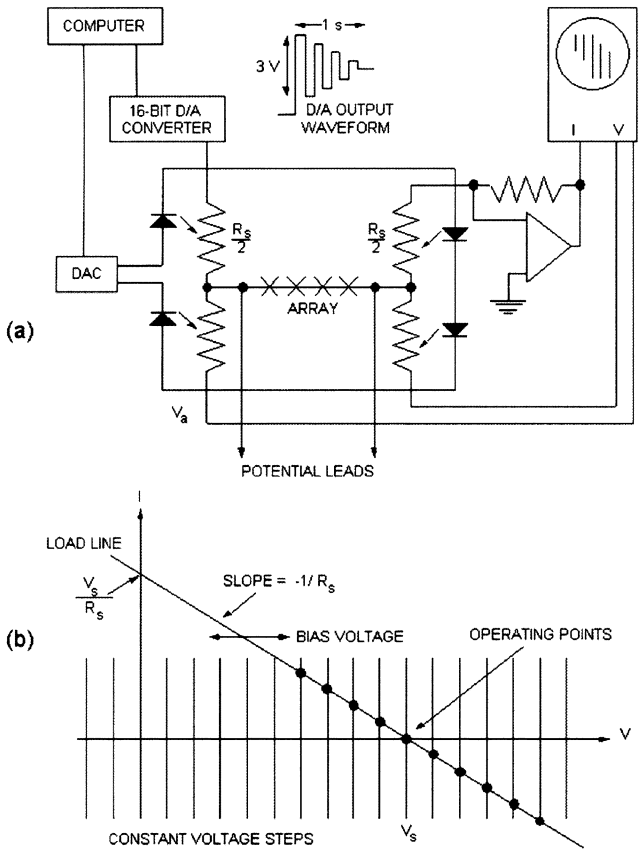

Fig. 9. (a) The bias circuit for a Josephson junction array. Light-emitting diodes control the bias resistance R_s by modulating photoconductive resistors (represented by arrows). (b) A graphical solution of the operating points for the array.

selection are all controlled by a computer. Systems like that shown in Fig. 8 are used to calibrate secondary standards, such as Weston cells, Zener references, and precise digital voltmeters. The typical uncertainty in measurements of 10-V Zener standards is limited by noise in the Zener to about 0.01 parts in 10^6. The ability to set the Josephson array to a wide range of discrete voltages also makes it the most accurate tool for measuring the linearity of high-accuracy DVMs.

IV. Uncertainty

While the voltage appearing across the terminals of a Josephson device is given exactly, in principle, by $V = nf/K_J$, in any real measurement there are a variety of potential sources of error and uncertainty, as listed in Table 1. In the case of a known error, such as a reference-frequency offset or a known leakage resistance, a correction can be made. It is the metrologist's task to assign realistic numbers to all uncertainties including the uncertainty in the corrections. Note that only items 1 and 2 in Table 1 depend on the magnitude of the voltage being measured, while all of the other components are about the same regardless of the voltage. Therefore, the combined effect of items 3–8 can be quantitatively evaluated by making a set of measurements of a short circuit using exactly the same settings (microwave frequency and power, bias, etc.) and algorithm as is used for any other measurement. The standard error resulting from items 3–8 is just the root-mean-square (rms) value of the set of short-circuit measurements [20]. Additional experiments must be performed to estimate frequency and leakage uncertainty. Internationally accepted procedures for combining uncertainties and establishing confidence intervals are the subject of the BIPM's *Guide to the Evaluation of Uncertainty in Measurement*. Typically, the total uncertainty of a Josephson system is a few nanovolts. Since the most common use of these systems is the calibration of Zener standards with a noise level of 50–100 nV, the contribution of the Josephson system is negligible.

V. Programmable Voltage Standards

Conventional JVSs based on the zero-crossing steps of series arrays of hysteretic junctions have two important disadvantages: (1) the step number n cannot be quickly set to a desired value and (2) noise may cause spontaneous transitions between steps. The step-transition problem requires that the bandwidth of all connections to the chip be severely restricted in order to filter out noise. In the case of classical dc measurements, these are minor inconveniences that can be easily dealt with in software. However, the step stability, step selection, and bandwidth problems preclude measurements such as the rapid automated analysis of analog-to-digital (A/D) and digital-to-analog (D/A) converters and the synthesis of ac waveforms with a computable rms value. In order to address these applications, two new standards have been developed, one of which focuses on producing stable programmable dc voltages, while the other can produce ac voltages and arbitrary waveforms.

VI. Stable Programmable DC Voltage

For the applications that require stable and programmable dc voltages, a new type of JVS has been developed in which the output voltage $V = nMf/K_J$ is defined by dividing a series array of M total junctions into smaller independently biased programmable segments and then digitally programming the junction step number n for the junctions in each segment [21]. The key to this new Josephson standard is the use of low-capacitance damped junctions that are designed to be nonhysteretic, that is, the junction voltage is a single-valued function of the junction current, as in Fig. 1. This is achieved by choosing β_c to have a value less than one. This, of course, brings us back to the situation in 1980 when it was deemed that arrays of such junctions would require individual bias currents to ensure that each junction was biased on a constant-voltage step. There are two reasons why this is now practical. First, in a number of different technologies [22]–[25], junction fabrication has advanced to the point where arrays of many thousands of junctions have variations in critical current and resistance of only a few percent. Second, better microwave design allows very uniform distribution of power to very large arrays [26]. These technological improvements allow a design in which each junction is typically biased only to the $n = -1, n = 0$, or $n = +1$ steps, and large voltages are obtained by using very large arrays. The result is a large increase in the operating margin, that is, the range of current over which every junction is biased on the same constant-voltage step.

The circuit for this new programmable JVS (PJVS) uses an array of nonhysteretic junctions that is divided into a binary sequence of array segments, as shown in Fig. 10(a), [21]. The microwave excitation for each junction is set to equalize the amplitude of the $n = 0$ and $n = \pm 1$ steps, as shown in Fig. 10(b). Each segment of the array can be set to the $n = -1, 0$, or $+1$ step by applying a bias current $(-I_s, 0, +I_s)$ at the appropriate nodes. The combined total step number for the whole array can, thus, be set to any integer value between $-M$ and $+M$, where M is the total number of junctions in the array. For example, to select step 5 we would set $I_3 = I_1 = I_s, I_2 = I_o = -I_s$. This would bias the single junction and the set of four junctions on the $n = 1$ step and leave all other junctions on the $n = 0$ step.

The rapid settling time and inherent step stability of the PJVS in Fig. 10 make it potentially superior to a conventional JVS for dc measurements. (We define a dc measurement to be one in which the transient associated with changing n can be excluded from the measurement.) Such measurements include calibration of dc reference standards and digital voltmeters, and the characterization of A/D and D/A converters. The circuit of Fig. 10 can also generate a staircase approximation to a sine wave by selecting appropriate step numbers in rapid succession. In theory, the resulting waveform has a computable rms value and might be used to confirm the ac–dc difference of a thermal voltage converter and for other ac measurements. In the case of ac measurements, however, the transient waveform during step transitions is included in the rms value and may lead to an unacceptably large uncertainty. Work continues to make this approach practical for ac synthesis at frequencies below 1 kHz [27], [28] and for fast reversed dc calibrations [29], [30].

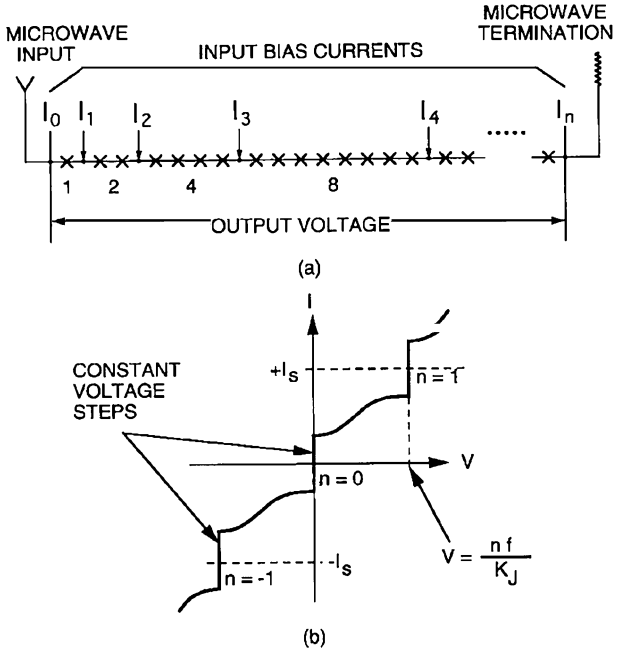

Fig. 10. (a) Circuit schematic of a programmable voltage standard based on a set of binary weighted arrays. (b) *I–V* curve of a single junction with the microwave power set to equalize the amplitude of the $n = 0$ and $n = \pm 1$ steps.

The National Institute of Standards and Technology (NIST) has produced a PJVS system that is based on junctions with niobium superconductors and palladium–gold normal metal barriers [22]. Yield and fabrication have made possible PJVS chips with over 30 000 junctions [26]. Photographs of one of these chips are shown in Fig. 11(a) and 11(b). These chips can be rapidly programmed to precise dc voltages between +1.1 and −1.1 V. Custom bias and measurement electronics were implemented in order to achieve complete automation and programmability of the output voltage [31]. A second and more important reason for automation is that the voltage steps of nonhysteretic junctions, unlike the zero-crossing steps of the conventional standard, must be occasionally checked to make sure that they are flat in voltage. The precision voltage is compromised if the steps are not flat because these arrays are continuously current biased, and the current flowing through any series resistance between the voltage leads will produce an error voltage. Nonflat steps are not a concern in the conventional JVS because no current flows through the array once it is settled on a quantum step.

With full automation to quickly program voltages and to check for step flatness, the PJVS is now a complete, easy-to-use system. NIST PJVS systems are being used in a number of applications, including primary dc voltage calibration at NIST, Watt-balance experiments at both NIST [32] and the Swiss Federal Office of Metrology (OFMET) [33], [34], and a metrology triangle experiment at the French

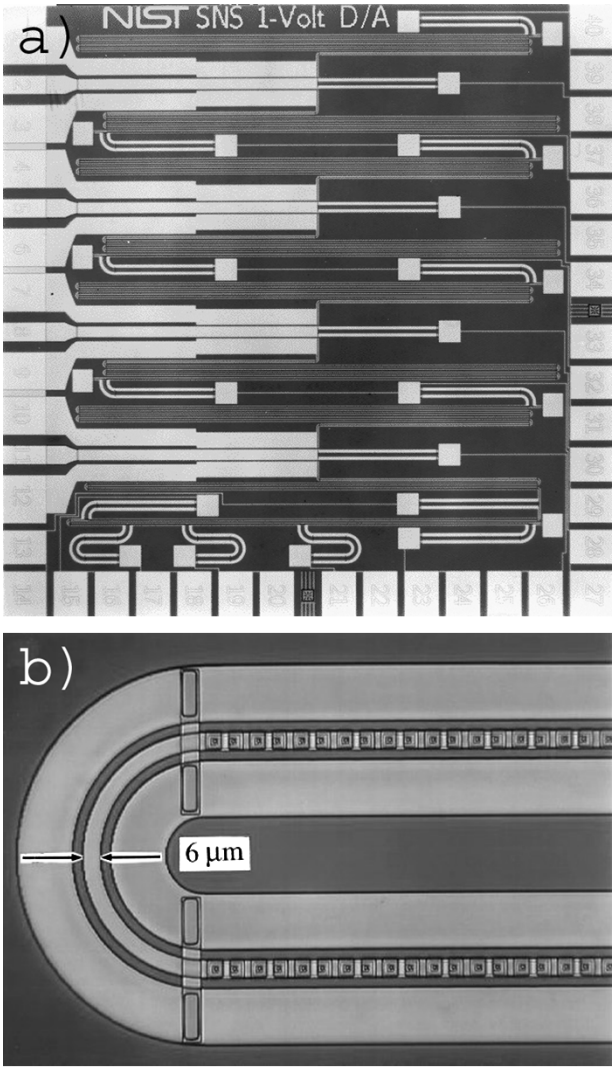

Fig. 11. (a) Photograph of NIST's 1 × 1 cm 32 768 junction programmable-array chip. (b) Section of coplanar waveguide showing the distribution of junctions along the center conductor.

Laboratorie Central des Industries Electriques (LCIE) [35]. Both experiments require stable precision voltages with high noise immunity, which can be provided by the large (>1 mA current range) voltage steps of the PJVS. Other metrology laboratories have focused their PJVS development programs on applications to higher voltage [36] or operation at higher temperature [37].

VII. AC Voltage and Arbitrary Waveforms

Although quite useful in several new applications, binary programmable arrays have not been very successful in the synthesis of ac waveforms because the undefined voltage during transitions between steps adds an unacceptable level of uncertainty. Another approach in which the array is biased with pulses has the potential to solve this problem. Thus far, we have discussed ways to program the voltage of a Josephson array by changing the step number n in the equation $V = nf/K_J$. It is clear that the same result might be achieved by changing f. Unfortunately, in the case of a

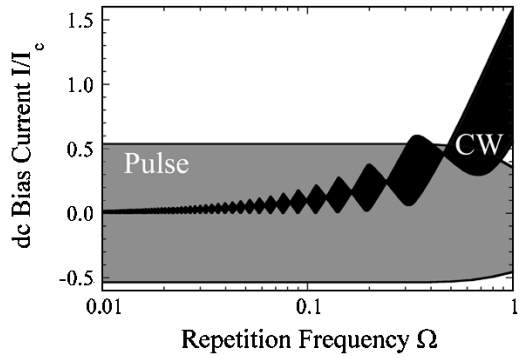

Fig. 12. Comparison of the normalized $n = 1$ step boundaries for a junction driven with a pulse train (black) and a CW (shaded) as a function of normalized frequency $\Omega = f/f_c$.

sine-wave excitation, the step amplitudes—that is, the current range over which the steps are at constant voltage—collapse rapidly to zero as the frequency decreases. This means that it is practical to control the voltage via the frequency over only a small range of frequency. However, if the sine-wave excitation is replaced with a pulse excitation, then the step amplitude becomes nearly independent of the pulse repetition frequency. Driving a Josephson junction with a current pulse of the proper amplitude and duration will cause the junction to make exactly one perfectly quantized voltage pulse. Fig. 12 shows a calculation of the $n = 1$ step current boundaries for a junction driven with a sine wave (black area) and a pulse train (shaded area) [38], [39]. Note that for a pulse drive, the step amplitude (range of dc current bias) is large, symmetric around zero, and independent of frequency all the way to zero frequency. This is because the shape of the current-drive pulse (in amplitude and duration) determines the operating range of the junctions, and not the spacing between pulses, as for a continuous sine-wave (CW) drive. If the pulse polarity is reversed, then the array can generate both positive and negative voltages [40].

A programmable voltage source based on this idea consists of a single large array of N junctions distributed along a wide-bandwidth transmission line. A pulse train at frequency f propagating down the line generates a time-averaged voltage Nf/K_J across the ends of the array. A complex output waveform can be generated by modulating the pulse train with a digital word generator. For example, using a clock frequency of $f_{\text{clock}} = I_c R K_J = 10$ GHz, the 10-b pulse sequence $11\,111\,000\,001\,111\,100\,000\ldots$ creates an output square wave of amplitude of Nf_{clock}/K_J and frequency of 1 GHz.

Fig. 13 is a block diagram of the process that is used to generate an accurate sine wave of frequency f_1 or any other periodic waveform from quantized Josephson pulses [40]. The modulator algorithm block is a computer program that digitizes an input signal $S(t)$ at a sampling frequency f_s. The algorithm is a second-order delta–sigma modulator that optimizes the signal-to-quantization-noise ratio over a desired frequency band [41]. For a repetitive waveform, the code generated by the modulator is calculated just once and stored in the circulating memory of a digital code generator.

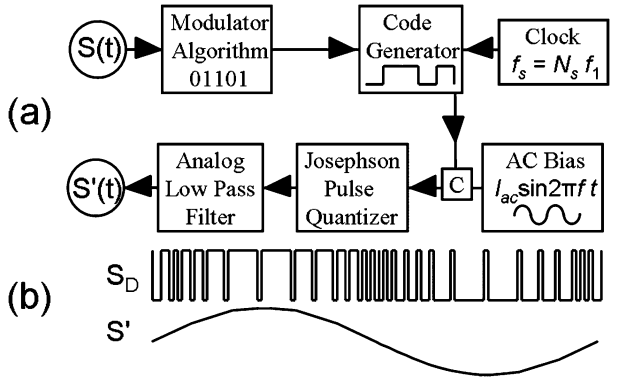

Fig. 13. (a) Block diagram of a delta–sigma DAC based on bipolar pulsed Josephson junctions [40]. $S(t)$ is the desired waveform and $S'(t)$ is the synthesized output waveform. (b) S_D represents a coarse bipolar bitstream signal applied in parallel with the microwave ac bias. The frequency f of the microwave bias is set to an odd half-integer multiple of the sampling frequency, e.g., $f = 3f_s/2$, in order to generate bipolar Josephson pulses for the desired integrated analog output waveform S'.

When the digital code generator is clocked at the sampling frequency, it creates a timed series of bias-current pulses for which the low-frequency spectral components approximate the original signal. The physics of Josephson junctions allows these pulses to be quantized to a single-flux quantum, that is, the time integral of their voltage is exactly equal to $h/2e = 1/K_J = 2.067\,834$ mV · ps. It has been shown both theoretically and experimentally that quantizing the pulses leads to a reduction in noise on the order of 60 dB [39], [42]. When the ratio f_s/f_1 is large, (e.g., $>10^4$) the in-band component of the voltage across the array is an almost perfect reproduction of the input signal. With quantized pulses, a knowledge of the digital code, the sampling frequency, and the number of junctions in the array is sufficient to exactly compute the spectrum and the rms value of output signal $S'(t)$.

The pulse-driven Josephson array has the potential to be both a dc voltage standard and an ac voltage standard with a bandwidth of 1 MHz or more. The importance of perfect quantization for precision waveform synthesis can be seen in Fig. 14, where a digital code is chosen to synthesize an analog waveform with no even harmonics, but where the odd harmonics are specifically chosen to decrease by precisely 10 dB for each higher odd-harmonic tone. Nonlinearities in the digital code generator (DCG) cause significant distortion in its output signal and inaccurate voltage reproduction of the odd tones as seen in Fig. 14(a). However, this DCG signal is adequate to drive the Josephson arrays, creating perfectly quantized Josephson pulses so that the Josephson array output gives the desired precision output voltage waveform, as seen in Fig. 14(b). Similar comparisons of distortion for sine waves synthesized by DCG and Josephson arrays are presented in [39] and [40]. Precision quantized Josephson output signals are of great interest for calibration and metrology applications.

Although the above demonstration shows the power of perfect quantization from Josephson arrays, there remain many challenges to developing this Josephson arbitrary waveform synthesizer as a practical ac JVS (ACJVS). The

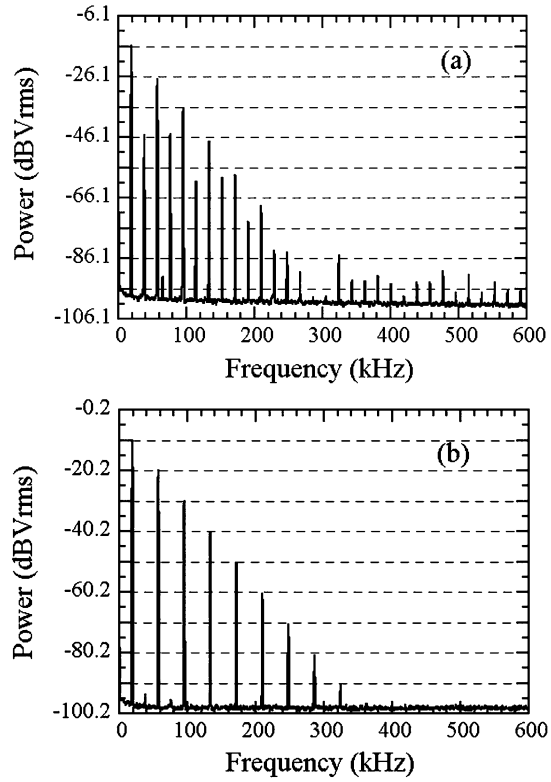

Fig. 14. Fourier spectra for a synthesized waveform having only odd-harmonic tones whose amplitudes are consecutively decreased by 10 dB. The measured signals were synthesized by: (a) a digital code generator and (b) a 3750-junction series array. The Josephson synthesized tones show the expected spectrum of the desired synthesized waveform, while the DCG has incorrect amplitudes for the odd tones and significant power at even harmonics due to internal nonlinearities.

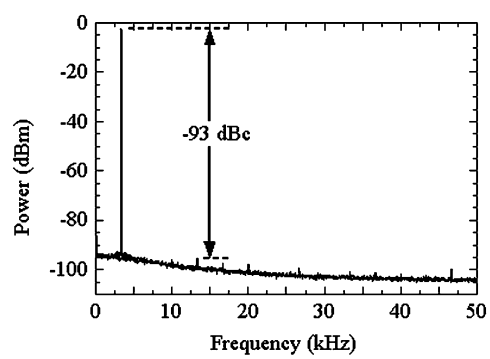

Fig. 15. Spectrum analyzer measurement demonstrating −93 dBc low distortion for the ACJVS with two Josephson arrays generating a 242-mV (zero-to-peak) sine wave at 3.3 kHz using 8200 junctions at 10 Gb/s. The spectrum measurement used 100-Hz resolution bandwidth and 100 averages to reduce noise of the measurement.

NIST effort has focused primarily on increasing the output voltage to practical levels [40]–[43]. Recent advances in circuit design and fabrication of superconducting integrated circuits have enabled demonstration of waveforms with a record 242-mV peak voltage, as shown in Fig. 15 [44]. Waveforms at both 3.3 and 33 kHz were demonstrated at this voltage, both having harmonic distortion below −93 dBc (dB below the fundamental). This larger output voltage allows practical metrology measurements for the first time.

In order for the ACJVS system to truly meet the definition of an "intrinsic" ac and dc standard, there must be a finite range for each bias parameter over which the output voltage does not measurably change [45]. This "flat spot" in the operating margins needs to be confirmed every time the ACJVS system is used for precision measurements and for each synthesized output waveform generated by the Josephson array. Every bias parameter must have a range over which the output voltage does not change at the level of parts in 10^7. Such a "flat spot" was recently found for the ACJVS using a thermal transfer standard [44]; however, it was not found at the full output voltage, in spite of the low harmonic distortion. This is because a very small -100-dBc distortion or error signal in the ACJVS output at the fundamental (with a relative phase of 0° or 180°) remains undetected by the spectrum analyzer, but still produces an error in the rms voltage of ten parts in 10^6. At 193 mV (zero-to-peak) and 2.8 kHz, we were able to find a flat spot in the operating margins for all eight different drive parameters. Using an ac/dc transfer standard we confirmed the ACJVS output flatness to be better than a part in 10^6. This is an important step toward developing a complete ac system.

VIII. Higher Performance With Lumped Arrays

One of the development goals for improving Josephson systems is to further increase the output voltage for both programmable and ac voltage standards. Present junction fabrication technologies use distributed arrays, where the junctions are *distributed* along a superconducting transmission line over many wavelengths of the microwave-drive frequency. The performance of these distributed arrays is degraded by microwave attenuation of the junctions and by standing waves from reflections. A few years ago, NIST became interested in developing nanoscale junctions for lumped arrays [46], [47]. A lumped array is one in which all of the junctions are placed in the transmission line within a small fraction, say one-eighth to one-quarter, of the wavelength of the highest drive frequency. Our goal is to make a lumped array whose total impedance is equal to the 50-Ω transmission-line impedance and which can generate as many Josephson pulses as possible. These arrays would be very efficient because most of the broadband power would not be wasted in a termination resistor, as in distributed-array circuits. A single optimized 50-Ω lumped array with 10-mA critical current and drive frequency matched to the characteristic frequency of the junction would be able to produce a maximum output voltage of 0.5 V for a single array on the $n = 1$ step and a 1-V output for the $n = 2$ step. The output voltage of these lumped arrays would, thus, be four to eight times that of the distributed arrays. This approach would increase the output voltage of the ACJVS to 1 V and the PJVS output voltage to 10 V for ten parallel arrays.

The challenge for lumped arrays is to put the junctions very close together. With junction characteristics optimized for a drive frequency of 16 GHz, 13 500 series junctions are needed with a maximum spacing of 120 nm [46], [47]. This close spacing is a significant challenge, since the smallest

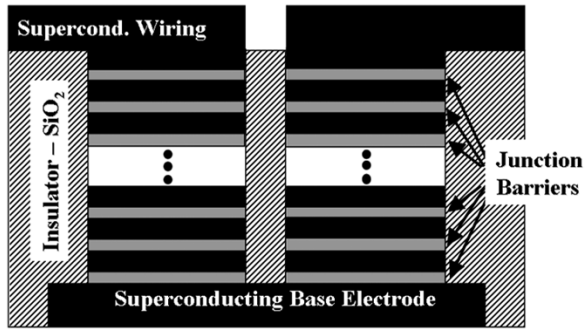

Fig. 16. Side view of two series-connected SNS junction stacks. Niobium superconducting layers are shown in black. The junction barriers are solid gray. The insulating silicon dioxide dielectric is shown as hashed lines.

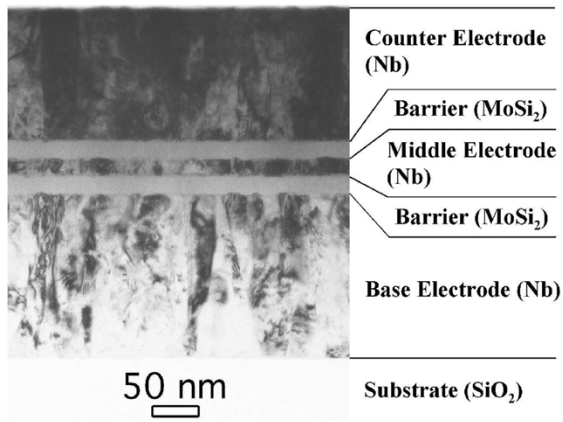

Fig. 17. Cross-sectional TEM image of a five-layer $Nb/(MoSi_2/Nb)_2$ film [50]. Each of the $MoSi_2$ barriers is 23 nm thick and the thickness of the Nb middle electrode is 20 nm. The image shows that the $MoSi_2$ deposits uniformly on the niobium, even when the niobium is as thin as 20 nm. (Image by John Bonevich-MSEL, NIST, 2002.)

SNS arrays fabricated using our PdAu-barrier process have junction spacing of 7 μm. Nanometer control of the barrier thickness, typically 20–30 nm, is essential because junction electrical characteristics depend exponentially on barrier thickness. Lumped-array junctions will, thus, require nanometer-scale dimensions and control to achieve sufficient uniformity.

The most successful approach to creating lumped arrays has been to place the junctions in vertical stacks, as shown in Fig. 16. The stacked junctions have multiple barriers deposited alternately with superconducting layers. Adjacent stacks are interconnected with superconducting base and wiring electrodes to create the series arrays. The National Institute of Advanced Industrial Science and Technology (AIST) in Japan demonstrated the first stacked-junction arrays for programmable standards in 2002 using niobium nitride superconductors and titanium nitride normal-metal barriers [48]. In order to accomplish this task at NIST we are investigating normal-metal barriers that can be dry-etched in-situ with the Nb superconductor [49]–[51]. Our most promising barrier material to date is $MoSi_2$. A transmission electron micrograph of two barriers separated by a 20-nm Nb middle electrode is shown in Fig. 17. Using $MoSi_2$ barriers

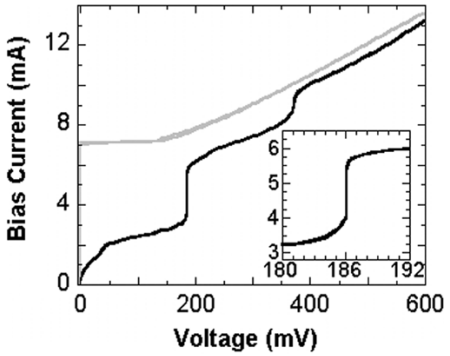

Fig. 18. *I–V* characteristics without (gray) and with (black) 9-GHz microwave bias for a 1000-stack series array of 10-JJ stacks [52].

we can make uniform constant-voltage steps with superconducting middle electrodes (the Nb between the $MoSi_2$ barriers in the stacks) as thin as 5 nm [50]. Furthermore, we have shown that the superconducting order parameter (and, thus, the junction electrical characteristics) remains unaffected, provided the superconducting electrodes are at least 20 nm thick. This corresponds to a junction spacing of only 40 nm, which is well below the 120-nm maximum spacing for lumped arrays.

Another significant result for Nb–$MoSi_2$ stacks is the first demonstration of operating margins for ac voltage–waveform synthesis. Precision audio sine waves at 2.5 kHz with 73-mV peak voltage were produced when a 2000-junction double-stack array was biased with an 18.5-GHz microwave signal and a 3-Mb-long digital code clocked at 7.4 Gb/s. The measured fast Fourier transform of this waveform showed harmonic distortion lower than 92 dB below the fundamental (−92 dBc), consistent with our best results from circuits with PdAu-barrier junctions.

The above results show that Nb–$MoSi_2$ stacks are very promising for the next generation of voltage standards. However, cooling the stacks and fabrication of tall stacks are issues that are still being addressed. For example, we have found that the maximum current through a stacked array is limited by the conductivity between the stack and substrate [51]. Fabricating tall stacks with nearly vertical walls in this multilayer structure is another significant challenge. However, improvements in our etch process have recently allowed Hadacek to demonstrate flat constant voltage steps in an array of ten-junction stacks [52], as shown in Fig. 18. The uniformity of the 10 000 total junctions in the array is sufficient to allow a flat $n = 1$ step over a current range greater than 1 mA (see inset). This range, although sufficient, is significantly lower than the expected 4.5-mA range, because the 7 mm-long 1000-stack array is twice the quarter-wavelength of the 9-GHz drive frequency and is, therefore, not lumped. Nevertheless, this is the first ten-junction stacked array to produce constant-voltage steps and is an important milestone. However, taller stacks and shorter arrays are needed to achieve the goal of a 50-Ω array that acts as a lumped element at its characteristic frequency (16–20 GHz).

IX. Summary

The accuracy and stability of JVSs far surpass those of Zener and electrochemical voltage-standard devices. The generated voltage can be adjusted to any value in the range ±10 V. The voltage is independent of environmental and material characteristics because it is derived directly from a fundamental constant, the ratio of the electron charge to Planck's constant. International agreement on a defined value for this constant ensures uniformity and reproducibility near 1 part in 10^9 in the approximately 60 Josephson standards located throughout the world. Newly developed programmable Josephson standards act like DACs with 12 or more bits of resolution and 30 b of absolute accuracy. They are being used for fast dc measurements and metrology experiments that demand great accuracy and noise immunity. The Josephson arbitrary waveform synthesizer is being developed as a next-generation standard voltage source with a bandwidth from dc to 1 MHz or more. Its design places great demands on fabrication technology, microwave design, and thermal engineering. Feasibility experiments at voltages up to 0.25 V confirm its potential as a broadband voltage source. New approaches including stacked junctions and lumped arrays hold the key to the practical realization of this ultimate standard for voltage metrology.

Acknowledgment

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He joined the National Institute of Standards and Technology (NIST, formerly the National Bureau of Standards) Boulder, CO, in 1971 and became a NIST Fellow in 1987. Most of his career at NIST has focused on Josephson devices and voltage standards. In 1999, he retired from NIST to start his own company, VMetrix LLC, Boulder, which specializes in system design, consulting, and training related to Josephson voltage standards. He has authored 80 publications and holds three patents.

Dr. Hamilton shared IR100 awards for his work on infrared detectors (1976) and Josephson array voltage standards (1987), and he has received two U.S. Department of Commerce Gold Medals for his work on superconducting integrated circuits using Josephson devices (1984 and 1989). He received the 1995 IEEE Electrotechnology Transfer Award.