Metrology Development for the Nanoelectronics Industry at the National Institute for Standards and Technology

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ABSTRACT

The National Institute of Standards and Technology has provided and continues to provide critical metrology development for the semiconductor manufacturing industry as it moves from the microelectronics era into the nanoelectronics era. This presentation will describe the National Semiconductor Metrology Program, including a detailed discussion of several projects: Nanolithography Using Scanning Probe Oxidation; Atomic-Level Film Characterization; and Nanoelectronic Device Characterization.

Keywords: gate dielectrics, molecular electronics, nanoelectronics, nanolithography, thin films.

1 BACKGROUND

Integrated circuit manufacturing has moved aggressively through the "microelectronics" era into the "nanoelectronics" era. The National Institute of Standards and Technology (NIST) has provided and continues to provide critical metrology for this remarkably productive industry. This presentation will describe broadly the National Semiconductor Metrology Program and discuss in detail several projects in the "nano-regime."

In 1992, the United States Congress, recognizing the critical role of the semiconductor industry for the United States economy, created the National Semiconductor Metrology Program (NSMP) initiative to accelerate semiconductor metrology development at NIST. The NSMP is currently funded at $12.5 million, and leverages approximately an equivalent dollar value of funds from other sources.

The NSMP is administered by the Office of Microelectronics Programs (OMP), which was established to identify projects of high impact to the semiconductor manufacturing industry, to fund those projects, and to monitor the progress. A further function of the OMP is to serve as broker between the industry and NIST, insuring timely transfer of achievements, and to gather critical industry metrology needs to continuously reprioritize NIST projects.

The NSMP projects are grouped into program clusters; (1) **Lithography Metrology**, providing critical optical measurements on materials for next generation lithography (NGL) solutions, calibration of NGL sources, and characterization of NGL resist materials; (2) **Critical Dimension and Overlay Metrology,** delivering measurement techniques and artifacts for length measurements and positioning in the plane of the semiconductor wafer; (3) **Thin Film and Junction Metrology,** developing vertical dimension metrology, film and junction characterization and artifacts; (4) **Interconnect and Packaging Metrology,** reflecting the blurring of back-end-of-wafer interconnect processing and packaging processing, this program explores properties, reliability and mutual compatibilities of the materials used; (5) **Wafer Characterization and Process Metrology,** advancing and refining measurement techniques for the ever tightening requirements for wafer processing; (6) **Test Metrology,** investigating novel techniques for improving high frequency and non-linear circuit testing; and (7) **Manufacturing Support,** contributing to the necessary infrastructure and standards for manufacturing productivity improvement.

2 TECHNICAL MOTIVATION

The CMOS FET (Field Effect Transistor), which is the current basis of ULSI (Ultralarge-Scale Integration) circuits, is beginning to show fundamental limits associated with the laws of quantum mechanics and the limitations of fabrication techniques. By 2005, the Semiconductor Industry Association's (SIA's) 2001 International Technology Roadmap for Semiconductors (ITRS) shows no known solutions for a variety of technological requirements including gate dielectric, gate leakage, and junction depth. Therefore, it is expected that novel fabrication, process monitoring, and device measurement approaches will be needed to continue aggressive CMOS scaling. In addition, it is predicted that entirely new device structures and computational paradigms will be required to augment and/or replace standard planar CMOS devices.

The evolving decrease of the gate dielectric film thickness to an oxide-equivalent value of 1 nm is identified as a

critical front-end technology issue in the ITRS [1]. For effective gate dielectric thicknesses below ~ 2.0 nm, SiO_2 is being replaced, initially by oxynitrides or oxide/nitride stacks, and then by either metal-oxides or metal-silicates. Process control tolerance needs for dielectric thickness are projected to be ±4 % (3 σ), which translates to less than 0.1 nm for 2 nm films. Requirements for process control measurements are a factor of ten smaller still. Electrical and reliability characterization methodologies need to be developed and enhanced to address issues associated with both ultra-thin SiO_2 and alternate dielectrics including large leakage currents, quantum effects, and thickness dependent properties. As compared to SiO_2, very little is known about the physical or electrical properties of high dielectric constant gate dielectrics in MOS devices. The use of these films in CMOS technology requires a fundamental understanding of the relationship between the gate dielectric material/interface and device electrical and reliability measurements.

3 ATOMIC-LEVEL FILM CHARACTERIZATION

NIST's work in gate dielectrics ranges from thickness measurements by using spectroscopic ellipsometry to electrical and reliability measurements of MOS devices. The ellipsometry work is directed at determining preferred structural models, spectroscopic index of refraction values, or preferred optical dispersion functions for each of high-k films. Analysis is done with software developed by NIST for spectroscopic ellipsometry; [2] this software allows maximum flexibility for addition of the latest published or custom-developed optical response models as appropriate for each material system investigated. Through collaborations with SEMATECH, IC industry companies, and SRC university staff, as well as with key researchers in other parts of NIST, Project staff are leading and participating in a number of multimethod comparison studies of various ultra-thin gate dielectric films. These multimethod studies utilize techniques such as X-ray and neutron reflectivity, high resolution TEM, EELS, angle-resolved XPS, SIMS, C-V and I-V analysis, as well as spectroscopic ellipsometry and reflectivity. The results of these multimethod studies improve the general understanding of state-of-the-art measurement capability for very thin films, and also allow Project staff to assess the results of various optical models being applied to the analysis of these films with respect to interface layers and structural composition, morphology, and uniformity.

Researchers are also investigating the physics of failure and the reliability testing techniques for ultra-thin SiO_2 and high dielectric constant gate dielectrics [3]. The physical mechanism responsible for "soft" or "quasi" breakdown modes in ultra-thin SiO_2 films and its implications for device reliability are investigated as a function of test conditions and temperature. The understanding generated in this research is used to continue generating standard measurements through a NIST coordinated collaboration between EIA-JEDEC (Electronic Industries Association Joint Electron Device Engineering Council) and the American Society for Testing and Materials (ASTM). In collaboration with SEMATECH, electrical measurement techniques, procedures and analysis associated with devices having thin oxide and alternate gate dielectrics are investigated. Electrical characterization methodologies are developed to address various issues associated with these films, including large leakage currents, quantum effects, thickness dependent properties, large trap densities, transient (non-steady state) behavior, unknown physical properties, and the lack of physical models. Issues associated with thickness extraction have been addressed [4].

4 ATOM-BASED DIMENSIONAL METROLOGY

At the nanometer scale, the development of nanometer sized structures with accurately measured geometry and position is a primary goal. Samples of this type are not readily available from commercial sources and have to be fabricated in house. In addition, the fabricated features must be measured with tools having high enough imaging and measurement resolution. These samples also have to be dimensionally stable at the nanometer scale and externally accessible to allow transfer to other measurement tools. Chemically-prepared hydrogen-terminated silicon samples are used as substrates and methods for etching nano-scale structures into the silicon have been developed [5]. FIM measured tips can be used to measure features fabricated in-situ (UHV STM and preparation) or prepared externally [6]. These features can be measured accurately with the additional use of a unique picometer-resolution diode laser-based interferometer system [7].

In the atomic regime, we are developing atom-based standards. These are structures of controlled geometry whose dimensions can be measured and traced directly to the intrinsic crystal lattice. This work is based on the preparation and imaging of features with atomic resolution. The atomic spacing is verified with advanced diode laser interferometry. Most current work is also focused on silicon substrates due to our ability to prepare atomically-ordered, hydrogen-terminated samples and their subsequent potential to be etched on the atomic scale. However, other materials for measurement in the atomic regime are being explored for pitch and linewidth artifacts. An essential aspect of this work is the ability to measure features on the atomic scale with a traceable measurementtechnique. We have developed a new implementation of a Michelson interferometer which maintains a fixed number of wavelengths in the measurement path. This method, based on a tunable diode

laser, then mixes the tunable laser with a fixed HeNe laser enabling a traceable frequency measurement. An example of this technique is shown below demonstrating the resolution on a graphite lattice.

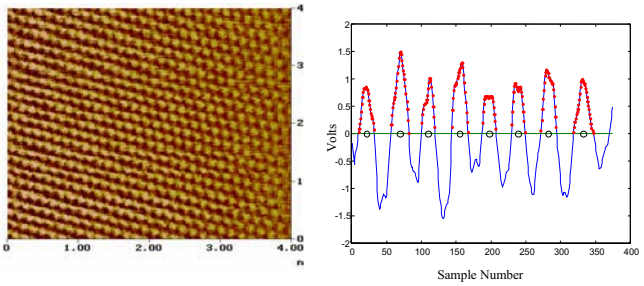
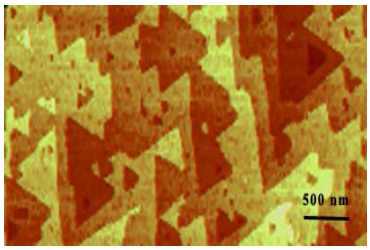


Figure 1. These figures show an STM image of an atomic lattice on the left and a high resolution interferometer measurement on the right. The individual data points in the profile indicate where STM height and interferometer position data were simultaneously acquired.



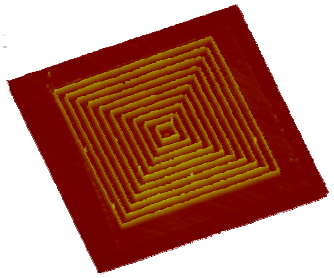


Figure 2. The figure on the left shows a hydrogen terminated silicon surface. The step and terrace surface is seen with each step being a single atom in height. The triangular structures are a result of complex etching dynamics. The figure on the right shows features written on a silicon surface in a medium vacuum environment. Features in the system have been fabricated below 20 nm in critical dimension.

The fabrication of high resolution features is accomplished in two different environments. The methods used in fabricating these samples have a similar origin to those air ambient methods described in the next section, except that these samples are prepared in UHV or high vacuum complex multi-chamber systems equipped with a STM, FIFEM, and sample preparation facility. The writing process shown in the figure above results in a hard etch mask written directly on a Si (111) substrate. Extensive work has gone into the preparation of atomically ordered hydrogen terminated surfaces [8]. These surfaces can now be routinely prepared and allow for the systematic development of fabrication processes of sub-20 nm sized features.

5 NANOLITHOGRPHY USING SCANNING PROBE OXIDATION

Scanning probe oxidation is a high-resolution lithography technique pioneered at NIST. It has been in use at research laboratories worldwide for prototyping nanoelectronic, nanoelectromechanical, and nanophotonic devices. NIST projects currently employ this technique for the fabrication and characterization of sub-50-nm linewidth 1-D and 2-D prototype calibration structures for NIST's metrology program and silicon nanowires for novel electronic devices, as illustrated in Figures 1 and 2. Additional collaborations are exploring scanning probe oxidation for local thin-film materials characterization of metallic and nitride Ti, Zr, and Hf films.

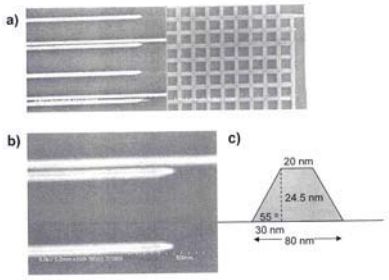


Figure 3. a) 1-D and 2-D prototype structures and nanowires made by scanning probe oxidation and anisotropic etching on a silicon-on-insulator substrate. B) Detail of nanowires. C)Schematic line profile: width along the top of the features is 20 nm and pitch of closely spaced wires is 60 nm.

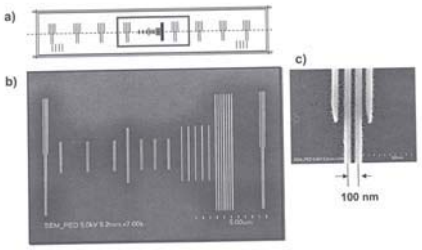


Figure 4. a) 80µm pitch prototype calibration grating with optically and SEM-accessible features made by scanning probe oxidation and anisotropic etching on a silicon substrate. B) Detail of the central SEM accessible pattern. C) Minimum 100 nm pitch obtained on this early prototype.

6 NANOELECTRONIC DEVICES

NIST is developing the metrology needed for nanoelectronic devices. This project is concerned with fundamental research related to possible future devices that will replace or augment standard CMOS technology. The industry for these emerging nanoelectronic devices will require reference data, standards, precision measurement protocols, and standardized test structures and associated measurement protocols to develop into a viable commercial technology.

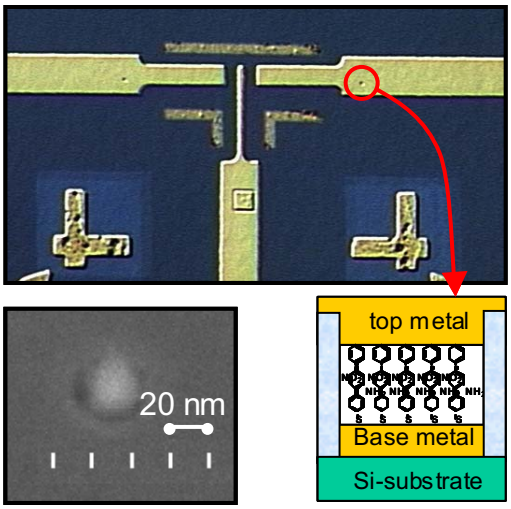


Figure 5: "nanoBucket" molecular electronic test structure. Top: optical micrograph showing three completed nanobuckets of varying areas. Bottom left: SEM micrograph of the base metal of a nominally 30 nm nanoBucket. Bottom right: schematic cross-section of a nanoBucket.

Metrology is under development for two specific areas of nanotechnology: molecular electronics [9] and Si-based quantum electronics [10]. In molecular electronics, we are developing test-structures based upon nanofabrication processing techniques for assessing the electrical properties and reliability of moletronic molecules. Figure 5 shows one example of a molecular electronic, referred to as a nanobucket, successfully fabricated and utilized at NIST. Molecules are incorporated into the test structures via self-assembly to form high-quality SAMs (self-assembled monolayers). In addition to the complexity of the nanofabrication of test structures, the challenges associated with measuring the electrical properties (such as current-voltage and capacitance-voltage as functions of temperature and applied fields) of these small molecular ensembles are daunting. The measured electrical properties are correlated with systematic characterization studies by a variety of advanced analytical probes and the results used in the validation of predictive theoretical models. In Si-based quantum electronics we focus on physical and electrical metrology of the basic building blocks of silicon quantum electronic devices (e.g., quantum layers, wires, and dots of silicon surrounded by silicon dioxide). By working with advanced lithographic techniques such as scanned probe oxidation, device structures are fabricated in order to correlate the physical properties of these silicon building blocks with the ultimate device performance. By identifying and addressing the critical metrology issues associated with these basic building blocks, the basis of metrology for future Si-based ULSI nanotechnology will be defined.

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