A LOW THERMAL ERROR SAMPLING COMPARATOR FOR ACCURATE SETTLING MEASUREMENTS

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ABSTRACT

A new sampling comparator design employing a signal-dependent biasing scheme is described. The dynamic bias significantly reduces signal-induced thermal error in the comparator. The circuit design approach is applicable to comparators intended for use in equivalent-time, successive approximation analog-to-digital conversion where required bandwidths may exceed 1 GHz and digitizing resolution may be as high as 16 bits. The technique is well suited for high accuracy settling measurements where thermal tail error can undermine the achievable settling response of an otherwise high bandwidth sampler. The new comparator design is a logical follow-up to previous work in which front-end bias on/off switching was employed. A prototype circuit has been fabricated in a 1.5 µm BiCMOS process. In the prototype device, the technique reduces settling error at 300 ns from 800 µV/V to 80 µV/V and improves gain flatness to within 300 µV/V from dc to 1 MHz.

1. INTRODUCTION

Accurate measurement of settling parameters is critical to the needs of electronic instrumentation and automated test equipment (ATE) providers and their customers. Oscilloscope calibrations depend upon step generators that are well characterized not only for transition duration but also for settling response. End-use applications such as high resolution video/graphics and radar imaging require that the settling behavior of components including analog-to-digital (ADC) and digital-to-analog (DAC) converters as well as associated signal conditioning amplifiers be characterized accurately.

This paper describes a design idea for improving the settling performance of a digitizer that samples in equivalent-time. The method uses a dynamic bias technique to minimize signal-induced thermal error in a sampling comparator. A reduction in settling error at 300 ns from 800 µV/V to 80 µV/V is demonstrated in a prototype, proof-of-concept device.

Dynamic or adaptive biasing has been discussed in the literature as a way to address slew rate limit problems and reduce operating power consumption [1][2]. The approach described in this paper is similar but differs in that the technique is applied to the problem of thermal distortion in a comparator. Particular attention is given to the error in settling response.

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2. BACKGROUND

Various methods for measuring settling have been described previously [3][4]. One method based on sampling and digitizing is illustrated in Fig. 1. A sampling comparator probe forms the comparator portion of a successive approximation type ADC and at the same time performs the sampling function. Operating in equivalent-time, a single conversion is obtained through a series of successive approximations, each occurring on a different period of the waveform being digitized. As each conversion is completed, the timebase delay is increased by one sample period allowing the next point on the waveform to be sampled. For low frequency signals, a more sophisticated timebase can decrease acquisition time by allowing more than one comparator decision to be made per signal period [6][10].

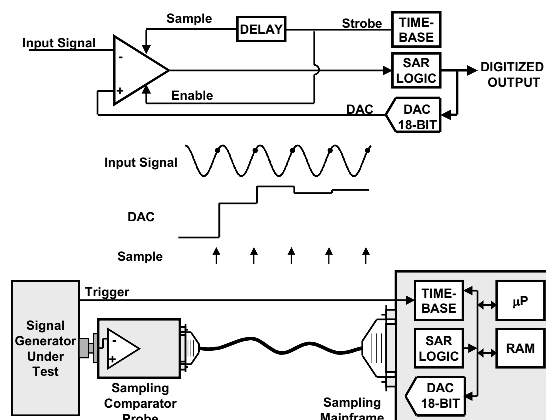

Fig. 1. Equivalent-time, successive approximation digitization. Comparator probe connects to sampling mainframe through umbilical harness.

In this arrangement, the DAC, successive approximation register (SAR) logic, and timebase reside within the sampling mainframe. Overall performance is enhanced because the critical and sole wideband component of the measurement process - the comparator - is placed in close proximity to the signal source being measured.

At least one commercially available instrument has used this technique, packaging the comparator and companion circuitry neatly in a pencil-type probe [5]. NIST has also developed its

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own custom comparator ASIC and sampling system with high bandwidth (2.3 GHz) and excellent settling performance [6]-[8]. A NIST Special Test measurement service for step settling using this equipment is available for customers seeking settling uncertainty as low as 0.2 % at 2 ns or 0.02 % at 10 ns [9].

A properly designed SAR-type digitizer sampling in equivalent-time can achieve 3 dB bandwidths in excess of 1 GHz with digitizing resolution of 16 bits or more. A drawback of this approach is that in order to sample in equivalent-time, the waveform being sampled must be repetitive, and a synchronous trigger signal must be available.

Implicit to this design philosophy is the fact that although multi-comparator digitizing schemes achieve higher real-time sample rates, their accuracy is limited to the input offset mismatch among the individual comparators. In contrast, a single comparator SAR approach has only a single offset, and it can be calibrated. The offset does not limit overall accuracy which, through signal averaging, can surpass the limit imposed by the noise floor of the sampling system.

3. SIGNAL-INDUCED THERMAL ERROR

To measure the settling performance of a step signal generator over time epochs shorter than 100 ns with uncertainty less than several hundred parts in 10^6, attention must be paid to the problem of signal-induced thermal error within the sampling electronics. The problem is described as follows.

For waveform samples taken at time instants following the step transition, the DAC reference value under SAR control approaches the waveform final value when the lesser significant bits are being decided. In order to allow maximum time for the DAC to settle, the DAC value required for the next comparator decision is programmed as soon as the comparator decision for the present bit is available. For step signals, this means that during the time period before the waveform transition, a differential voltage equal to the step signal amplitude is present at the comparator inputs. During this period, the two transistors comprising the comparator input differential pair will heat unevenly, and a voltage offset between the two will develop. When the step transition occurs, differential power dissipation between the two transistors becomes zero, but the time for thermal equilibrium to be reestablished can be as long as hundreds of nanoseconds. As the thermally induced offset voltage returns to zero, its superposition onto the true signal will be sampled by the latch, and an error in the sampled data will be manifest as a long exponential tail.

The NIST sampling comparator [7] employs a novel method for minimizing thermal errors in the differential pair front-end. A switch controlling the bias current for the front-end differential pair is included that is normally in the off or open position. When the switch is in this position, the stage is not powered, so large differential voltages at the comparator inputs do not cause differential heating. Prior to sampling, the switch enables the front end bias current just long enough for the signal to be acquired. For the NIST comparator, the time between front-end turn-on and strobing is 2 ns.

Fig. 2 illustrates how front-end off/on switching reduces thermal tail error when measuring step signals. During most of the period preceding the waveform transition, the comparator front-end is switched off. (For the NIST equivalent-time sampling system, the time between strobes is always at least 30 μs). During this time, no thermal offset error is produced. For samples taken within the first 2 ns after the waveform transition, differential heating takes place for at most 2 ns. For samples taken more than 2 ns after the step transition, no error is produced because the waveform transition has already occurred before the front-end has turned on.

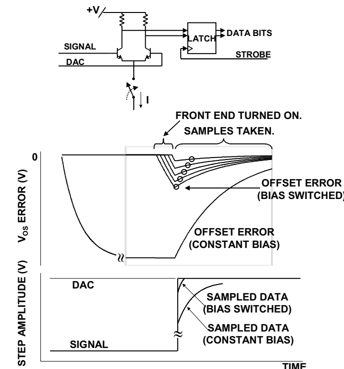

Fig. 2. Signal-induced thermal error with and without front-end bias switching.

4. DYNAMIC BIAS APPROACH

A dynamic bias approach replaces the front-end bias enabling switch with circuitry that continually varies the bias current according to the magnitude of the differential input voltage. When the absolute differential input voltage is large, bias current to the tracking amplifiers is reduced to the minimum level needed to sustain a correct latch decision. When the differential input voltage is small, bias current is increased to the level required for the desired bandwidth and signal-to-noise performance. Varying the bias current in this manner lowers input amplifier differential power dissipation, and associated thermal error is significantly reduced. This approach eliminates the additional bias on/off control signal and its requisite timing requirement.

Fig. 3 shows a schematic of a dynamic bias comparator circuit. Transistors Q1-Q8 comprise a conventional sampling comparator with two tracking stages (Q1-Q4) and a latch (Q5-Q6). Transistors Q11-Q18 provide the variable bias. The coupled Q15/Q16 emitters provide an absolute value function that drives current steering transistors Q17 and Q18 to produce the variable current. Constant current source I_x ensures that the latch has sufficient current to regenerate when the dynamic bias current is at a minimum. I_x is steered toward the latch by extra switching transistors Q9 and Q10 during strobing. I_x is chosen to be approximately equal to the maximum value of the front-end bias current. Current source I_0 establishes a minimum current level for the tracking stages ensuring that valid latch decisions can be obtained when the differential input voltage is large.

Fig. 4 shows a simulation of the difference in power dissipation between the input transistors versus signal level when bias current is held at a static level of approximately 800 μA and when it is modulated by the input signal. In the simulation, the signal input was swept from –1 V to +1 V with the DAC input held constant at 0 V. For signal magnitudes greater than 0.1 V, differential power dissipation is less in the dynamic bias case. For signal magnitudes greater than 0.25 V, differential power dissipation in the dynamic bias case is less than one tenth the dissipation for the static case.

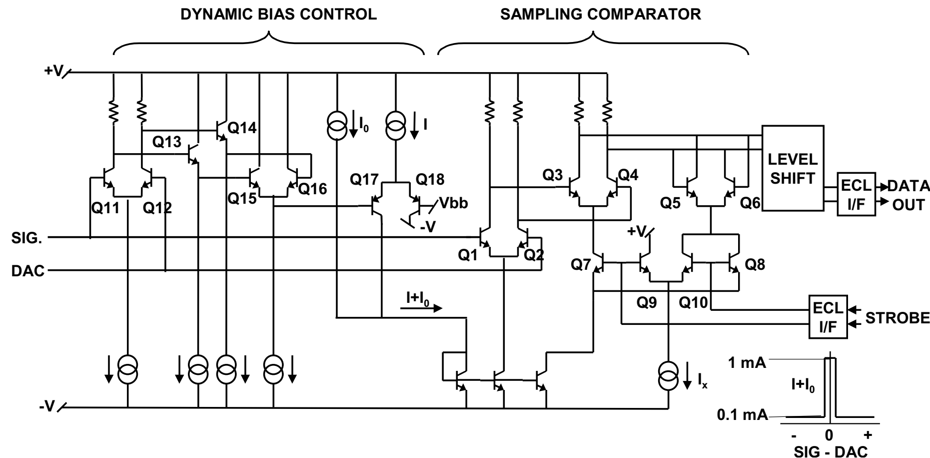

Fig. 3. Simplified schematic of a sampling (latching) comparator with dynamic bias.

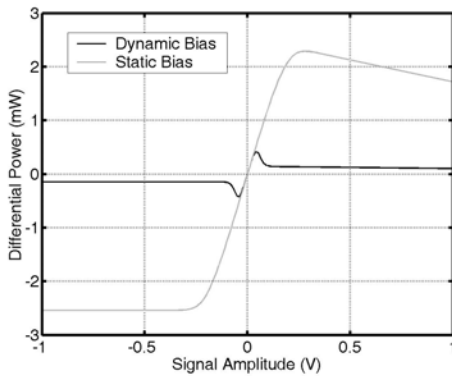

Fig. 4. Simulation of difference in power dissipation between the transistors making up the front-end differential pair.

5. RESULTS

The circuit of Fig. 3 has been prototyped in a 1.5 μm CMOS process that also provides a P base layer for the construction of npn bipolar junction transistors. A micrograph of the chip is given in Fig. 5. The chip has been designed into a probe circuit board along with additional circuitry to receive the DAC reference signal from the sampling mainframe. The circuit board also provides externally programmable dc currents for the bias sources (for experimentation) as well as the pnp transistors since these were not available on-chip. The circuit was operated from ±6 V power supplies. The DAC full scale range was configured for ±2 V.

Fig. 6 shows the tail current of the Q1/Q2 pair when the comparator input signal is a sine wave with peak amplitude of 1 V at a frequency of 1 MHz. The DAC value was fixed at 0 V. To monitor the bias current, an additional transistor with an uncommitted collector was included in the current mirror string. The bias current ranges from approximately 70 μA during most of the signal period to a peak of 800 μA at the zero crossings.

Fig. 7 shows the probe's step response in the transition region. The source was a commercial step generator designed to produce an accurate-settling step waveform with a transition duration of approximately 15 ps. The sample period was 100 ps. The

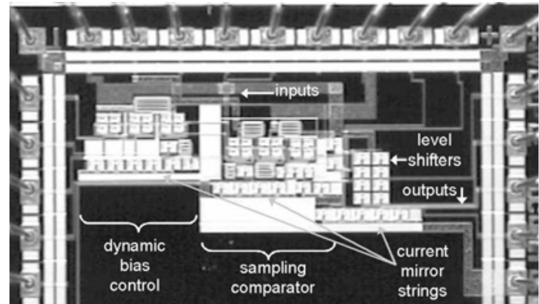

Fig. 5. Micrograph of prototype comparator chip (2200 μm x 1250 μm). All differential pairs are laid out in a common centroid configuration.

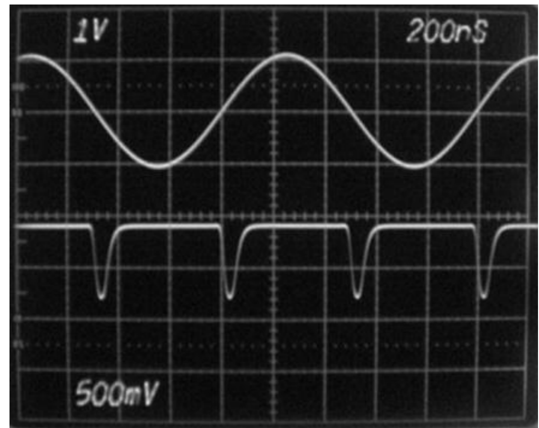

Fig. 6. Front-end differential pair tail current (lower trace) measured across a 1 kΩ resistor.

probe's transition duration is 3.5 ns, consistent with a 3 dB bandwidth of approximately 100 MHz.

The primary motivation for using a dynamic bias is the improvement that can be obtained in settling behavior. Fig. 8 shows the probe's step response in the settling region. 800 data record averages were acquired to produce the waveforms shown. In the dynamic bias case, the probe has settled to within 80 μV/V

of the step amplitude after 300 ns. In contrast, the settling error at 300 ns when the bias is held constant is approximately 800 μV/V. Residual thermal tail is apparent even though an interdigitated, common centroid layout of the input differential amplifier was used.

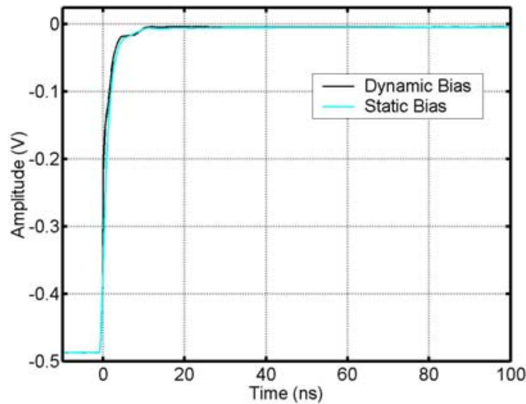

Fig. 7. Comparator probe step response.

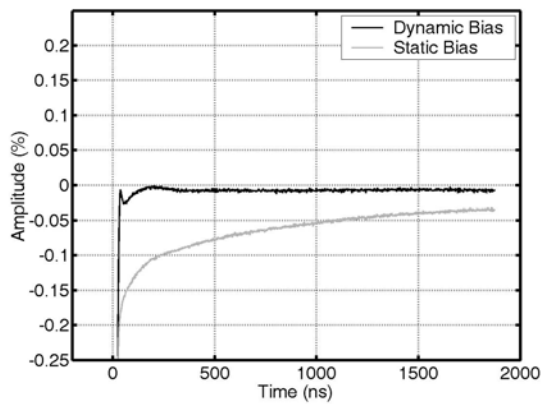

Fig. 8. Comparator probe step settling behavior.

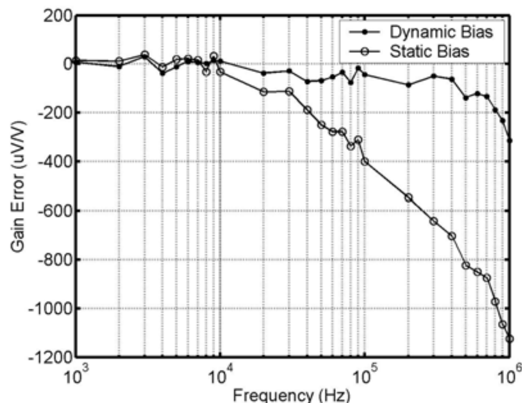

Fig. 9. Comparator probe frequency response.

Performance improvement with dynamic biasing can also be seen in the frequency domain. Fig. 9 shows probe gain flatness for the dynamic and static bias cases. The comparator's frequency response was measured against a thermal transfer standard traceable to NIST using a swept sine test method. Gain in the static bias case is down 1100 μV/V at 1 MHz. In the dynamic bias case, gain flatness is improved to within 300 μV/V from dc to 1 MHz.

6. CONCLUSION

A sampling comparator with low thermal error suitable for use in high speed, high accuracy digitizers has been described. The low thermal error is achieved though a technique that dynamically varies the input stage bias current as a function of differential signal amplitude. Requiring no additional signals to those of a conventional sampling comparator, the device can serve as a drop-in replacement for existing ADC designs. Results from testing a proof-of-concept prototype device have been presented. Most significant is the improvement in step settling response resulting from the dynamic minimization of differential power dissipation in the input tracking stage.

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