Asymmetric Energy Distribution of Interface Traps in n- and p-MOSFETs With HfO_2 Gate Dielectric on Ultrathin SiON Buffer Layer

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***Abstract*—The variable rise and fall time charge-pumping technique has been used to determine the energy distribution of interface trap density ($D_{\rm it}$) in MOSFETs with a HfO_2 gate dielectric grown on an ultrathin ($<$1 nm)–SiON buffer layer on Si. Our results have revealed that the ($D_{\rm it}$) is higher in the upper half of the bandgap than in the lower half of the bandgap, and are consistent with qualitative results obtained by the subthreshold current–voltage (I–V) measurements, capacitance–voltage (C–V), and ac conductance techniques. These results are also consistent with the observation that n-channel mobilities are more severely degraded than p-channel mobilities when compared to conventional MOSFETs with SiO_2 or SiON as the gate dielectric.**

***Index Terms*—Charge pumping, energy distribution, HfO_2 gate dielectric, high-κ, interface trap density, MOSFETS, subthreshold swing (SS).**

I. Introduction

MOST REPORTS published so far on the use of high-κ or high-κ–SiO_2 stacks gate dielectrics to replace SiO_2 in scaled CMOS technology show significantly degraded channel carrier mobility in a MOSFET, which has held back the implementation for next-generation devices. The causes of such degradation are still not fully understood; Coulomb scattering [1], remote phonon scattering [2], and charge trapping [3], [4] have been proposed to be primarily responsible, although opposing evidence has recently been reported [5]. In any case, it is clear that a viable high-κ gate dielectric on Si must at least have a low density of interface traps in order to realize the desired high transconductance for advanced CMOS technology. In this letter, we report the energy distributions of interface traps, obtained by the use of the charge-pumping (CP) technique [6], in n- and p-MOSFETs with a HfO_2 gate dielectric grown on an ultrathin ($<$1 nm) SiON buffer layer on Si. Various versions of the CP technique have been extensively used to measure interface-trap density in MOSFETs [7]–[9]. Most researchers use CP pulses with a fixed rise time and fall time to obtain the total density of interface traps across a portion of the Si bandgap. In this study, we apply the variable rise and fall time CP procedure, as described in [6] and [7], to probe the energy distribution of interface-trap density in high-κ HfO_2-gated MOSFETs. The results are complementarily verified with the subthreshold current–voltage (I–V), mobility simulation, capacitance-voltage (C–V), and ac conductance techniques.

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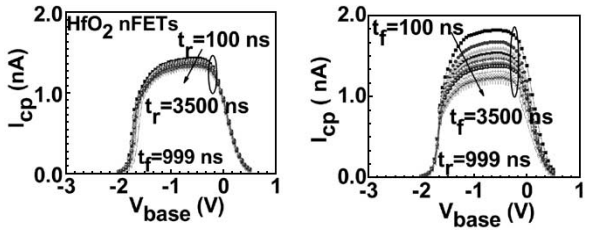
II. Device Details and Experiments

Both n-channel and p-channel MOSFETs were fabricated by using a conventional CMOS process flow with a poly-Si gate [3]. The gate dielectrics were fabricated by atomic layer deposition of 6-nm HfO_2 on an ultrathin layer of pre-grown silicon oxynitride ($<$1 nm); the equivalent oxide thickness (EOT) of the gate stack is 2.4 nm. This study focused on transistors with a channel length (L) of 2 μm and a width (W) of 100 μm, although other sizes ($L < 2\,\mu$m) have also been investigated with similar results [6]. Note that the interfacial transition region between HfO_2 and Si is quite complicated and very thin, and therefore the interface traps we measure include all electrically active defects at or near the interface that respond to charge-pumping signals. The gate tunneling current is much smaller than the CP currents in the frequency range that we measured, either at flatband or at threshold voltage.

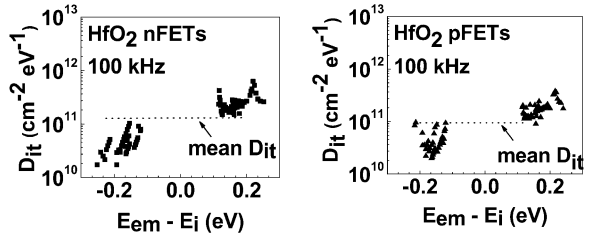
The charge-pumping measurement was performed with both source/drain (S/D) regions grounded while sweeping the base (V_b) level of a constant-amplitude (V_a) gate pulse from inversion to accumulation. By measuring the CP currents ($I_{\rm cp}$) with variable fall and rise times, one can obtain the energy distribution of the interface traps in a relatively large part of the forbidden energy gap on both sides of midgap. More specifically, the energy is gradually swept through the electron emission energy level ($E_{\rm em,e}$) above midgap by changing the fall time (t_f) of the gate pulse while keeping the rise time (t_r) fixed. Likewise, the energy is gradually swept through the hole emission energy level ($E_{\rm em,h}$) below midgap by changing the rise time (t_r) while keeping the fall time (t_f) fixed [6], [7]. The relevant equations are given in [6, Table 1]. Note that (4) and (5) in [6] are approximations derived with the assumption that $D_{\rm it}$ is a slow function of energy, and the errors will become significant where $D_{\rm it}$ changes rapidly with energy.

Subthreshold drain current versus gate voltage (I_d–V_g) measurements were performed on the same samples to verify the results obtained from CP, since subthreshold swings are proportional to the interface trap density in the weak inversion region



(a) (b)

Fig. 1. (a) Weak rise-time dependence of charge-pumping current curves for fixed fall time of 999 ns for HfO_2-gated n-MOSFET. (b) Strong fall-time dependence of charge-pumping current curves for fixed rise time of 999 ns for HfO_2-gated n-MOSFET. A trapezoidal wave form was used.



(a) (b)

Fig. 2. Energy distribution of interface traps as determined by rise and fall time dependence of charge-pumping currents for HfO_2-gated MOSFETs. (a) n-MOSFET. (b) p-MOSFET.

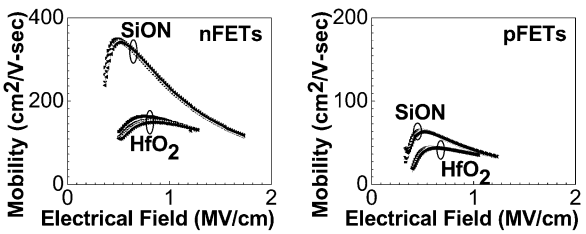
[10]. The mobility simulation program compiled by Hauser has also been applied [11].

III. Results And Discussion

Fig. 1(a) shows a very weak dependence of $I_{\rm cp}$ on rise time for a given fall time of 999 ns for a representative HfO_2 gated n-MOSFET $(L \times W = 2 \times 100\ \mu\text{m})$. This indicates that the density of the interface traps in the lower half of band gap is small, see (5) in [6]. On the other hand, Fig. 1(b) shows a strong dependence of $I_{\rm cp}$ on the fall time for a given rise time of 999 ns, indicating a high density of interface traps in the upper half of the bandgap, see (4) in [6]. The p-MOSFET shows a similar rise and fall time dependence of CP characteristics, although the data are not shown here for brevity.

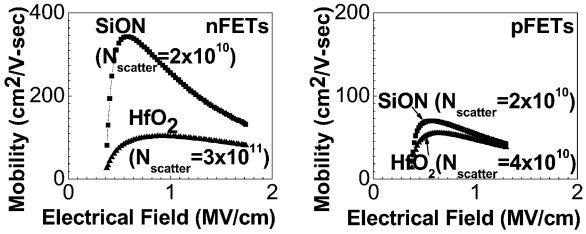
Fig. 2(a) shows the density of interface traps as a function of energy in the Si bandgap extracted from the data in Fig. 1 for the n-MOSFETs. Using the same procedure, we have also extracted the density of interface traps as a function of energy in the Si bandgap for a representative p-MOSFET, and the results are shown in Fig. 2(b). It is obvious that in both cases the $D_{\rm it}$ is higher in the upper half of the bandgap than in the lower half of the bandgap. One should emphasize that room-temperature CP data does not allow us to extract $D_{\rm it}$ closer to the band edges because of thermal emission [7], but the trend is obvious. The extracted mean values of $D_{\rm it}$ of SiON-gated n- and p-MOSFET control samples ($2\text{–}3 \times 10^{10}\ \text{cm}^{-2}\text{eV}^{-1}$) are about one order of magnitude lower than that with the HfO_2 gate stack ($1\text{–}3 \times 10^{11}\ \text{cm}^{-2}\text{eV}^{-1}$).

We also compared the subthreshold characteristics of the n-MOSFET and p-MOSFET with HfO_2 gate dielectric discussed above and found that the subthreshold swing (SS) for the n-MOSFET (100 mV/dec) is larger than that for the p-MOSFET (87 mV/dec). Since SS not only depends on the



(a) (b)

Fig. 3. Effective carrier mobility in HfO_2-gated and SiON-gated MOSFETs. (a) n-MOSFET. (b) p-MOSFET, where the data for the SiON-gated MOSFETs are substantially similar to the universal mobility data.



(a) (b)

Fig. 4. Effective mobilities of the samples in Fig. 3, simulated by the use of the NCSU Mob2d program.

$D_{\rm it}$ but also on depletion-layer capacitance, we compared the SS values of n-MOSFET and p-MOSFET with a SiON gate dielectric. They were comparable ($\sim$75 mV/dec) and much lower than the ones with the high-κ dielectric stack. The SS value for the n-MOSFET is increased by charging of interface traps in the upper half of the Si bandgap, while that for the p-MOSFET is increased by the charging of interface traps in the lower half of the Si bandgap; the results are consistent with a larger $D_{\rm it}$ in the upper half of the bandgap as determined by CP. It should be noted that SS measurement, being a quasi-dc measurement, includes not only quasi-interface traps, but also slow states (boarder traps), which may not be detected by the relatively high frequency CP.

The ac conductance measurement [12] and C–V data were also used to verify the CP results qualitatively, as reported previously [6], and the results are again consistent with the asymmetric interface trap distribution observed by other techniques.

We suspect that the gross asymmetry of the $D_{\rm it}$ distribution in high-κ gated MOSFETs may be partially responsible for the frequent observation that the channel mobility in n-MOSFETs tends to degrade more severely than in p-MOSFETs with high-κ gate dielectrics [13], [14], because the electrons in the n-channel interact with interface traps in the upper half of the bandgap, while holes in the p-channel interact with interface traps in the lower half of the bandgap. Fig. 3(a) and (b) compares the channel mobility data between a HfO_2-gated n-MOSFET and its p-MOSFET counterpart. The data for the control samples with high-quality SiON as the gate dielectric are also shown for comparison. HfO_2-gated n-MOSFETs exhibit more severe mobility degradation than the p-MOSFET counterpart, which is consistent with the results reported by others [13], [14] and is also consistent with the higher density of interface traps in the upper half of the Si bandgap. We also used the NCSU Mob2d program compiled by Hauser [11] to simulate mobility by assuming the interface scattering density is equivalent to the interface trap density. The results shown in Fig. 4 illustrate that

the asymmetry in interface trap density alone can degrade the mobility of n-MOSFETs more than that of p-MOSFETs. The results on SiON samples are consistent with numerous previous experimental studies [15]–[18].

It is interesting to note that, very recently, Fermi-level pinning at the polySi–metal HfO_2 interface just below the conductance band (E_c) was proposed [19]. This idea is not inconsistent with our results, provided that the $D_{\rm it}$ continues to increase as one approaches E_c and that there are even higher densities of $D_{\rm it}$ for a polySi–HfO_2 interface than for a single-crystal Si–HfO_2 interface.

IV. Conclusion

By analyzing the rise and fall time dependence of charge-pumping data, we have revealed that $D_{\rm it}$ above midgap is much higher than that below the midgap in both n-channel and p-channel HfO_2-gated MOSFETs. These results are consistent with the subthreshold I–V characteristics of these MOSFETs and the qualitative outputs obtained by C–V and ac conductance techniques. We believe that the gross asymmetry of the $D_{\rm it}$ distribution may be partially responsible for the much more severe degradation of mobility in the n-MOSFET than in its p-MOSFET counterpart.

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