Semiconductor Microelectronics and Nanoelectronics Programs

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Disclaimer: Certain commercial equipment and/or software are identified in this report to adequately describe the experimental procedure. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the equipment and/or software identified is necessarily the best available for the purpose.

References: References made to the *International Technology Roadmap for Semiconductors* (ITRS) apply to the most recent edition, dated 2001. This document is available from the Semiconductor Industry Association (SIA), 181 Metro Drive, Suite 450, San Jose, CA 95110, phone: (408) 436-6600; fax: (408) 436-6646.

The reader will notice that there are acronyms and abbreviations throughout this document that are not spelled out due to space limitations. We have listed the acronyms and abbreviations in an appendix at the end of this document. We also have included a list of the NSMP projects that demonstrate the synergism resulting from this matrix-managed program.

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Welcome and Introduction

Welcome

The microelectronics industry supplies vital components to the electronics industry and to the U.S. economy, enabling rapid improvements in productivity and in new high technology growth industries such as electronic commerce and biotechnology. The National Institute of Standards and Technology, NIST, in fulfilling its mission of strengthening the U.S. economy, works with industry to develop and apply technology, measurements and standards; and applies substantial efforts on behalf of the semiconductor industry and its infrastructure. This report describes the many projects being conducted at NIST that constitute that effort.

Historical Perspective

NIST's predecessor, the National Bureau of Standards (NBS), began work in the mid-1950s to meet the measurement needs of the infant semiconductor industry. While this was initially focused on transistor applications in other government agencies, in the early 1960s the Bureau sought industry guidance from the American Society for Testing and Materials (ASTM) and the (U.S.) Electronic Industries Association (EIA). ASTM's top priority was the accurate measurement of silicon resistivity. NBS scientists developed a practical nondestructive method ten times more precise than previous destructive methods. The method is the basis for five industrial standards and for resistivity standard reference materials widely used to calibrate the industry's measurement instruments. The second project, recommended by a panel of EIA experts, addressed the "second breakdown" failure mechanism of transistors. The results of this project have been widely applied, including solving a problem in main engine control responsible for delaying the launch of a space shuttle.

From these beginnings, by 1980 the semiconductor metrology program had grown to employ a staff of sixty with a $6 million budget, mostly from a variety of other government agencies. Congressional funding in that year gave NBS the internal means to maintain its semiconductor metrology work. Meeting industrial needs remained the most important guide for managing the program.

Industrial Metrology Needs

By the late 1980s, NBS (now NIST) recognized that the semiconductor industry was applying a much wider range of science and engineering technology than the existing NIST program was designed to cover. The necessary expertise existed at NIST, but in other parts of the organization. In 1991, NIST established the Office of Microelectronics Programs (OMP) to coordinate and fund metrological research and development across the agency, and to provide the industry with easy single point access to NIST's widespread projects. Roadmaps developed by the (U.S.) Semiconductor Industry Association (SIA) have independently identified the broad technological coverage and growing industrial needs for NIST's semiconductor metrology developments. As the available funding and the scope of the activities grew, the collective name became the National Semiconductor Metrology Program (NSMP), operated by the OMP.

The NSMP has stimulated a greater interest in semiconductor metrology, motivating most of NIST's laboratories to launch additional projects of their own and to cost-share OMP-funded projects. The projects described in this book represent this broader portfolio of microelectronics projects. Most, but not all, of the projects described are partially funded by the NSMP, which provided a $12 million budget in fiscal year 2003.

Fostering NIST's Relationships with the Industry

NIST's relationships with the SIA, International SEMATECH (ISMT), and the Semiconductor Research Corporation (SRC) are also coordinated through the OMP. Staff from OMP represent NIST on the SIA committees that develop the International Technology Roadmap for Semiconductors (ITRS) as well as on numerous SRC Technical Advisory Boards. OMP staff are also active in the semiconductor standards development work of the ASTM, the Deutsches Institut für Normung (DIN), the EIA, the International Organization for Standardization (ISO), and Semiconductor Equipment and Materials International (SEMI).

Learn More about Semiconductor Metrology at NIST

This publication provides summaries of NIST's metrology projects for the silicon semiconductor industry and their suppliers of materials and manufacturing equipment. Each project responds to one or more metrology requirements identified by the industry in sources such as the ITRS. NIST is committed to listening to the needs of industry, working with industry representatives to establish priorities, and responding where resources permit with effective measurement technology and services. For further information, please contact NIST as follows:

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Lithography

Advances in lithography have largely driven the spectacular productivity improvements of the integrated circuit industry, a steady quadrupling of active components per chip every three years over the past several decades. This continual scaling down of transistor dimensions has allowed more and more components on a chip, lowered the power consumption per transistor, and increased the speed of the circuitry. The shrinking of device dimensions has been accomplished by shortening the wavelength of the radiation used by the lithography exposure tools. The industry at this point has moved into the deep ultraviolet (DUV) spectrum. Currently, exposure tools operating at 193 nm are being introduced, and exposure tools operating at 157 nm are in development. Looking beyond the deep ultraviolet, extreme ultraviolet radiation (EUV) at 13 nm is being investigated, and demonstration tools are being designed and assembled. The overall goal of this task is to support these developments in DUV and EUV. The areas of emphasis are lens materials, laser calorimetry, radiation detector sensitivity and damage, EUV lens metrology, and metrology for the development of advanced phoresist materials for both DUV and EUV.

Metrology Supporting Deep Ultraviolet Lithography

Technical Contacts:
J. H. Burnett
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"It's an excellent service NIST has performed for the entire industry. The kind of thing NIST is there for – to identify issues before the train wreck takes place."

Mordechai Rothschild, Massachusetts Institute of Technology's Lincoln Laboratory

Goals

Develop solutions to key metrology issues confronting the semiconductor lithography industry. These include development of measurement methods and standards for characterizing deep ultraviolet (DUV) laser sources, detectors, and materials. One focus is on delivering high-accuracy measurements of DUV detector parameters and materials properties of immediate need by the industry. There is ongoing activity in the following areas: standards development, calibration services, characteriza-tion of optical materials, sources, and detectors, in addition to advising customers on in-house measurements.

Customer Needs

Increasing information technology requirements have yielded a strong demand for faster logic circuits and higher-density memory chips. This demand has led to the introduction of DUV laser-based lithographic tools for semiconductor manufacturing. These tools, which employ KrF (248 nm) and ArF (193 nm) excimer lasers, have led to an increased demand for accurate measurements at DUV laser wavelengths. Next generation tools employing F_2 (157 nm) excimer lasers, projected for insertion into production lines by 2005, require even higher accuracy measurements. To support these efforts, the National Institute of Standards and Technology (NIST), with International SEMATECH support, has initiated a DUV metrology program focusing on the characterization of DUV optical materials, sources, and detectors.

The potential solutions for lithographic systems are discussed in the 2001 International Technology Roadmap for Semiconductors on page 14 of the Lithography Section, and in Figure 34 on page 15. "Optical lithography is the mainstream approach through the 90 nm node,—." The emphasis is on 193 nm and 157 nm light source systems.

Technical Strategy

1. Beginning with the first edition of the National Technology Roadmap for Semiconductors (NTRS) in 1992, the semiconductor industry has made an organized, concentrated effort to reduce the feature sizes of integrated circuits. As a result, there has been a continual shift towards shorter exposure wavelengths in the optical lithography process. Because of their inherent characteristics, deep ultraviolet (DUV) lasers, specifically KrF (248 nm) and ArF (193 nm), and more recently F_2 (157 nm) excimer lasers, are the preferred sources for high-resolution lithography at this time. To meet the laser metrology needs of the optical lithography community, we have developed primary standards and associated measurement systems at 193 and 248 nm, and are in the process of developing standards at 157 nm measurements, Fig. 1.

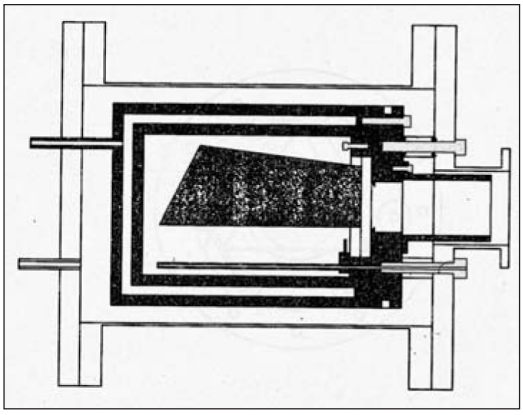


Figure 1. Excimer laser calorimeter for 157 nm measurements.

DELIVERABLES: Develop a 157 nm excimer laser primary standard and calibration service to provide support for the next generation of optical lithography. 1Q 2003

2. To meet the semiconductor industry's demands for more rapid, accurate measurements of excimer laser power and energy, we are building a system to determine the nonlinear response of an excimer laser detector, Fig. 2. This system uses a correlation method to measure the nonlinear response of pulsed-energy detectors at 248 nm. The response of the detector under test is compared to the corresponding response of a linear monitor detector as a function of incident laser pulse energy. This method addresses the difficulties related to large pulse-to-pulse instability of most excimer laser and delivers measurement results with an expanded uncertainty (k=2) of 0.8 %.

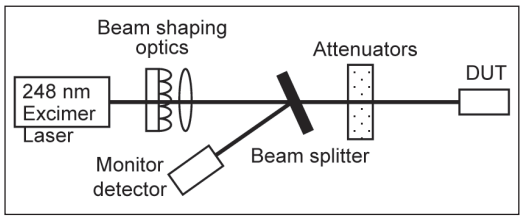


Figure 2. Schematic diagram of 248 nm nonlinear response system.

DELIVERABLES: Add capability to perform nonlinearity measurements at 248 nm. 4Q 2003

3. High-accuracy measurements of the index properties of UV materials is a requirement for the design of DUV lithography systems. To meet this demand NIST has developed methods to make measurements of the DUV refractive index, as well as its wavelength, temperature, and stress dependencies to the high accuracy needed. Index variations and birefringence have become a limiting factor in the development of the optics for lithography systems, especially at 157 nm. To address this problem we have developed unique VUV polarimetry and Twyman-Green interferometer systems to measure 157 nm index variation in lens materials due both to external stress and grown-in defects.

DELIVERABLES: Characterize index inhomogeneities of DUV materials near 157 nm at the sub ppm level. 4Q 2003

4. In the course of our measurements we discovered that in addition to index variations and birefringence due to material defects and external stress, there are also index variations and birefringence *intrinsic* to the material. The commonly-accepted assumption that the cubic symmetry of the crystals used would ensure the isotropy of the optical properties, in fact breaks down due to the finite value of the photon momentum q. This previously-neglected effect on ultraviolet optics has a $1/\lambda^2$ wavelength dependence, and is negligible at visible wavelengths, where the index homogeneity and birefringence are measured. However, at 157 nm the effect is large (≈ten times the 157 nm birefringence specification), and this has serious implications on 157 nm lithography system design and performance. This intrinsic birefringence must be accurately characterized for all materials considered for optics in 157 nm systems, including the mixed crystals $Ca_{1-x}Ba_xF_2$ we are co-developing that have the potential of having negligible intrinsic birefringence.

DELIVERABLES: Develop and characterize $Ca_{1-x}Sr_xF_2$ mixed crystals, produced to eliminate intrinsic birefringence. 4Q 2003

5. We are developing a new method for measuring the refractive index of transmissive samples to a high accuracy ≈1 ppm in the DUV and VUV using a VUV FT spectrometer. This method is directed to measurements down to 135 nm using synchrotron radiation as a continuum source.

DELIVERABLES: Measurements of VUV index properties of optical materials important for the lithography industry, using an interferometric technique in conjunction with SURF III. 4Q 2003

6. Our efforts for complete characterization of the optical properties of materials involve measuring the transmittance, reflectance, surface and bulk scatter, and surface and bulk absorption. This characterization is done on one of the beam lines at the NIST Synchrotron Ultraviolet Radiation Facility (SURF) which is devoted to material and detector characterization in the wavelength range 120 nm – 320 nm. We have used this facility to characterize various samples of calcium fluoride where the transmittance and reflectance was measured with an uncertainty of better than 1%.

SURF III acts as the primary standard for both sources and detectors in the DUV and VUV spectral region.

DELIVERABLES: Achieve a 0.1% standard uncertainty of UV irradiance from 3 nm to 400 nm, and enable accurate, direct radiance, and irradiance comparisons with new as well as existing source transfer standards. 4Q 2002

7. Monochromatized radiation from SURF III along with a cryogenic radiometer is used to provide absolute detector-based radiometric calibrations in the spectral range from 125 nm to 320 nm with a standard uncertainty of better than 1%. This facility has also been used to study the degradation in diodes induced by exposure to UV radiation. A wide variety of diodes (Si diodes from Hamamatsu, nitrided Si diodes from IRD, PtSi, GaN, GaP, GaAsP, and diamond) were characterized for spectral responsivity and uniformity mapping, and the degradation in these diodes at 130 nm was also measured.

A new facility for characterizing the degradation of diodes to excimer radiation at 157 has been completed. This facility allows the measurement of the spectral responsivity of the devices in the spectral range from 130 nm to 500 nm along with the measurement of the reflectivity of the diodes as the devices are irradiated by the excimer

radiation. This allows identification of potentially stable diodes for UV irradiance measurements. The facility can also be used to characterize other types of detectors such as photochromic films.

DELIVERABLES: Characterize the stability of variety of semiconductor diodes to excimer radiation at 157 nm. 2Q 2002

8. We plan to use the synchrotron radiation in conjunction with a cryogenic radiometer to measure the transmittance, reflectance, surface and bulk losses, which would lead to a complete optical characterization of the transmissive samples. Capability will also be developed to make polarization dependent measurements in the spectral range from 125 nm to 320 nm.

DELIVERABLES: Build a state of the art facility for an accurate and complete characterization of the optical properties of transmissive materials. 4Q 2002

Accomplishments

■ We have developed a system to characterize the nonlinear response of a 193 nm excimer laser detector based on the correlation method. The method and system solves measurement difficulties associated with the temporal and spatial fluctuations of excimer laser pulse energy. The system has a dynamic range of 30 µJ to 50 mJ of pulse energy. The typical measurement uncertainty is 0.8 %. Several DUV detectors were tested. Using this system, one can easily determine the origin of a detector's nonlinear response, such as those due to the incident pulse energy, range discontinuities associated with detector gain, and detector background noise, see Fig. 3. We have discovered detectors having nonlinearity as high as 8 %.

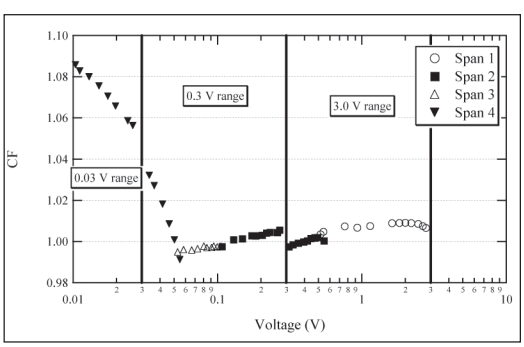


Figure 3. Nonlinearity measurement result of a 193 nm pulsed laser energy detector. CF is the correction for the detector's nonlinear response. The response is measured in four spans, covering 2.5 meter settings. The large degree of nonlinearity at the low end of the meter range is due to background effects.

■ We have determined the damage thresholds and lifetimes of several materials using 157 and 193 nm excimer lasers and a beam profile technique similar to ISO 11254-2, Fig. 4. We made these measurements to select an appropriate absorbing material for use in our primary standard laser calorimeter for 157 nm excimer laser power measurements. The materials we tested were nickel-plated sapphire, chemically-vapor-deposited silicon carbide (CVD SiC), nickel-plated copper, and polished copper. Applied pulse energy densities (or dose) ranged from 80 to 840 mJ/cm^2. We determined the applied dose from a series of laser beam profile measurements. Silicon carbide had the highest damage threshold: 730 mJ/cm^2 per pulse. For this reason, and for its high thermal and electrical conductivities, we have chosen silicon carbide as the absorber material for the 157 nm calorimeter.

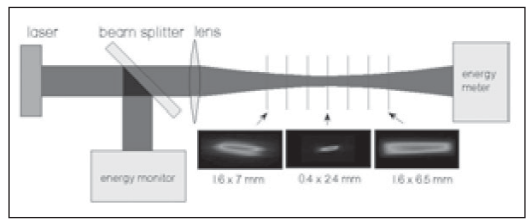
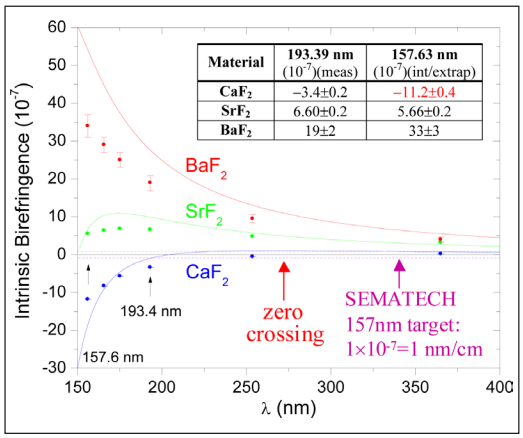


Figure 4. Damage threshold measurements. Beam profiles were recorded and characterized at 22 planes along the propagation axis using a CCD camera and quantum converter. Three energy density distributions at inner- and outer-most positions, together with their dimensions, are shown. The dimensions are based on the calculation of the second moments according to ISO 11146.

■ Using a unique UV polarimetry system we developed, we made the first measurements of an intrinsic birefringence in CaF_2 and BaF_2. These values turned out to be over ten times the 157 nm lithography birefringence target value, and have forced all 157 nm system designs to be substantially redesigned. We developed the complete theory of the effect, now fully accepted, and analyzed its angular dependence. From this we first suggested a compensation approach based on combining lenses of different crystal axis orientations. All 157 nm system designs now utilize this correction approach. We also showed that since the intrinsic birefringence of CaF_2 and BaF_2 have opposite signs, then a mixed crystal $Ca_{1-x}Ba_xF_2$ can in principle be made which has zero intrinsic birefringence at 157 nm, Fig. 5. We have worked with crystal growers to develop this material and characterize its optical properties.



Material	193.39 nm (10^{-7})(meas)	157.63 nm (10^{-7})(int/extrap)
CaF_2	−3.4±0.2	−11.2±0.4
SrF_2	6.60±0.2	5.66±0.2
BaF_2	19±2	33±3

Figure 5. Measured (symbols) and calculated (curves) intrinsic birefringence of CaF_2. SrF_2, and BaF_2. The figure shows opposite signs of the effect for CaF_2, and SrF_2 and BaF_2.

■ Immersion lithography has been identified as a possible way to extend the commercial viability of 193 nm lithography technology. However, various technical issues with immersion lithography cannot be resolved without accurate data on the refractive index (n) of the immersion fluid (water), and its dependencies on temperature (dn/dT), pressure (dn/dP), dissolved gas content, and impurities. We have made the first accurate measurements of these index properties of water near 193 nm using both the goniometric method and the interferometric method, with consistency of results. These values are now being used by the semiconductor industry for design of immersion lithography tools.

■ The stability of semiconductor diodes under irradiation from an excimer laser operating at 157 nm has been evaluated. We have built a facility at SURF III that allows simultaneous exposure of photodiodes to excimer radiation, see Fig. 6, and synchrotron radiation. Measurements of the spectral responsivity can be made in the spectral range from 130 nm to 320 nm with a standard uncertainty of less than 1%. The intense, pulsed laser radiation was used to expose the photodiodes for varying amounts of accumulated irradiation whereas the low intensity, continuously-tunable cw radiation from the synchrotron source was used to characterize the photodiodes. The changes in the spectral responsivity of different kinds of diodes such as UV silicon, GaP, GaAsP, PtSi, diamond, and GaN were measured for a large range of total accumulated dose from an F_2 excimer laser operating at 157 nm. Differing amounts of changes were seen in different diodes depending on the total excimer irradiation dose and they showed different spectral changes in the responsivity as well. This yields important information about the mechanism responsible for the degradation of photodiodes.

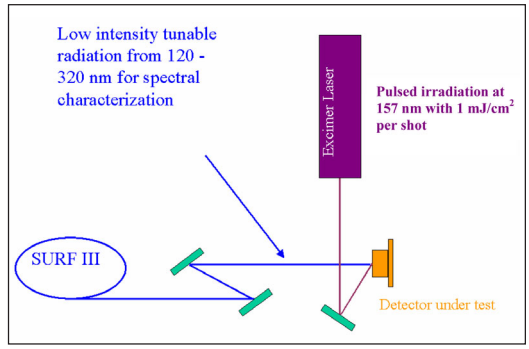


Figure 6. Photodetector damage experiment for 157 nm radiation.

■ We have also characterized pyroelectric detectors which are commonly used for high-power laser application. In the vacuum UV to near UV range, pyroelectric detectors are commercially available because of important applications in areas like semiconductor photolithography. Instead of calibrating these detectors using high-power radiation, we performed measurements with low-power UV radiation at beamline 4 of the SURF III. To accommodate the pulse detection nature of the pyroelectric detectors, we installed a 10 Hertz tuning fork chopper at beamline 4 and lock-in amplifiers were used for detector signal processing. Several commercial pyroelectric detectors were tested at our facility. We found that in most cases, the manufacturer-supplied amplifiers were too noisy for our light intensity on the order of one microwatt. Subsequently, a low-noise amplifier was constructed and installed near the detection head. In addition, for several high reflectance pyroelectric detectors, we also measured the reflectance of the pyroelectric element to check the internal quantum efficiency of the detector.

■ We have constructed and characterized a probe that is suitable for accurate measurements of irradiance in the vacuum ultraviolet spectral range. Many industrial applications such as UV curing, photolithography, or semiconductor chip fabrication require accurate measurement of the irradiance and will benefit from having such a stable, accurate UV probe. The probe was characterized at various wavelengths ranging from 157 nm to 325 nm, encompassing many of the

important industrial application wavelengths. The principle of measurement of the irradiance is based on scanning the probe in a light field and measuring the spectral responsivity on a grid with regular spacing. Measurement of the spectral responsivity in the center of the probe along with the integrated total responsivity yields the spectral irradiance, Fig. 7. This method can alternatively be used to calculate aperture areas as well by measuring the ratio of the total responsivity and the responsivity in the center.

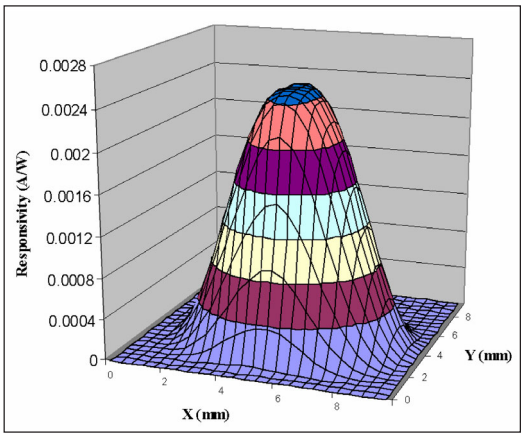


Figure 7. Measurement of the areal responsivitity of a UV probe at 157 nm.

Collaborations

MIT Lincoln Laboratory, Mordechai Rothschild; DUV detector damage, immersion optical fluid measurements.

Recent Publications

"A Primary Standard for 157 nm Excimer Laser Measurements," C. L. Cromer, M. L. Dowell, R. D. Jones, D. A. Keenan, S. Yang, 2003 Int'l Conf. on Characterization and Metrology for ULSI Tech. (March 2003) *in press*.

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"Measurement of the refractive index and thermo-optic coefficient of water near 193nm," J. H. Burnett and S. Kaplan, to appear in, *Optical Microlithography XVI*, Proceedings of SPIE Vol. 5040 (2003).

Metrology Supporting EUV Lithography

Goals

Provide leading-edge metrology for the development and characterization of optical components and detectors used in Extreme Ultraviolet Lithography (EUVL). (EUVL utilizes radiation at 13.4 nm.)

Customer Needs

An intense international effort is presently underway to develop EUVL for the patterning of wafers beginning in 2007. A milestone in the U.S. effort was the building of an alpha-tool called the ETS (Engineering Test Stand) that is housed at the Sandia National Laboratory. While the ETS has demonstrated the feasibility of EUVL for 70 nm design rules and beyond, much work needs to be done to improve the throughput, mask fabrication, and lifetime of the optics.

High resolution imaging with EUV radiation was not possible until the development of multilayer EUV mirrors in the mid 80s. This development has spawned the relatively new field of EUV optics and its associated set of new metrological challenges. Among these are: 1) precise EUV reflectivity maps; 2) EUV dosimetry; 3) EUV damage characterization; and 4) nanometer level optical figure measurement.

Technical Strategy

1. Precise EUV reflectivity maps

The present NIST/DARPA EUV Reflectometry Facility is located on a multipurpose beamline on the NIST Synchrotron Ultraviolet Radiation Facility (SURF III) storage ring. The beamline can provide a monochromatic beam of EUV or soft x-ray radiation in the 3 nm to 40 nm (400 eV to 30 eV) spectral range. Although primarily designed to serve the EUVL community by providing accurate measurements of multilayer mirror reflectivities, this beamline with its associated sample chamber has been used for many other types of measurements since the beamline's commissioning in early 1993. Among the other measurements performed recently are grating efficiencies, photocathode conversion efficiencies, phosphor conversion efficiencies, film dosimetry, and determination of EUV optical constants through angle dependent reflectance measurements. A diagram of the NIST/DARPA EUV Reflectometry Facility is shown in Fig. 1.

Currently the NIST/DARPA facility is the only one in the U.S. large enough to measure optics larger than 200 mm in diameter. A recent international intercomparison among NIST and several other labs demonstrated reflectivity accuracy of 0.3 % and wavelength accuracy of 0.01 nm. Plans are underway to reduce wavelength uncertainty by an order of magnitude.

DELIVERABLES: Full reflectivity map of EUV mirrors up to 40 cm in diameter and 45 kg mass on an as needed basis for the EUVL community. Reflectivity and transmittance measurements of metrology components for International SEMATECH.

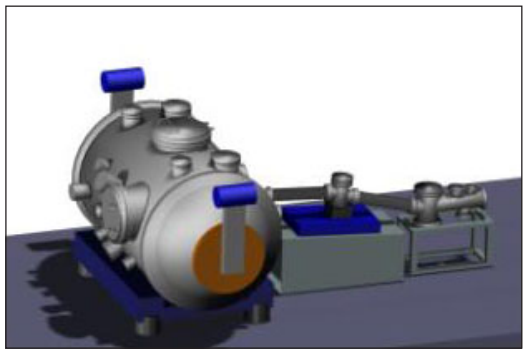

Figure 1. Diagram of NIST/DARPA EUV Reflectometry Facility, including the sample chamber and monochromator.

2. EUV Dosimetry

NIST is the primary national source for the radiometric calibration of detectors from the infrared to the soft x-ray regions of the spectrum. Until recently all NIST-characterized EUV photodetectors were calibrated on the SURF storage ring, which is essentially a cw source. Recently we have designed and built a pulsed EUV source similar to the source being used in the ETS to calibrate EUV detectors for characterizing sources as well as wafer-plane dosimeters to be used in EUVL. A schematic of the pulsed radiometric facility is shown in Fig. 2.

Two major concerns arise when using solid state photodiodes for detection of short pulse length radiation. First, while the average power may be quite modest, the peak power can be quite high. For example, a 10 Hz laser with an average power of 10 mW has a peak power of 100 kW for a 10 ns pulse. Photodiode saturation may seriously affect the linearity of EUVL dosimeters, even at fairly

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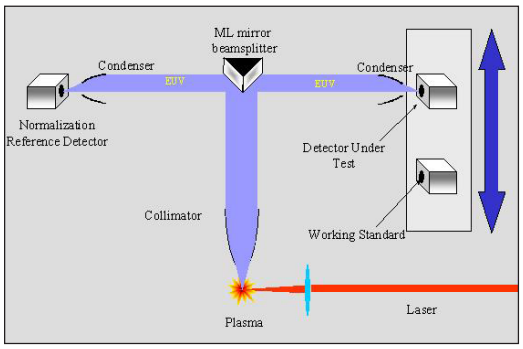

Figure 2. Schematic of Pulsed Radiometric Facility.

low average power levels. We have measured the limit of the linear operating range for an EUV sensitive Si photodiode using 532 nm radiation as a proxy for 13.4 nm; the absorption characteristics in Si are nearly identical. We have found that the photodiode responsivity is an inherently non-linear function of pulse energy, but the responsivity can be fit by a calibration function having two constant parameters. Use of the non-linear calibration function allows the photodiode to be used with reasonable uncertainty even when the responsivity has decreased due to saturation effects by as much as a factor of two. Defining the limit of linear operation as the pulse energy at which there is a loss of responsivity of 2 %, the total charge collected from a Si photodiode is a linear function of pulse energy at peak powers of 1 W (for an unbiased device) to 5 W (for a reverse bias of 10 V). The peak voltage developed is a linear function of pulse energy from 60 mW (unbiased) to 250 mW (10 V reverse bias). Currently, we are extending these results to determine the effect of the longer pulse lengths typical of EUVL plasma discharge sources, to understand the dependence on pulse energy density, and to explore a range of higher reverse bias conditions. A second concern is the equivalence of the responsivity under pulsed conditions and under the cw conditions of calibration facilities. We have compared the measured responsivity of a Si photodiode under pulsed conditions to the results of a low-power cw calibration. The low-power limit of the non-linear pulsed responsivity function is identical to the low-power cw responsivity with a relative standard uncertainty of 1 %. Thus, the results of a cw calibration may be transferred to a pulsed application if the pulse energy dependence is properly accounted for.

We have developed a model of the physical processes that are responsible for the observed non-linear response function of the photodiodes. The loss of total collected charge is modeled as a result of recombination processes in the device during the electronic readout process. In this model, the decrease in the peak voltage developed arises from an increase in the junction capacitance due to the presence of the photogenerated electron-hole pairs, which act as a polarizable dielectric medium. The model correctly predicts the behavior of both calibration parameters as a function of reverse bias. To date, we have obtained results in the reverse bias range from 0 V to 10 V, and we will shortly be extending our observations to 150 V.

We are currently working to reduce the uncertainty of our cw radiometric scale in the neighborhood of 13 nm wavelength from the current relative standard uncertainty of 4 % to 1 %. We will accomplish this by operating an absolute cryogenic radiometer (ACR) on a high-throughput beamline at the SURF III synchrotron radiation facility and calibrating working standard photodiodes by direct comparison to the radiometer. The improved cw scale will be transferred to the EUVL calibration facility described above to provide a U.S. national radiometric scale for detector-based pulse energy measurements at 13.4 nm wavelength with a relative standard uncertainty of a few percent.

DELIVERABLES: (1) Commission ACR based EUV calibration facility 4Q 2003. (2) Finalize model for pulsed response of photodiode responsivity 4Q 2003. (3) Determine the feasibility of using LPP-based EUV calibration facility to calibrate assembled instrumentation packages. 4Q 2003

3. EUV Damage Characterization

The energetic (91 eV) EUV photons impinging on the mirrors in the vacuum environment of the stepper induce various reactions that can damage the multilayer coatings. Some of the reactions can be attributed to EUV-excited water vapor and EUV-dissociated hydrocarbons. (Both a small amount of residual water and hydrocarbon vapors are present in the stepper environment.) In fact, lifetime tests show that the expected lifetime under present conditions is far short of the year duration needed for economic operation.

We have recently commissioned a beamline that is dedicated to the exposure of multilayer optics under controlled environmental conditions. This effort has been supported by Sandia National Laboratory and International SEMATECH. Multilayer samples with silicon and ruthenium capping layers, provided by Lawrence Livermore

National Laboratory, have been exposed for periods of 60 hours each. The samples resided in a water rich atmosphere under an average EUV intensity of 5 mW/mm^2. The results are shown in Fig. 3. The Si capped sample exposed for 60 hours suffered a degradation in reflectivity of more than 20 % due to oxidation at the surface of the mirror. In contrast, the Ru-capped sample suffered a reflectivity degradation of only 2 % under similar illumination and atmospheric conditions. We are currently adding the capability of introducing additional atmospheric components like hydrocarbons to further simulate the conditions present in a projection optics box. This beamline will provide a valuable tool for the EUV optics development community by permitting long-term exposures of various capping layer schemes under controlled atmospheric conditions.

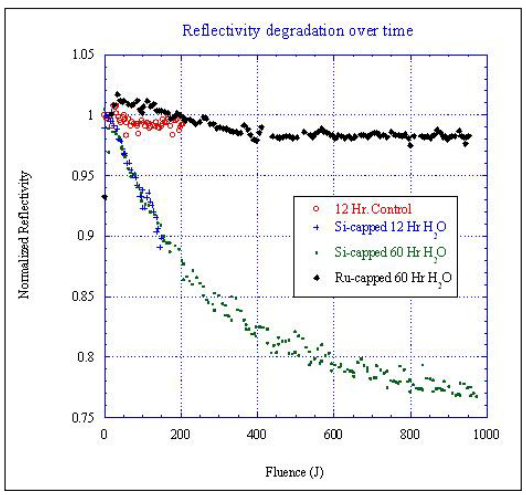

Figure 3. Reflectivity vs. fluence for multilayer samples exposed to EUV radiation.

DELIVERABLES: (1) Install new exposure chamber 4Q 2003; (2) Determine feasibility of multioptic schemes for increased intensity on sample 3Q 2003; (3) Carry out exposures on samples provided by the EUVL community and International SEMATECH.

4. Sub-nm Optical Figure Measurement

The commissioning of the "eXtremely accurate CALIBration InterferometeR" (XCALIBIR) at NIST is now complete and the instrument is fully functional (Fig 4). The XCALIBIR interferometer is a multi-configuration precision phase-measuring interferometer for optical figure measurements of flat, spherical and aspheric optics that can achieve the very low measurement uncertainties that are required for the measurement of EUVL optics.

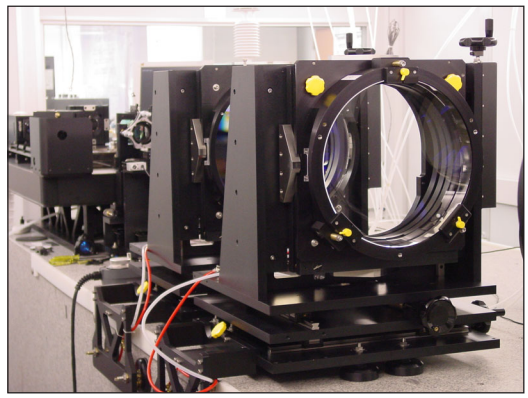

Figure 4. A view of the XCALIBIR interferometer.

The interferometer may be operated in either Twyman-Green or Fizeau configurations. A beam expander in the test arm of the interferometer provides a collimated test beam with 300 mm diameter. Transmission spheres are used to realize a spherical Fizeau interferometer for the testing of spherical and aspheric surfaces. The part under test is mounted on a remotely controlled 5+1-axis mount that can be moved on air bearings along a precision slideway in the direction of the optical axis of the interferometer. A system of three laser-interferometers tracks the movement of the test mount in the direction of the optical axis. A single-mode external cavity diode laser (ECDL) is used as the light source in XCALIBIR. The laser frequency can be modulated to vary the effective temporal coherence over a wide range. Optical fibers with different core diameters are used to couple the light into the interferometer. The spatial coherence of the light source can thus be varied by changing the fiber core diameter.

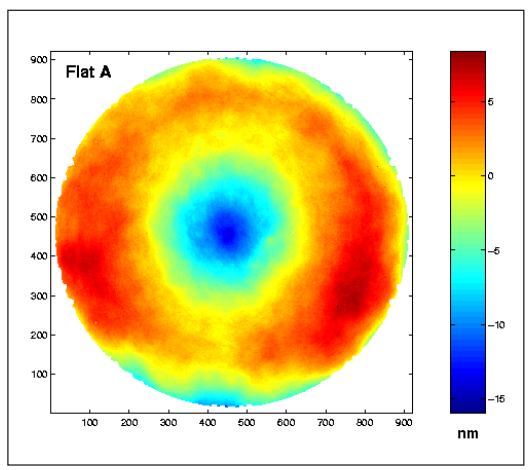

Figure 5. Topography of a 300 mm diameter XCALIBIR reference flat.

The 300 mm diameter reference flats for the flat Fizeau configuration of the interferometer were calibrated with a 3-flat, 6-position self-calibration test. Fig. 5 shows the topography of one of the reference flats. A large number of 3-flat measurements were made to estimate the measurement uncertainty. For each of the flats A, B, and C the *rms* of the difference between the averaged flat solutions and the individual measurements was plotted in a histogram (Fig. 6). A (statistical) measurement *rms* uncertainty of approximately 0.2 nm is evident.

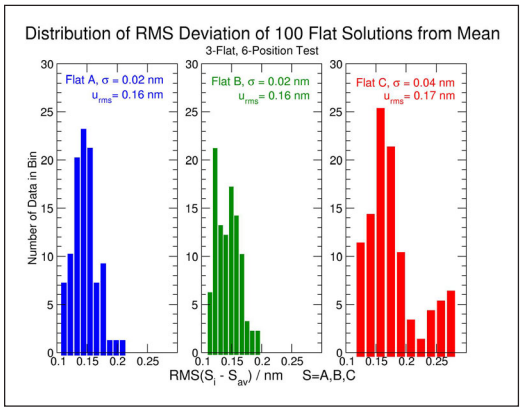

Figure 6. Distribution of rms *deviations from best estimates surface (mean) for three flats A, B, and C.*

When measurements of aspheric optics without null-optics are made, it is frequently the case that only a part, or subaperture, of a surface can be measured at once. For the figure measurement of the entire aspheric surface a number of overlapping subaperture measurements must then be combined, or "stitched" together. We have implemented flexible and robust algorithms for the stitching of subaperture measurements. To demonstrate the power of the stitching algorithm a precision silicon sphere was set up on a rotary table in XCALIBIR and the surface figure error was measured with an F/1.3 transmission sphere. 36 surface error measurements were made at 10° intervals. As shown in Fig. 7, the individual, overlapping, surface error measurements were then stitched together to form a map of the "equatorial region" of the silicon sphere.

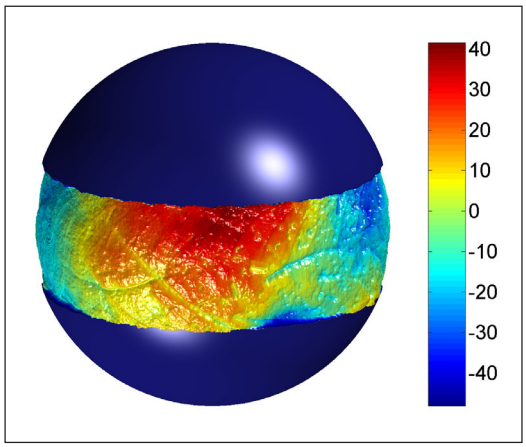

Figure 7. Topography of a precision silicon sphere, stitched from 36 measurements. The figure error is approximately 60 nm PV.

DELIVERABLES: Establish capability for measuring aspheric optics without null optics. (4Q 2003)

Collaborations

VNL at Sandia National Laboratory, Leonard Klebanoff, and Mike Malinowsky, Environmental Team.

VNL at Lawrence Livermore National Laboratory, Eberhard Spiller (consultant), Don Sweeney, Saša Bajt, and Regina Soufli, EUV Multilayer Development and Coating Team.

Recent Publications

"Design and performance of capping layers for EUV multilayer mirrors," S. Bajt, H. N. Chapman, N. Nuygen, J. Alameda, J. C. Robinson, M. E. Malinowski, E. M. Gullikson, A. Aquila, C. Tarrio, S. Grantham in preparation for Proc. SPIE vol. 5037, Emerging Lithographic Technologies VII.

"At wavelength metrology for EUV Lithography," C. Tarrio, S. Grantham, R. E. Vest, and T. B. Lucatorto, proceedings of the First International EUV Lithography Symposium, published on CD by International Sematech, Austin, TX, (2002).

"Accurate reflectometry for Extreme Ultraviolet Lithography at the National Institute of Standards and Technology," S. Grantham, C. Tarrio, and T. B. Lucatorto, Journal of Vacuum Science and Technology **20**, 3080 (2002).

"Facility for extreme ultraviolet reflectometry of lithography optics," C. Tarrio, S. Grantham, T. B. Lucatorto, Metrologia **40**, S229 (2003).

"First results from the improved NIST/DARPA EUV Reflectometry Facility," S. Grantham, C. Tarrio, M. B. Squires, and T. B. Lucatorto, in Proc. SPIE vol. 4688 Emerging Lithographic Technologies VI, p. 348 (2002).

"Response of silicon photodiode to pulsed radiation," R. Vest and S. Grantham. Submitted to Applied Optics.

"Characterization of the response of chromium-doped alumina screens in the VUV using synchrotron radiation," K. J. McCarthy, A. Baciero, B. Zurro, U. Arp, C. Tarrio,. T. B. Lucatorto, A. Morono, P. Martin, and E. R. Hodgson, J. Appl. Phys. **92**, 6541 (2002).

"Uncertainties in Interferometric Measurements of Radius of Curvature," Schmitz, T., Davies, A., and Evans, C., to appear in Proc. SPIE 4451 (2001).

"Interferometric Testing of Photomask Substrate Flatness," Evans C. J., Parks R. E, Shao L-Z., Schmitz T., and Davies A. Proc SPIE Vol 4344, in press.

"Interferometric Metrology of Substrates for VLSI," Evans C. J., Davies A., Schmitz T., Parks R. E, and Shao L-Z., Proc of 2nd EUSPEN International Conference, Turin, May 2001, pp. 388-92.

Polymer Photoresist Fundamentals for Next-Generation Lithography

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"[This work] opens a window of opportunity to construct structure-property relationships between chemical transport mechanisms and ultimate resist resolution. It may also lead to insights into the ultimate, intrinsic resolution limits and critical dimension control of polymer-based imaging materials."

E. Reichmanis and O. Nalamasu, Bell Labs, Lucent Technologies, Science, 297, 349 (2002).

Goals

In this project, we are developing an integrated program involving fundamental studies of photoresist materials to be correlated with resist performance metrics impacting next generation photolithography. We work closely with industrial collaborators to develop and apply high spatial resolution and chemically specific measurements to understand varying material properties and process kinetics at nanometer scales and to provide high quality data needed in advanced modeling programs. The understanding developed in this program will provide a detailed foundation for the rational design of materials and processing strategies for the fabrication of sub 100 nm structures. The unique measurement methods we apply include x-ray and neutron reflectivity (XR, NR), small angle neutron scattering (SANS), incoherent neutron scattering (INS), near-edge xray absorption fine structure (NEXAFS) spectroscopy, quartz crystal microbalance (QCM), nuclear magnetic resonance (NMR), atomic force microscopy (AFM), Brillouin light scattering (BLS), and combinatorial methods. Our efforts focus on the fundamentals of polymeric materials and processes that control the resolution of the photolithography process including: (1) the physical properties of and polymer chain conformation within sub 100 nm structures, (2) the spatial segregation and distribution of photoresist components, (3) the transport and kinetics of photoresist components, environmental contaminants, and the deprotection reaction interface over nanometer distances, (4) the material sources of line-edge roughness (LER), a measure of the ultimate resolution of the lithographic process, and (5) the polymer physics of the developer solution and the dissolution process. These data are needed to meet the future lithographic requirements of sub 100 nm imaging layers and critical dimensions.

Customer Needs

Photolithography remains the driving and enabling technology in the semiconductor industry to fabricate integrated circuits with ever decreasing feature sizes. Today, current fabrication facilities use chemically-amplified (CA) photoresists, complex and highly tuned formulations of a polymer film loaded with photoacid generators (PAGs) and other additives. Upon exposure of the photoresist film through a mask, the PAG creates acidic protons. A post-exposure bake is then applied and the acid protons diffuse and catalyze a deprotection reaction on the polymer that alters its solubility in an aqueous base developer solution. These reaction, diffusion, and development processes must be understood and controlled at the nanometer length scale to fabricate effectively integrated circuits. Chemically amplified resists are also deposited onto bottom anti-reflection coatings (BARCs). Interactions and component transport between the BARC and resist layer can lead to loss of profile control or pattern collapse. Detailed studies of these interaction and transport mechanisms are needed to design materials for the successful fabrication of sub 100 nm structures.

There are significant challenges in extending this technology to fabricate the smaller feature sizes (sub 100 nm) needed to continue performance increases in integrated circuits. First, new radiation sources with shorter wavelengths (193 nm, 157 nm, or EUV) require photoresist films nearing 100 nm thick to ensure optical transparency and uniform illumination. In these ultrathin films, confinement can induce deviations in several key materials parameters such as the macromolecular chain conformation, glass transition temperature, viscosity, or transport properties. Furthermore, the required resolution for a sub 100 nm feature will be on the order of 2 nm, approaching the macromolecular dimensions of the photoresist polymers. It is not yet clear how deviations due to confinement will affect the ultimate resolution in these ultra-thin photoresist films. Additionally, the material sources of feature resolution (line-edge and sidewall roughness) and profile control need to be identified and understood to ensure the success of needed patterning technologies.

The requirements for advanced photoresists are discussed in the 2001 International Technology Roadmaps for Semiconductors on page 243, Lithography, "Photoresists need to be developed that provide good pattern fidelity, good linewidth control, and low defects at several new wavelengths. Each of the 130 nm, 90 nm and 65 nm nodes could involve the introduction of a

new wavelength or non-optical lithography, so each node will require the development of an entirely new resist platform. As feature sizes get smaller, defects and polymers will have comparable dimensions with implications for filtering of resists."

Technical Strategy

1. In this project, we use model photoresist materials to validate the new measurement methods. Model 248 nm photoresist materials have been used initially to address several important fundamental questions including the thermal properties of ultrathin films as a function of film thickness and substrate type, the conformation of polymer chains confined in ultrathin films, the surface concentration of PAGs, the diffusion and the reaction kinetics of the deprotection reaction, and the physics of the development process. We also are adapting the application of combinatorial methods as a tool to determine rapidly important lithographic parameters and to identify material factors impacting feature resolution. These results provide a strong basis for understanding the material property changes that may affect the development of lithography for sub 100 nm structures using thin photoresist imaging layers. The interaction between model photoresists and BARC materials also requires detailed experimental investigation to optimize the materials factors impacting lithographic performance.

DELIVERABLES: Correlate x-ray reflectivity, bilayer deprotection reaction rate, and incoherent elastic neutron scattering $<u^2>$ data corresponding to changes in small molecule diffusion in thin films. 2Q 2003

DELIVERABLES: Develop depth profiling NEXAFS method to quantify spatial extent of changes in surface versus bulk chemistry in photoresist films. 2Q 2002

DELIVERABLES: Measure NEXAFS spectra and developer solution conformation of model 157 nm photoresist polymers. 3Q 2002

DELIVERABLES: Use SANS to measure the deprotection path of dispersed PAG molecules in d-PBOCSt resist films. 2Q 2003

DELIVERABLES: Quantify solvent quality of photoresist polymers in developer solutions as a function of added salt and temperature. 4Q 2003

DELIVERABLES: Identify material transport and chemical interactions leading to the formation of residual layers at the BARC-resist interface as a function of processing conditions. 4Q 2003

DELIVERABLES: Obtain crucial insight by using different polymers and polymer/substrate combinations, we will obtain crucial insight into the dynamical effects of polymer thin film confinement by studying different polymers and polymer/substrate combinations with INS and QCM. 4Q 2003

Accomplishments

■ Incoherent neutron scattering was used to measure the atomic-level dynamics of model photoresist polymer thin films for the first time. The local, atomic-level, dynamics of the photoresist polymer directly affect transport processes essential to modern photoresists, such as the diffusion of photogenerated acids and other small molecules within the polymer matrix. To date, changes in the local dynamics of polymer thin films have been inferred from changes in macroscopic quantities such as the apparent glass transition temperature, Tg, as a function of film thickness and substrate interaction energies.

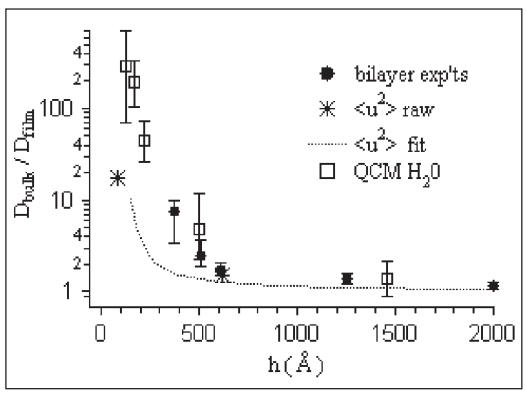

Figure 1. The ratio of the bulk to film diffusion coefficients are displayed as a function of film thickness for the bilayer, neutron scattering, and QCM experiments. All three techniques indicate similar reductions of mobility at similar length scales.

Direct measurements of the segmental motions of polymer chains confined to ultrathin films provide a molecular picture of observed changes in these macroscopic quantities and insight into differences in photoresist transport processes in ultrathin films. QCM measurements of moisture diffusion rates in ultrathin resist films are dramatically reduced relative to those in thicker films. Further, in Fig. 1, three different measurements show similar reductions of mobility at similar film thickness length scales.

■ After photogeneration, acid molecules catalyze multiple reactions within the photoresist matrix. A central issue in photoresist design is quantifying both the number of reactions each acid can catalyze and the size and shape of the deprotected volume created upon reaction. The size and shape of the volume have been identified in recent computer simulations as a primary source line edge roughness (LER) formation.

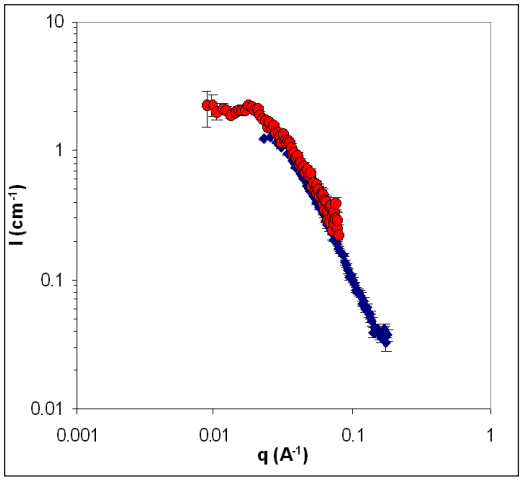

Figure 2. SANS data from the deprotection of dispersed PAGs after exposure and bake. The data are consistent with a random walk deprotection reaction path.

Using SANS and specially deuterated polymers, we successfully measured characteristics of the deprotection volume due to acid diffusion paths in a model photoresist. The general technique is readily extendible to photoresists with the appropriate deuterium labeling, independent of the PAG species. The deprotection volume from dispersed acid molecules features a diffuse interface, a result inconsistent with a well-defined two-phase structure. The data in Fig. 2 are consistent with models for random walk statistics. We determined that the deprotection volume has a radius of approximately 8.5 nm after 120 s of post exposure bake at 90 ºC. Infrared spectroscopy was used to determine the level of deprotection at 32 % with a 0.7 % mass fraction of PFOS. The result is consistent with a large diffusion path, and hence a large number of catalyzed reactions per acid molecule.

■ The deprotection reaction front profile was measured with nanometer resolution using both xray and neutron reflectometry on a bilayer structure prepared with a specially labeled (deuterated) protected polymer. The upper layer of the structure is loaded with the PAG. Upon exposure and baking, the acid diffuses into the lower layer and catalyzes the deprotection reaction. The protecting group is deuterated and is volatile upon reaction. Thus, contrast to neutrons results from the reaction allowing for observation of the reaction front. By comparing the reaction front to the developed film profile, we obtain important insight into both the spatial extent of the reaction and the development process itself. These data are the first available with this spatial resolution and are critically needed for the development of process control over nanometer length scales. We find that the reaction front broadens with time while the surface roughness of the developed structure remains relatively sharp. Additionally, we find that a broader reaction front results in changes in the compositional profile upon development in an aqueous base.

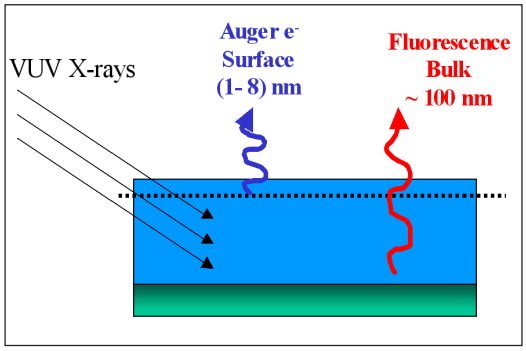

Figure 3. Schematic diagram of the NEXAFS measurement geometry. Spectra are obtained from the film surface and bulk simultaneously.

■ NEXAFS measurements were used to measure the surface concentration of photoresist and BARC components and the surface reaction kinetics in model photoresist polymers as a function of common processing conditions. A significant advantage of the NEXAFS measurement is the capability of separating interfacial and bulk signals within the same sample and experiment in Fig. 3. NEXAFS measurements of interfacial chemistry are possible because of the limited escape depth of produced secondary electrons. By separately observing the electron and fluorescence yield, the chemistry at the surface (2 nm) and bulk (200 nm) may be determined. Different chemistries may be observed by examining the near-edge xray spectra of light elements such as carbon, oxygen, fluorine, and nitrogen. In this way, changes in the surface chemistry relative to the bulk film can be investigated as a function of lithographic

processing steps such as exposure and heating. We have found that fluorinated PAG molecules preferentially segregate to the film surface. The relative amount of segregation is dependent upon the specific polymer. In addition, NEXAFS analysis of residual layers arising from BARC-resist component transport and interactions enable detailed analysis of potential mechanisms leading to loss of profile control.

■ The development step selectively removes UV exposed photoresist material and represents the last step in the fabrication of nanostructures prior to semiconductor etch and deposition. With dimensions shrinking to sub 100 nm, control of line-edge roughness becomes more important and contributions to roughness from the development step requires an improved framework. In the development step, the aqueous base TMAH developer shifts the local chemical equilibrium from an un-ionized form to the ionized form, for instance in the 248 nm material poly(hydroxystyrene). SANS data, in Fig. 4, demonstrate the origin of the miscibility in aqueous base is due to the ionization of the photoresist leading to polyelectrolyte behavior. The identification of the presence of polyelectrolyte behavior during the development process provides an improved framework to understand the roles of added electrolytes, such as low molecular weight organic (tetramethyl ammonium chloride) and inorganic salts (NaCl, KCl). The addition of salts controls the observed line-edge roughness, by reducing the influence of polyelectrolyte behavior. Current experiments using different developing and rinsing protocols demonstrate that the pH of the rinse step is very important. This suggests the surface layer may contain polyelectrolyte effects even after development as demonstrated by an increase in surface RMS roughness for the development of bilayer samples with 0.26N TMAH followed by water rinse and 0.01 M HCl rinse.

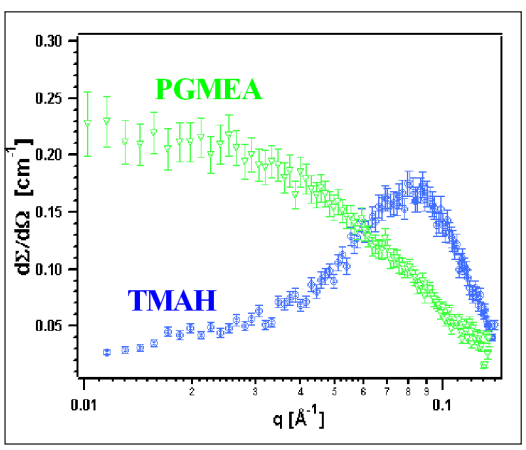

Figure 4. SANS data from a model photoresist polymer in organic solvent (PGMEA) and the developer base solution (TMAH). The scattering peak in TMAH solution is representative of the polyelectrolyte behavior.

Collaborations

Polymers Division, NIST – Ronald L. Jones, Vivek M. Prabhu, Chia-Ying Wang, Erin L. Jablonski, Bryan D. Vogt, Tengjiao Hu, Natsuko Noda, Michael X. Wang, Francis W. Starr, Patricia M. McGuiggan, David Vanderhart, Michael Fasolka, Alamgir Karim.

Ceramics Division, NIST – Daniel A. Fischer, Sharadha Sambasivan.

Center for Neutron Research, NIST – Charles J. Glinka, Sushil K. Satija, Daniel Neumann, Robert M. Dimeo.

IBM T. J. Watson Research Center – Dario L. Goldfarb, Arpan Mahorowala, Karen Temple, Marie Angelopoulos.

IBM Almaden Research Center – Hiroshi Ito.

DARPA – Advanced Lithography Program, Contract N66001-00-C-8083.

Brewer Science, Inc. – Chelladurai Devadoss, Yubao Wang, Rama Puligadda, James Claypool.

University of Texas at Austin – Brian C. Trinque, Sean D. Burns, C. Grant Willson.

University of Akron – Alexsei Sokolov, Ryan Hartschuh, Yifu Ding, Joon Roh, Alexander Kisliuk.

Sandia National Laboratories – Joseph L. Lenhart.

Recent Publications

C. L. Soles, J. F. Douglas, E. K. Lin, J. L. Lenhart, R. L. Jones, W. L. Wu, and D. L. Goldfarb, "Incoherent Neutron Scattering and the Dynamics of Thin Film Photoresist Polymers," J. Appl. Phys. **93**, 1978 (2003).

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Critical Dimension and Overlay Metrology Program

The principal productivity driver for the semiconductor manufacturing industry has been the ability to shrink linear dimensions. A key element of lithography is the ability to create reproducible undistorted images, both for masks and the images projected by these masks onto semiconductor structures. Lithography as a whole, fabricating the masks, printing and developing the images, and measuring the results, currently constitutes ≈35 % of wafer processing costs. The overall task of the Critical Dimension and Overlay Program is to assist the industry in providing the necessary metrology support for current and future generations of lithography technology. These goals include advances in modeling, the provision of next generation critical dimension and overlay artifacts, and comparisons of different critical dimension and overlay measurement techniques.

Currently, resolution improvements have outpaced overlay and critical dimension measurement improvements. To maintain cost effectiveness significant advances must be made.

Atom-Based Dimensional Metrology

Technical Contact:
R. Silver

Goals

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing the methods, tools, and artifacts needed to apply leading edge, high-resolution atom-based dimensional measurement methods to meet the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on wafers with nanometer accuracy. We are developing three-dimensional structures of controlled geometry whose dimensions can be measured and traced directly to the intrinsic crystal lattice. These samples are intended to be dimensionally stable to allow transfer to other measurement tools which can measure the artifacts with dimensions known on the nanometer scale.

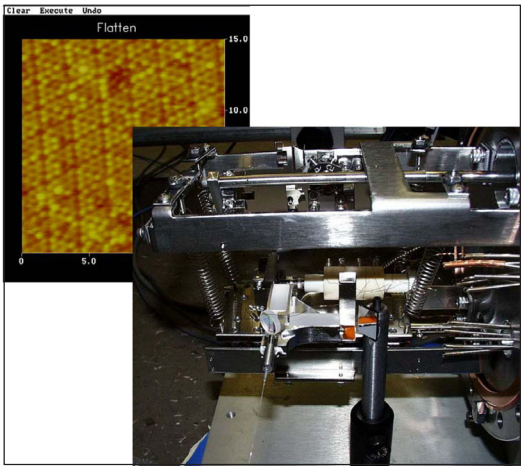

Figure 1. The atomic resolution image above was measured with a 20 picometer resolution interferometer system mounted on the UHV STM.

Customer Needs

NIST responds to U.S. industry needs for developing length intensive measurement capabilities and calibration standards in the nanometer scale regime. The new class of scanned probes have unparalleled resolution and offer the most promise for meeting these future needs of the microelectronics industry. One important application of the high-resolution SPM methods is in the development of linewidth standards whose dimensions can be measured and traced through the crystal lattice from which they are made. In addition, these high-resolution tools can be coupled directly to a new NIST-designed picometer resolution interferometer.

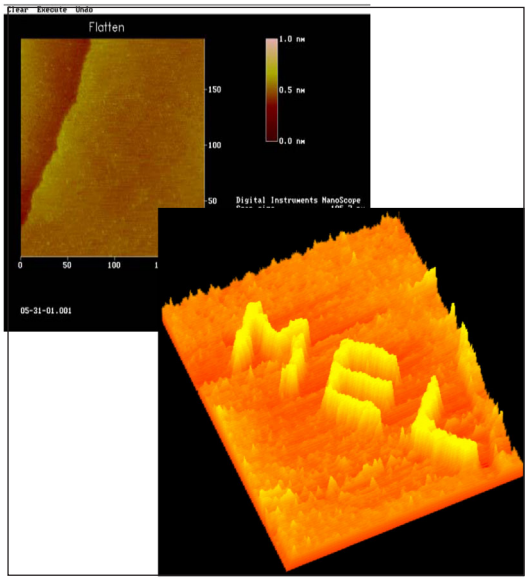

Figure 2. This recent result utilizes the atomically flat surfaces as a substrate for nanomanufacturing. The feature's CDs are 10 nm and the entire lateral field of view is 250 nm. The background shows an atomically flat substrate.

The work funded in this project is for the development of atom-based linewidth standards to assist in the calibration of linewidth metrology tools and the development of unique interferometry capabilities which can be used in conjunction with accurately measured tips to measure feature critical dimensions. This effort is intended to enable the accurate counting of atom spacings across a feature in a controlled environment and to subsequently transfer that artifact to other measuring instruments as a structure with atomically known dimensions. As critical dimensions continue to shrink, the detailed atomic structure, such as edge roughness or sidewall undercut, of the features to be measured represents a larger portion of the measurement uncertainty. Furthermore, particularly with SEMs, the instrument response and the uncertainty in the edge location within an intensity pattern becomes a significant issue due to the increased sensitivity to detailed elements of the edge detection model. The complexity of these models and large computer resources required for each individual computation make the idea of having samples of known geometry and width, essential.

This project is intended to develop samples of known geometry and atomic surface structure which will yield measurements resulting in a specific number of atoms across the line feature or between features. These samples will be measured in the UHV environment and then stabilized and subsequently transferred to other instruments (see Fig. 1).

There are three primary applications of this type of artifact after it has been atomically counted. The first method is the direct calibration in an SEM for a product wafer whose geometry and material is near to the structure of the atomically counted sample. The second method utilizes an AFM to calibrate the SEMs with the AFM acting as an SEM matching tool. In this method, the AFM is calibrated with an atomically measured sample of the same geometry as the product wafer to be measured by the SEMs. This sample only needs to have similar geometry to the product wafer, but does require similarity in materials due to the insensitivity of an AFM to materials, variations. AFM, that has been calibrated for a particular geometry by an atomic artifact, can then transfer that calibration to a product wafer of similar geometry and any material such as photoresist, resulting in a calibrated product wafer which can then be transferred to calibrate an SEM.

The third method uses the number of atoms between features to determine the feature spacing. This method can be used to make magnification and pitch calibration standards based on the intrinsic crystal lattice.

These methods of atom counting and high-resolution interferometry, as outlined in this project description, are non-destructive and are intended to yield samples which can be measured by various instruments such as an SEM and subsequently re-measured atomically. This is a unique and important element of this work since there are no other known methods that allow this kind of atomic dimensional measurement without being destructive. In addition, this new method opens up the possibilities of basing the measurement metric on the intrinsic crystal lattice.

Technical Strategy

The technical work is focused into four thrust areas.

1. The development of methods to prepare photolithographically patterned three-dimensional structures in semiconductor materials. These structures must be prepared in such materials as to allow the atomic surface reconstruction of those features such that the atomic order is commensurate with the underlying crystal lattice. This involves either using conventional photolithography methods for sample production or using the STM itself to fabricate very small nanometer scale features as shown in Fig. 2.

DELIVERABLES: Write features in silicon with critical dimensions as small as 10 nm. Develop the process so it can be implemented in the M-cubed STM metrology system. Develop the process to write features for optical methods. 2Q 2003

DELIVERABLES: Work with SEMATECH and EEEL for the development of improved methods for etching nanostructures written in silicon. Use RIE etching techniques. These structures must be prepared in such materials as to allow the measurements of those features in silicon. 4Q 2003

2. The development of techniques for the preparation of SPM tips with reproducible geometries and the direct characterization of the SPM tip geometry and dimensions on the atomic scale. These well characterized tip probes can then be used to measure the samples with photolithographically defined and canonically ordered surfaces on the sub-nanometer length scale. We are developing the SPM tip etching, field evaporation, and cleaning procedures which reliably yield stable W tips and produce atomic resolution on Si (7x7) surfaces. These tips are also useful in a collaboration with the SEM project for development as nanotips as SEM field emitters. Our tip preparation methods leave us uniquely qualified in this arena.

DELIVERABLES: Work with the SEM metrology project for the testing of nanotips as SEM field emitters. Assist in automation and tip modeling for field emitters. 1Q 2003

3. Focus on the development of artifacts that can be atom counted and then measured in a number of different metrology tools such as SEM and AFM. The integrity of the line geometry, such as side wall angle, is crucial to having useful artifacts for linewidth specimens. These edge geometry requirements are not as stringent for the magnification standards since feature symmetry is the most crucial element in these measurements. The work on linewidth artifacts, therefore, is focused on reducing the process temperatures required for atomic reconstructions. We have made wet chemical processing fully operational and are currently working on preparing atomically ordered Si surfaces at significantly reduced temperatures. For

sample preparation, we are utilizing the existing in-situ processing apparatus and techniques from the UHV STM and concentrating on the reproducible production of atomically ordered Si surfaces and Si (111) step and terrace structures.

DELIVERABLES: Develop metrology methods for the new set of wafers specifically for atom-based dimensional metrology. This new wafer set was written by ebeam on silicon (111) wafers which are aligned crystallographically. 3Q 2003

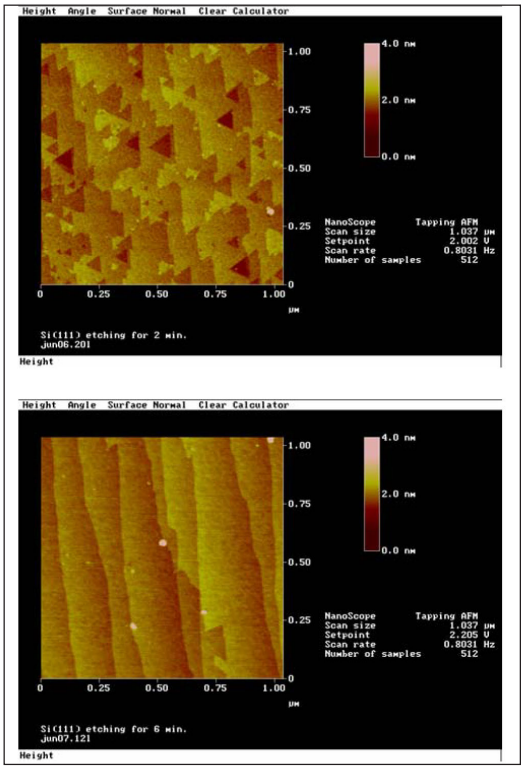

Figure 3. These are atomically flat, chemically prepared surfaces for use in atom-counting and nanomanufacturing.

4. The development of a new interferometer system intended to measure dimensions in the 20 picometer range with high accuracy. The system should also be capable of use on the STM so atomic scale measurements can be made with new levels of accuracy. In addition we are exploring new applications of field ion microscope (FIM) calibrated tips in conjunction with the interferometry to measure CDs of leading edge, small semiconductor features.

The long term technical objective is the development of *in situ* stabilized, atomically ordered surfaces which can be transferred to other measurement instruments such as scanning electron microscopes, AFMs, or optical metrology tools. These nanometer scale standard artifacts with atomically ordered surfaces will then act as linewidth or magnification calibration samples. These samples will have been measured either by direct atom counting or high-resolution interferometry and atomically measured tips.

Accomplishments

- We have obtained atomically flat surfaces and are now trying to obtain atomic order, to routinely obtain the low temperature wet chemical based methods. Although we had a similar effort with GaAs, which was successful, we are currently focused on silicon substrates

- The ability to prepare atomically sharp tips in W (111) has been demonstrated. The details of this methodology and the new models we have developed for analyzing sharpness have been prepared as a journal article.

- We have prepared two publications which give new insight into the etching process for fabricating atomically flat silicon surfaces. The results, seen in figure 3, yield a new, more comprehensive understanding of the physical processes involved in making atomically flat surfaces in silicon as required for much of the work in this project.

- The first UHV transfer was been demonstrated between the NIST MBE system and the PED UHV STM. The sample was maintained in a UHV environment during the entire event. Further UHV sample manipulation and preparation for transfer to other systems and long term storage will be investigated in the future as required.

- We have developed techniques for the preparation of SPM tips with reproducible geometries and the direct characterization of the SPM tip geometry and dimensions on the atomic scale. We are now applying these ideas to FIM tips used in SEM metrology.

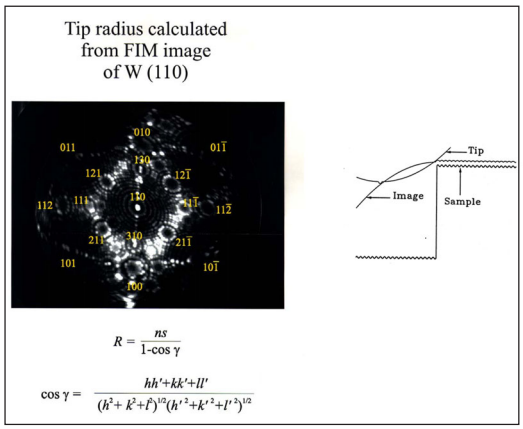

Figure 4. A FIM image showing the atomic order in a W tip is shown. The schematic on the right shows the method of atom counting or high resolution tip-based interferometry.

■ We have attempted our first direct measure of the surface atom spacings based on a traceable interferometer measurement. We have fitted our UHV STM with a high accuracy sub-angstrom resolution interferometer. We have closed the loop and made our first atomic resolution measurements with full interferometer length basis. The successful completion of this aspect has enabled direct distance determination with simple atomic counting.

DELIVERABLES: Publish the results for the first demonstration of direct interferometer measurements of surface atom spacings with a complete unbroken uncertainty. Present these results at the ASPE conference and SPIE to make the new interferometry methods available to the industry. 3Q 2003

■ Wafers from the NIST designed metrology reticle set have been evaluated for use in atom-based dimensional metrology. The initial evaluation is very promising and all four wafer flows yielded good product wafers. These wafers contain the prototype test structures, including a comprehensive set of critical dimension and line space arrays for general metrology purposes. The double-etched silicon multi-level features are intended to provide long term stable artifacts for calibration with the line arrays being test patterns for atom-based dimensional metrology work.

■ We have produced atomically ordered surfaces of GaAs at far reduced temperatures and have worked with patterned GaAs linewidth samples. The GaAs linewidth features have been fabricated and we have successfully prepared As capped samples without damaging the line geometry or integrity in any measurable way. These samples have been processed using the complete atomic surface preparation method, measured in UHV and then allowed to oxidize to create a stable surface for measurement in other tools.

Collaborations:

ISMT, IBM, University of Maryland, Dept. of Physics, University of Purdue, Dept. of Physics.

Recent Publications

"Wet Chemistry of Si samples," J. Fu, H. Zhou, and R. M. Silver, Applied Physics Letters, in press April 2003.

"A Macro-micro Motion System for a Scanning Tunneling Microscope," J. Gilsinn, B. Damazo, R. Silver, and H. Zhou, World Automation Congress, Proc. From Intl. Symp. on Robotics and Applications (2002).

"Nanomanufacturing of Atom Based Standards," NAMT final report. NISTIR 6850 (2002).

"Calibration of a Prototype Silicon Pitch Artifact Fabricated by Scanning Probe Oxidation and Anisotropic Etching," J. Dagata, F. Chien, W. Hsieh, S. Gwo, J. Jun and R. Silver. (WERB Complete FY02)

"A Generic Shape Model for STM Tip Geometry," P. V. M. Rao, C. Jensen, and R. M. Silver, submitted to Ultramicroscopy, (2002).

"A New Tunable Diode Laser Method for a Sub-nanometer Resolution Interferometry," R. M. Silver, S. Gonda, C. Jensen, and L. HowardAccepted in Optical Eng. 2003.

"A new design and uncertainty consideration of a metrology UHV-STM for direct measurements of atom spacings," S. Gonda, H. Zhou, J. Fu and R. M. Silver SPIE Nanotechnology workshop proceedings, NIST 2001.

"Processing atomically flat Si surfaces," H. Zhou, J. Fu, S. Gonda and R. M. Silver, SPIE Nanotechnology workshop proceedings, NIST 2001.

Scanning Electron Microscope-Based Dimensional Metrology

Technical Contacts:
A. E. Vladár
M. T. Postek

"Scanning Electron Microscopy (SEM) – continues to provide at-line and inline imaging … and CD measurements. Improvements are needed … at or beyond the 90 nm generation… Determination of the real 3D shape … will require continuing advances in existing microscopy…"

International Technology Roadmap for Semiconductors, 2001

Goals

- Provide the microelectronics industry with highly accurate SEM measurement and modeling methods for shape-sensitive measurements and relevant calibration standards with nanometer-level resolution.
- Carry out SEM metrology instrumentation development, including improvements in electron gun, detection, sample stage and vacuum system.
- Conduct research and development of new metrology techniques using digital imaging and networked measurement tools solutions to key metrology issues confronting the semiconductor lithography industry.

Customer Needs

The scanning electron microscope is used extensively in many types of industry, including the more than $200 billion semiconductor industry in the manufacture and quality control of semiconductor devices. The International Technology Roadmap for Semiconductors targets SEMs as the metrology tool of choice for use in semiconductor production through at least the year 2005. The industry needs SEM standard artifacts, specifically those related to instrument magnification calibration, performance and the measurement of linewidth. This entails a multidimensional program including: artifact fabrication, understanding the function and signal generation in the SEM, electron beam interaction modeling, developing NIST metrology instruments for the certification of standards, and developing the necessary artifacts and calibration procedures. The manufacturing of present-day integrated circuits requires that certain measurements be made of structures with dimensions of 100 nm or less with a high degree of precision. The accuracy of these measurements is also important, but more so in the development and pilot lines. The measurements of minimum feature sizes known as critical dimensions (CD) are made to ensure proper device operation. The U.S. industry needs high-precision, accurate, shape-sensitive dimension measurement methods and relevant calibration standards. The SEM Metrology Project supports all aspects of this need since scanning electron microscopy is the major microscopic technique used for this sub-micrometer metrology.

Technical Strategy

The Scanning Electron Microscope Metrology Project is a multidimensional project. It is being executed through several thrusts fully supported by the semiconductor industry.

1. SEM Performance Measurement Artifact:

This effort includes the development of the Reference Material 8091 and evaluation procedures suitable for correctly measuring image sharpness of scanning electron microscopes, especially of those that are used in the semiconductor industry. The performance characteristics of the SEM are particularly important to precise and accurate measurements on the semiconductor processing line. NIST has demonstrated that a critical dimension measured in a scanning electron microscope functioning poorly can be 5 nm or more larger than in the same instrument functioning optimally. For reliable image sharpness measurements a suitable sample with small features is needed. NIST is continuously working on further development of better image sharpness metrology methods; this includes cooperation with vendors and users. Currently a thorough work is underway to assess fundamental imaging properties of CD and other SEMs.

DELIVERABLES: New results to be introduced and presented at technical meetings as they are worked out.

2. SEM Linewidth Measurement Artifacts:

Artifacts that are characterized and calibrated to the required small levels of uncertainty were and are in the focal point of the IC industry's dimensional metrology needs. Therefore, at NIST, it has been a longer-term goal to develop and deliver appropriate samples. For a long time the possibilities were limited by the lack of various technologies available, especially the lack of accurate modeling methods. NIST, through several years of systematic efforts, developed Monte Carlo simulation-based modeling methods that can deliver excellent results. These new

methods can deduce the shape of integrated circuit structures from top-down view images through modeling and library-based measurement techniques with few nm accuracy. NIST in several publications demonstrated the possibilities and described power of this measuring approach. Based on the newest results, now it is becoming possible to start to develop the long-awaited relevant line width standard for the semiconductor industry. Reference Material 8120 line width samples will be a relevant sample on a 200 mm and 300 mm Si wafer with polySi features with sizes from 3 mm to down to 70 nm. Standard Reference Material 2120 is going to be the calibrated, traceable version for line width measurements. This work is being carried out in cooperation with ISMT.

DELIVERABLES: Assessment of the feasibility of ISMT polySilicon samples to use as SRM 2120 samples. Incorporation of a modified version of the SRM 2120 structure into ISMT's new "OMAG" overlay metrology masks set. 4Q 2003

Accomplishments

- **SEM Performance Measurements** – After comprehensive studies and experiments a plasma-etching Si called "grass" was chosen for Reference Material 8091. This sample has 5 nm to 25 nm size structures as is illustrated in Fig. 1. Fifteen pieces of RM 8091 were delivered to International SEMATECH (ISMT) for the member companies, and 75 additional samples have been delivered to the Office of Standard Reference Materials, NIST. A sharpness standard and evaluation procedure have been developed to monitor (or compare) SEM image quality. A NIST kurtosis method, Spectel Company's user-friendly analysis system called SEM Monitor, and University of Tennessee's SMART algorithm can be used with RM 8091. An effort is underway to produce more of these samples and measurements methods that give not just repeatable, but accurate results. These samples are now available to the public as 2 mm by 2 mm chips and can be mounted onto 150 mm and 200 mm drop-in wafers, which are also available form NIST.

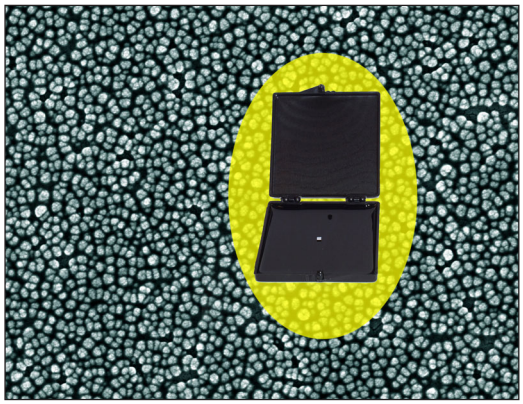

Figure 1. The RM 8091 SEM Image Sharpness Reference Material (100 000 x magnification).

- **SEM Linewidth Measurement Artifacts** – The development of accurate modeling methods in progress at NIST have shown excellent results on polySi samples. From a top-down view, using our high-accuracy modeling and fitting methods a cross section of the lines can be determined with few nm uncertainties and discrepancies. The match is so good that this method may be capable of eliminating the costly and destructive cross sectional SEM measurements. The candidate sample for linewidth artifact must be relevant to state-of-the-art IC technologies, should have chips on 200 mm and later 300 mm wafers with all process variation and include a meaningful focus-exposure matrix (FEM). The design and the fabrication of ISMT/NIST mask have been successfully completed and it is now being tried on a new high resolution 193 nm lithography tool. The lines are now well-formed, the resolvable problem on hand is edge roughness. Experiments with polySi deposition and etch are underway. The first wafers will come to NIST just before the end of summer. These wafers will go through a qualification process. Full wafers will get scatterometry and CD-SEM measurements at ISMT, and cross sectional measurements will be made at NIST. All these measurements will yield an excellent database for a decision on how to

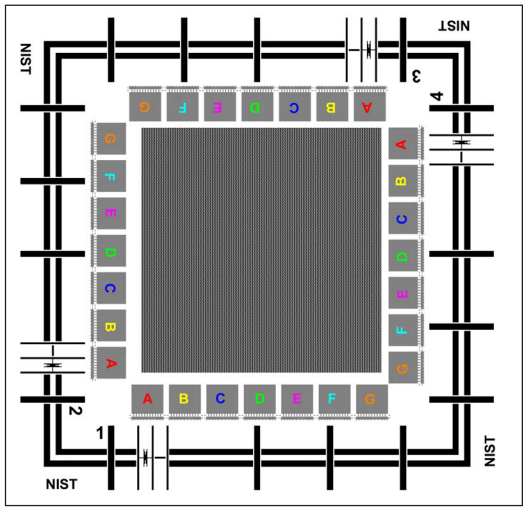

Figure 2. The design of the SRM 2120 Linewidth calibration Standard Reference Material.

proceed with this wafer type linewidth reference sample. It is conceivable that by the end of the year 2003 the Reference Material 8120 line width samples, as seen in Fig. 2., will be available. This work is being carried out in close cooperation with ISMT.

■ **Development of Ultra-High Resolution Nano-Tip Electron Gun for CD-SEMs** – The source diameter and the brightness of the electron beam are two of the major factors limiting the performance of CD-SEMs in the semiconductor production environment. Thus, alternative solutions to improve performance are being sought as the metrology for sub 100 nm lithography is being pushed to its limit. One possible alternative approach is the application of nano-tips as an electron source replacement. Nano-tips, by comparison to both conventional cold field (CFE) and to Schottky field emitters, offer a substantial increase in brightness (10 x to 100 x) and a large reduction (5 x to 10 x) in source size. Therefore, in an optimized electron optical column, substitution of a CFE or Schottky source by a nano-tip could be expected to produce:

– Higher beam currents into a spot of given size.

– Better signal-to-noise ratio and resolution.

– Faster scan rate and better charge control.

This work has progressed through:

– New tip preparation and evaluation procedures;

– The Hitachi S-6000 CD-SEM was prepared for the installation of the nano-tips. This was facilitated through the help of Hitachi Scientific Instruments. The SEM currently works to the original specifications. One sharp tip was successfully tried with good results.

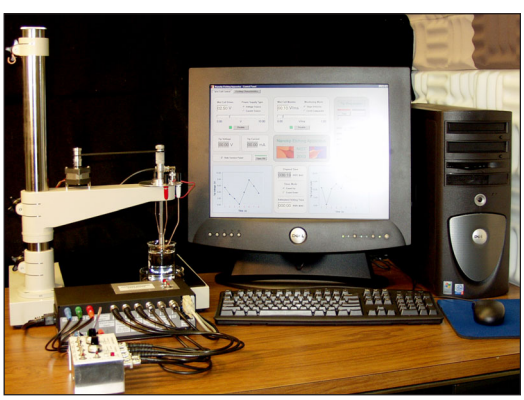

Figure 3. Photograph of the NIST nano-tip etcher tool.

– Fabrication of a nano-tip assembly, which matches in geometry the S-6000 CD-SEM field emitter tip. This new version works with rod-type tips and greatly improves the speed of tip exchanges.

The nano-tip fabrication technology (i.e. sharpening process) is now working reliably, and the main issue of how to properly mount the prepared nano-tip in place of the original hairpin shaped tungsten tip holder has been successfully solved. With the NIST-developed new fully computer-controlled etching apparatus, Fig. 3, new tips are being made and tried in the S-6000 CD-SEM, as can be seen in Fig. 4.

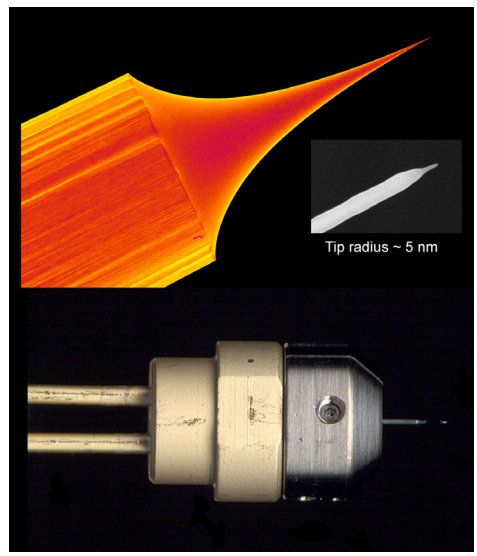

Figure 4. Photograph of the NIST nano-tip.

The results so far are promising; the tip life-time is several months in light use and the resolution is better than as of the regular tip. Further experiments to fine-tune the electron gun assembly and explore the full applicability of nano-tips are underway.

Collaborations

International SEMATECH, Metrology Council.

Naval Research Laboratory; E-beam Lithography.

International Technology Roadmap for Semiconductors; Microscopy and Metrology Sections.

Recent Publications

"A New Way of Handling Dimensional Measurement Results for Integrated Circuit Technology," A. E. Vladár, J. S. Villarrubia and M. T. Postek. Proc. SPIE 2003, in press.

"CD-SEM Measurement of Line Edge Roughness Test Patterns for 193 nm Lithography," B. D. Bunday and M. Bishop, J. S. Villarrubia and A. E. Vladár. Proc. SPIE 2003, in press.

"Applications of image diagnostics to metrology quality assurance and process control," A. Starikov; J. A. Allgair; V. V. Boksha; B. D. Bunday, A. C. Diebold; D. C. Cole; A. W. Gurnell; D. C. Joy; J. M. McIntosh; J. C. Pellegrini; R. D. Larrabee, J. E. Potzick; A. E. Vladár; N. P. Smith; N. T. Sullivan. Proc. SPIE 2003, in press.

"Scanning electron microscope analog of scatterometry," J. S. Villarrubia, A. E. Vladár, J. R. Lowney, and M. T. Postek, Proc. SPIE 4689, pp. 304-312 (2002).

"Test of CD-SEM Shape-Sensitive Linewidth Measurement," J. S. Villarrubia, A. E. Vladár, and M. T. Postek, final report to International SEMATECH, January 2003, available to member companies at SEMATECH web site.

"Exploring and Extending the Limits of SEMs' Resolution," A. E. Vladár, J. S. Villarrubia, and M. T. Postek, final report to International SEMATECH, November 2002, available to member companies at SEMATECH web site.

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Optical-Based Dimensional Metrology

Technical Contact:
R. Silver
J. Potzick
T. Doiron

Goals

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply optical techniques to the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on photomasks and wafers, where appropriate, at the customer's facility. The industry focus areas of this project are primarily the optical based methods used in overlay metrology, photomask critical dimension metrology, and high-accuracy two-dimensional placement metrology.

Customer Needs

Tighter tolerances on CD measurements in photomask and wafer production place increasing demands on photomask linewidth accuracy and on overlay tolerances. NIST has a comprehensive program to both support and advance the optical techniques needed to make these overlay and photomask critical dimension measurements.

In addition, improved two-dimensional measurement techniques and standards are needed for measuring and controlling overlay capabilities of steppers and mask-making tools under development. Overlay is listed in Table 96 of the 2001 SIA ITRS as a difficult challenge for both >65 nm and <65 nm processes. Overlay improvements have not kept pace with resolution improvements and will be inadequate for ground rules less than 67 nm. In fact, Table 98b shows that no known solutions for overlay output metrology exist beyond the 67 nm node. As shown in Table 99a, the problems are more acute for CD mask metrology where the industry is currently encountering metrology problems without known manufacturing solutions.

Technical Strategy

There are three main strategic technical components of this project.

1. The first strategy consists of the development of NIST's overlay metrology tool, continuous development of the tool, measurement methods to obtain uncertainties comparable to or better than the best industry overlay tools, and standards to support and calibrate these tools. The technical strategy for overlay metrology is divided into two segments: a) instrumentation development and overlay metrology methodology and b) design and calibration of standard artifacts. Pattern placement and overlay of the various lithographic levels is monitored with a series of targets, each in a different plane. The overlay offset is then obtained by optical measurements with a determination of the relative target centerlines. Any misalignment in the overlay metrology system will translate into an artificial overlay offset, referred to as *tool induced shift* (TIS). Additionally, there are residual errors caused by asymmetries in the target edges or covering layers (resist) known as *wafer induced shift* (WIS). A set of standard artifacts and procedures, under development at NIST, is designed to assist in aligning overlay measurement systems and eliminating TIS. After alignment, the tool must then be calibrated with standard artifacts to yield accurate overlay offsets. The measurement system used in this component is an optical reflection mode instrument, operational in either a bright field or confocal mode, with interferometry on three orthogonal axes also capable of monitoring the stage tilt. Additional hardware capabilities include the options to scan the sample while acquiring data with an on-axis photometer or high resolution image capture with a full field CCD data acquisition system. This latter mode has enabled a detailed study of CCD array performance and characterization. In this work, several CCD acquisition systems are being evaluated and improved edge detection and CCD array calibration procedures are being developed. These same methods for two-dimensional CCD array analysis are now being applied to optics analysis. Additional investigation of CCD measurement problems are focused on the detailed response of typical CCD camera light sensors.

WIS-free standard overlay artifacts have been fabricated in 200 mm wafers. These overlay artifacts are for the calibration of industrial optical overlay tools. The artifacts are being fabricated in single crystal silicon and will provide an array of etched silicon three-dimensional targets with additional targets fabricated using industry standard process levels. These wafers additionally have an extensive set of characterization targets and structures developed in close collaboration with International SEMATECH (ISMT) and several leading semiconductor manufacturers.

DELIVERABLES: Update the formal qualification numbers on the overlay microscope, optics, and the *x-y* metrology stage. This is largely completed and the final uncertainties need to be tabulated. The current, most difficult challenge is the qualification for calibration of complex overlay target process levels such as contact-to-poly. 2Q 2002

DELIVERABLES: Use the new metrology reticles from the ISMT collaboration to make leading edge overlay calibration targets/wafers. Work with industry partners to determine designs and which levels are most appropriate for the silicon fabrication phase. Calibrate these overlay standards (both alignment and calibration) for SRM certification. 3Q 2003

2. The ultraviolet transmission microscope, calibration of NIST Photomask Linewidth Standard SRM 2059, and the development of calibration methods to obtain photomask linewidth measurement uncertainties are adequate to meet industry needs.

The technical strategy for photomask linewidth standards is similarly divided into two segments: (1) instrumentation and model development and (2) design and calibration of standard artifacts. An ultraviolet transmission microscope (Fig. 1) has been constructed to replace the green-light linewidth calibration system. This new instrument uses a unique geometry (a Stewart platform) as the main rigid structure and shows considerable improvement in vibration characteristics over a conventional microscope. Higher image resolution, reduced transmission of UV light through the chrome, and reduced instrument vibration will offer improved linewidth measurement uncertainties.

NIST has supplied a substantial number of photomask linewidth standards worldwide over the past decade. Chrome-on-quartz photomasks with linewidth and pitch features in the range of 0.5 µm to 30 µm have been certified on a green light optical calibration system. Linewidth uncertainties have been reduced to 40 nm. The next generation in this line of standards is SRM 2059 (Fig. 2), printed on a standard size 6x6x0.25 inch substrate with calibrated line- and spacewidths ranging from nominally 0.25 µm to 32 µm and pitch patterns from 0.5 µm to 250 µm.

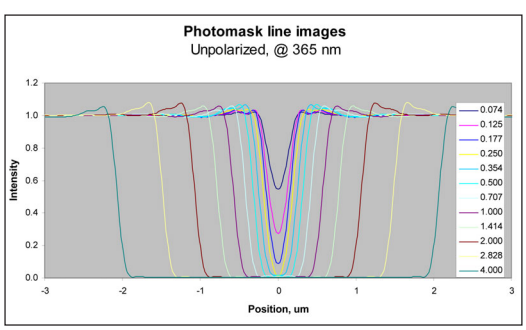

Figure 1. Modeling results for linewidth photomask samples showing CDs down to 0.25 micrometers.

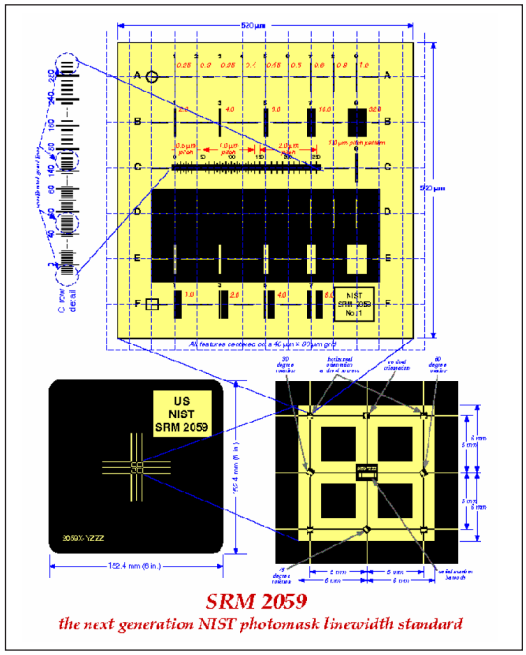

Figure 2. The new linewidth photomask standard.

In response to customers' needs for more accurate photomask feature size measurements, an industry group was formed for the improvement of mask metrology through process modeling. The features on even the highest quality masks exhibit roughness and runout at the chrome edges, compromising the definition of edge and linewidth. Modeling the effects of all of the relevant feature properties in both the mask metrology process and in wafer exposure and development processes, using existing and new software tools, can improve feature size accuracy by establishing the relationship between mask-feature metrology results and the corresponding wafer-feature sizes.

DELIVERABLES: Compare and test the accuracy of new scattering models for line width evaluation in transmission. 3Q 2003

DELIVERABLES: Work with SEMI and ISMT in the development of a new standards specifications document for overlay metrology. 4Q 2003

3. The third component is the development of two-dimensional grid calibration standards and associated measurement techniques, including

statistical analysis and CCD characterization as used by industry. These individual technical strategies for these components are described in more detail next.

We are approaching the problem of two-dimensional measurements from a couple of directions. The first, and most immediate, is to develop an artifact standard which can be used to bring all of the two-dimensional based inspection instruments to the same metric. This work has developed a standard grid which will be available as a NIST Standard Reference Material, # 5001, to standardize 2D measurements in the semiconductor industry. The effort has three main parts: development of an industry consensus standard grid, measurements by state-of-the-art machines in private industry, and verification of the measurements using NIST capabilities.

Grids for the SRM have been made and final measurements are in process. Each measurement of the grid will have data in each of at least two orientations. Rotating the grid 90° between measurements samples a number of the geometric errors of the machine. The remaining geometric sources of uncertainty are the scale and some components of the linearity of each machine axis travel.

Verification of the grid measurements is being done at NIST. The overall scale of the grid is checked with the NIST linescale interferometer, an instrument that is known to provide the most accurate 1D measurements available in the world. Two sources of uncertainty not captured by these measurements include components of the straightness and effects of the plate bending when fixtured. Work is now focused on methods to characterize both of these effects. These studies provide a complete error budget for SRMs.

To strengthen the foundation of NIST's claims for linewidth measurement traceability and to support the BIPM *Mutual Recognition Arrangement*, NIST has become the pilot laboratory for an international intercomparison of submicrometer linewidth measurements. National metrology institutes in nine countries around the world are participating.

DELIVERABLES: Calculate asymmetric overlay targets images upon successful comparison for modeling results of more standard double etched silicon structures. Publish and present these results at SPIE Microlithography. 2Q 2002

DELIVERABLES: Use fully automated focus and positioning control systems to improve system performance. Continue to develop comprehensive analysis capabilities for centerline and edge detection methods. 3Q 2003

DELIVERABLES: Develop standards and new mapping software for the new Nikon 5I system. Measure with a complete uncertainty 2 dimensional grids with a fully calibrated system. 4Q 2003

DELIVERABLES: Complete the overlay wafer calibrations and measurements. Continue to work with ISMT on the development of new standard wafers and test structures. Deliver the wafers to the SRM office. 4Q 2003

DELIVERABLES: Complete calibrations of SRM 2059 and the related documentation. Deliver the accompanying documentation to the Office of Standard Reference Materials for distribution to customers. 3Q 2003

Accomplishments

■ ***SRM 2800 Microscope Magnification Standard*** is a standard-size microscope slide with calibrated pitch features ranging from 1 µm to 1 cm. It contains a lithographically produced chrome pitch pattern consisting of a single array of parallel lines with calibrated center-to-center spacings. It contains no linewidth structures. This SRM is intended to be used for the calibration of reticles and scales for optical or other microscopes at the user's desired magnification. The SRM may be used in either transmission or reflection mode optical microscopes, SEMs, or SPMs. Calibration is traceable to the meter through NIST Line Scale Interferometer. Fifty-six units have been calibrated and delivered to the NIST Office of Standard Reference Materials.

■ NIST is currently commencing calibration for *SRM 2059 Photomask Linewidth Standard*, intended to enable customers to make traceable measurements of the dimensions of features on integrated circuit photomasks.

■ New image recognition and quantitative image analysis software has been developed by lead analyst J. Jun of the Precision Engineering Division. This comprehensive software package is based on the Matlab programming language and tool set and allows the evaluation of numerous effects on algorithm performance. The package has been used to quantify feature roughness and asymmetry effects on overlay pattern evaluation used in the feedback and control of lithography stepper tools. It has also been used in the quantification of algorithm

robustness for sample-to-noise effects. This code has been used extensively to evaluate correlation and least-squares.

■ Two sets of overlay wafers have now been received from ISMT. These will be made available in the very near future as RM 8100 for overlay.

■ The overlay metrology project is working closely with several companies such as Schlumberger and KLA Tencor to make available recent important research results on optical characterization, CCD data acquisition calibration, and focus and edge detection work. Neil Sullivan of Schlumberger showed strong interest in strengthening the collaboration with the overlay metrology project. NIST development of new correlation methods and image analysis/ recognition software has enabled the detailed evaluation of noise, feature roughness, and feature inhomogeneity effects on repeatability and robustness of measurement tool performance, issues of paramount importance in semiconductor overlay metrology. We have performed a detailed, in depth study of CCD data acquisition cameras including the development of CCD mapping methods

■ The NIST Overlay Metrology project leader has played a significant role in the Overlay Metrology Advisory Group (OMAG) of ISMT. This group is developing a comprehensive set of measurement guidelines, test methods, and tool performance measures to be adopted by the semiconductor manufacturing industry. The group is made up of more than 15 international semiconductor manufacturers. The OMAG has strong interest in adopting several new methods developed in the NIST Overlay Metrology Project. In particular, the recently published methods for evaluating CCD array performance and overall optical system characterization and calibration performance measures have been adopted.

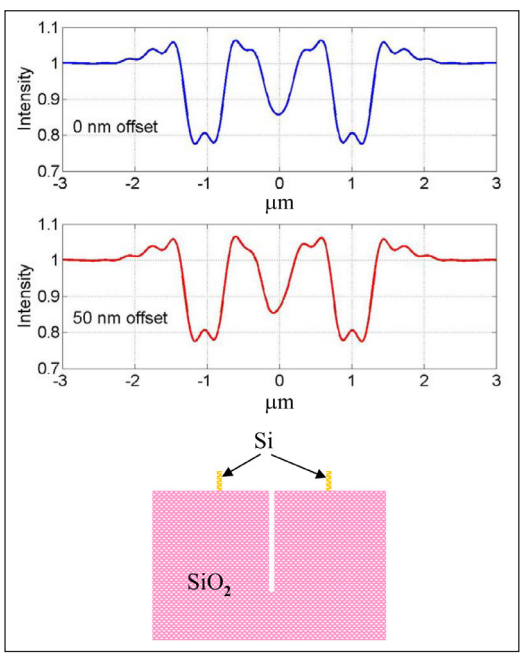

Figure 3. New proposed overlay targets which occupy less than 2 μm x 2 μm in total space. This is designed to be an in chip target.

■ The OMAG organized by ISMT has completed the specification document for the evaluation and benchmarking of overlay metrology tools for semiconductor manufacturing. The document will be used for procuring, testing, and matching tools.

■ The first set of two-dimensional grid artifacts, is known as SRM 5001, and has been received. These 15 cm (6 in) photomasks have been measured on a state-of-the-art I-pro metrology system by the photomask manufacturer. This effort, to make available traceable, 15 cm (6 in) feature placement standards involves a close collaboration between NIST and Photronics. The collaboration employs the industry tool and the traceability of the NIST line scale interferometer with appropriate statistical analysis. The uncertainty budget for grid measurements has been developed and peripheral studies on various items are near completion.

■ NIST researchers have made comparisons between the E. Marx developed optical scattering code with the Spectel company Metrologia metrology modeling package. Different material systems were compared as well as one overlay feature at different focus positions. New results, based on the full integration of the NIST scattering code and Spectel optical microscope model, show very good agreement. This is an important step in the effort to provide industry the quantitative ability to determine sample-dependent effects on overlay tool performance. Results were presented at SPIE Microlithography, 2002.

■ Near completion for the clean room enclosure on the overlay metrology tool. This will allow us to work closely with the industry and make SRMs directly transferable to a clean room environment.

■ Leadership for the industry group for the improvement of mask metrology through process modeling has been transferred to ISMT.

Collaborations:

ISMT, IBM, IVS Schlumberger, KLA-Tencor, Intel, Motorola, AMD and several other leading manufacturers or tool vendors.

The fourteen members of The Neolithography Consortium.

Recent Publications

R. Silver, R. Attota, M. Stocker, J. Jun, E. Marx, R. Larrabee, and M. Davidson, "Calibration Strategies for Overlay Metrology," Proc. SPIE 2003.

R. Attota, R. Silver, M. Stocker, J. Jun, E. Marx, R. Larrabee, and M. Davidson, "A New Method to Enhance Overlay Metrology," Proc. SPIE 2003.

R. Silver, R. Attota, M. Stocker, J. Jun, E. Marx, R. Larrabee, B. Russo, and M. Davidson, "Comparison of Measured Optical Image Profiles of Silicon Lines with Two Different Theoretical Models," SPIE Vol. 4689 (2002).

B. Russo, M. Bishop, D. Benoit, and R. Silver, "Overlay Tool Comparison for sub-130nm Technologies," SPIE Vol. 4689 (2002).

R. M. Silver, S. Gonda, L. Howard, and C. Jensen. "Atomic Resolution Measurements with a New Tunable Diode Laser-based Interferometer," To be submitted to Optical Engineering.

B. Russo, R. Silver et al. "Overlay Benchmarking Report," ISMT 2002.

R. Silver, J. Jun, E. Kornegay, "Recent advances in Overlay Metrology," Future Fab, 2001.

J. Potzick, "The problem with submicrometer linewidth standards and a proposed solution," *Proceedings of SPIE 26th International Symposium on Microlithography*, vol. 4344-20 (2001).

R. M. Silver, J. Jun, E. Kornegay, and R. Morton, "Comparison of Edge Detection Methods using a Prototype Overlay Calibration Artifact," Proc. SPIE Microlithography, Feb. 2001.

T. Doiron and R. Silver, "Two-dimensional grid Standards," Proc. Measurement Sciences Conf., 2000

S. Fox, E. Kornegay, and R. Silver, "Characterization of Imaging Optics and CCD Cameras for Metrology Applications," *Characterization and Metrology for ULSI Technology*, D. Seiler, et. al., eds, A.I.P. Press, 2000, pp. 378-382.

S. Fox, R. Silver, Thesis Advisor, "Focus, Edge Detection, and CCD Camera Characterization for Development of an Optical Overlay Calibration Standard," Graduate Thesis, Univ. of MD, 2000.

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M. Schroeck, and T. Doiron, "Probing of two-dimensional grid patterns by means of camera based image processing," accepted by SPIE for January 2000.

K. Meissner, and T. Wegener, "Robust Regression for Two Dimensional Coordinate Measurements," Proceedings of the International Symposium on Laser Metrology for Precision Measurement and Inspection in Industry, Florianoplis, Brazil, October 13-15, 1999.

R. Silver, T. Doiron, S. Fox, E. Kornegay, M. Takac, and S. Rathjen, Two dimensional Grid Standards, Proceedings of the SPIE, The International Society for Optical Engineering, Metrology, Inspection, and Process Control for Microlithography XIII (1999).

Scanning Probe Microscope (SPM)-Based Dimensional Metrology

Goals

Improve the measurement uncertainty of critical-dimension measurements in the semiconductor industry through improvements in SPM-based measurements. *The International Technology Roadmap for Semiconductors (ITRS)* identifies dimensional metrology as a key enabling technology for the development of next-generation integrated circuits. For example, the goal in 1999 for critical dimension (CD) measurement precision for isolated lines was ± 2.8 nm; this demand tightens to ± 0.8 nm by 2011. The technical focus of this project, development and implementation of scanned probe microscope instrumentation, is driven by the anticipated industry needs for reduced measurement uncertainty, particularly for existing tools such as the SEM.

Customer Needs

The SEM is the current tool of choice for inspection and metrology of sub-micrometer features in the semiconductor industry. SPMs possess unique capabilities, which may significantly enhance the performance of SEMs for in-line critical dimension (CD) measurements, and are also emerging as CD measurement tools in their own right. A creative strategy, which successfully harnesses the strong points of both techniques in order to reduce the measurement uncertainty of sub-micrometer features, will help NIST meet the expectations of the semiconductor industry expressed in the current *ITRS*. As is the case with SEMs, the magnification or scale of an SPM must be calibrated in order to perform accurate measurements. Although many SPMs are commercially available, appropriate calibration standards have lagged. In particular, traceable pitch/height standards with sub-micrometer pitch values are not yet available.

Technical Strategy

SPM development is proceeding along two parallel directions: The first direction addresses dimensional metrology of SPM specifically through an in-house research instrument we refer to as the calibrated atomic force microscope (C-AFM). This instrument, with metrology traceable to the wavelength of light for all three axes of motion, is furthering the design and development of SPM standards as well as providing customers with calibrated dimensional measurements at the nanometer scale. For example, pitch, height, and width measurement capabilities of the C-AFM have been evaluated and validated by internal comparisons. Pitch, ranging up to 20 µm, has been measured with standard uncertainties (u_c) as low as ≈0.5 nm at submicrometer scales and relative standard uncertainties of ≈ 0.1 % at the largest scales. Step height, ranging from a few nanometers up to several hundred nanometers, can be measured with u_c on the order of 0.5 %. The width of submicrometer, nearvertical features, as encountered in CD measurements, can be measured with u_c of ~10 nm, due mostly to the finite size of the SPM tip. As part of the project, we have begun to pursue research in the measurement and standardization of line edge roughness.

DELIVERABLES: Draft standard for calibration of AFM z-scales with Si single atom step heights completed and submitted to ASME and ASTM Standards Committees. 4Q 2003

DELIVERABLES: Report published demonstrating improved uncertainty for linewidth measurements using sharpened tips. 2Q 2004

DELIVERABLES: SRM 2089, a combined pitch and height standard for AFM, released. 2Q 2005

DELIVERABLES: Reports submitted on two remaining international Preliminary Key Comparisons in Nanometrology: 2-D grids, and linewidth. 4Q 2004

DELIVERABLES: Report published demonstrating improved performance of the C-AFM after integration of new x-y stage to increase scan area and reduce motion errors. 1Q 2004

DELIVERABLES: Report published demonstrating traceable measurements of line edge roughness using an AFM. 3Q 2003

The second direction addresses increasingly overlapping demands for dimensional control during fabrication and subsequent calibration of nanometer scale features. For this purpose we employ an SPM-based lithography technique, pioneered at NIST, to produce grating structures with linewidths of 20 nm or below. Latent oxide patterns function as masks for anisotropic wet or

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dry etching. We are also developing an instrument which integrates both SPM and probe station measurement capabilities whereby we are able to compare SPM-based electrical (capacitance and surface potential) and topographical measurements of active device structures simultaneous with traditional current-voltage (I-V) characteristics measured with a probe station. This allows us to examine local nanoscale variations at exposed and buried interfaces of critical dimensioned features in order to identify processing induced variations which contribute to linewidth uncertainty in dimensional and electrical test structures.

DELIVERABLES: Data analysis of optical and SEM images for a series of six 1-D calibration prototypes produced by SPM oxidation and anisotropic etching of silicon. Report in preparation. 2Q 2003

DELIVERABLES: Demonstrate the use of submicrometer-pitch, 2-D grids produced by SPM oxidation and anisotropic etching for controlling the spatial configuration of block co-polymer films. Second phase using large-scale patterned substrates underway. 2Q 2003

DELIVERABLES: Demonstrate a combined maskless optical and SPM lithography system for prototyping sub 100 nm pitch calibration scales integrated onto 1-cm square chips. 3Q 2003

DELIVERABLES: Demonstrate large-scale replication of sub 100 nm pitch 1- and 2-D features using SPM lithography, anisotropic etching, and nanoimprint lithography techniques. 4Q 2003

Accomplishments

■ We are participating in a series of international Preliminary Key Comparisons in nanometrology coordinated by the CIPM (Comité International des Poids et Mesures) CCL (Coordinating Committee for Length). Successful participation in these Comparisons will facilitate international recognition of NIST-traceable measurements of dimensional quantities important to the semiconductor industry. The results are submitted for entry in Appendix B of the Mutual Recognition Arrangement (MRA) between national measurement institutes (NMIs) under which the NMIs recognize each other's measurement capability, thus helping to eliminate technical barriers to trade. Appendix B establishes the technical underpinning of the MRA by showing the technical bases for mutual recognition. Comparisons of 1-D pitch, 2-D pitch, step height, and linewidth measurements are being carried out. During 2002 we completed the measurements and the report for the step height comparison. This was done for steps ranging in height from 7 nm to 800 nm. The final results show that NIST's step height measurements are among the best in the world. Previous C-AFM results for 1-D pitch currently appear in Appendix B.

■ Another effort involves the study of single atomic Si steps as fundamental height standards in the sub-nanometer regime. During 2002 we submitted a draft procedure for AFM z-calibration using the single atom steps to the ASTM Subcommittee 42.14 on STM/AFM and were invited to develop a draft standard based on the procedure.

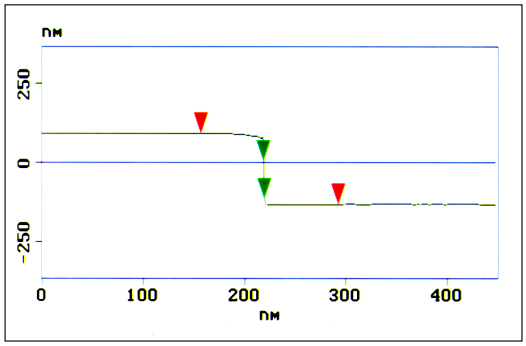

Figure 1. AFM profile of the edge of a prototype linewidth standard, measured with a nanotube probe. The calculated slope angle between the green cursors is approximately 89.6°. Measurement taken by X. Zhao, Guest Researcher; specimen developed by M. Cresswell and R. Allen; probe developed by C. Nguyen, NASA Ames.

■ We are developing techniques to measure linewidths and edges using AFMs with nanotube probes. Recent measurements of a prototype linewidth standard fabricated by colleagues in the Electronics and Electrical Engineering Laboratory (See Fig. 1) show leading edges with slopes higher than 89.5°, thus revealing both the capability of the measurement technique and the quality of the prototype.

■ We also began work on measurement and development of physical standards for line edge roughness (LER), a potential showstopper in the *ITRS*. Initial results of LER measured in cooperation with colleagues in the Building and Fire Research Laboratory are shown in Fig. 2.

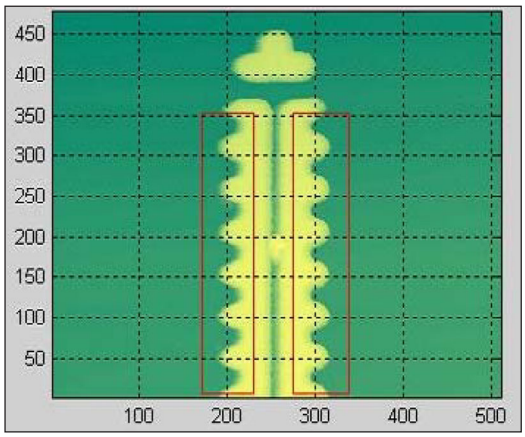

Figure 2. AFM image of a 193 nm lithography test structure used for LER studies. The image shows a periodic LER structure with nominal 800 nm spatial wavelength. Measurements taken by N.G. Orji, Guest Researcher; specimen developed by B. Bunday, International SEMATECH.

■ Ronald Dixson is currently on detail as NIST's first Guest Scientist at International SEMATECH (ISMT). He is working with ISMT researcher, Marylyn Bennett, on calibration and statistical process control techniques to establish ISMT's critical dimension AFM as a reference measurement system (RMS) with close traceability to the SI unit of length. The RMS-AFM is being used primarily for measurements of CD width, but also for step height and pitch as well.

■ In the integrated SPM probe-station thrust, we have completed construction and testing of the combined instrument. Test structures consisting of silicon FETs realized on silicon-on-insulator substrates are being used as a starting point for patterning nanodevices and performing in-situ correlation of the dimensional and electrical properties of these confined regions. SPM lithography has been used interactively with electrical mapping to create successively smaller active gate regions for detailed studies of local device scaling. This capability allows us to examine local nanoscale variations at exposed and buried interfaces of critical dimensioned features in order to identify processing induced variations which contribute to linewidth uncertainty.

■ We have also demonstrated large-scale (100 µm × 100 µm) patterning and anisotropic etching of sub 50 nm linewidth SPM oxide features on 110-oriented silicon substrates, as shown in Figures 3 and 4. A series of six 1-D pitch calibration prototypes were produced and analyzed using calibration optical and SEM instruments at NIST. The absolute placement accuracy of the oxide patterns was determined, allowing an instrument error map to be constructed. Error correction will reduce placement errors to well below 0.1 % over the 100 µm scan range of the SPM, limited by thermal gradients caused by an on-board CCD camera. A new series of prototypes will be produced to demonstrate placement accuracy in the sub 10 nm range. 2-D grid structures have also been fabricated using these methods.

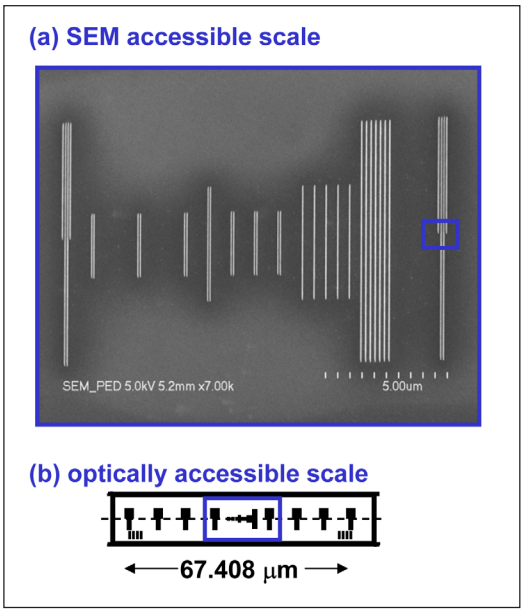

Figure 3. (a) SEM accessible scale of a 1-D pitch calibration prototype produced by SPM oxidation and anisotropic etching of a silicon substrate.
(b) Optically accessible scale with 8 µm pitch.

Collaborations

Department of Mechanical Engineering, University of North Carolina, Charlotte

Physikalisch Technische Bundesanstalt, Braunschweig, Germany

IBM Almaden Research Center, San Jose, CA

Department of Computer Science, University of North Carolina, Chapel Hill NC

School of Mechatronic Engineering, Harbin Institute of Technology, Harbin, China

Departments of Physics and Engineering, University of Akron, Akron OH

National Institute of Advanced Industrial Science and Technology, Tsukuba Japan

National Microelectronics Center of Spain, Barcelona Spain

Center for Measurement Standards, Industrial Technology Research Institute, Hsinchu Taiwan

Department of Physics, National Tsing-hua University, Hsinchu, Taiwan

International SEMATECH, Austin TX

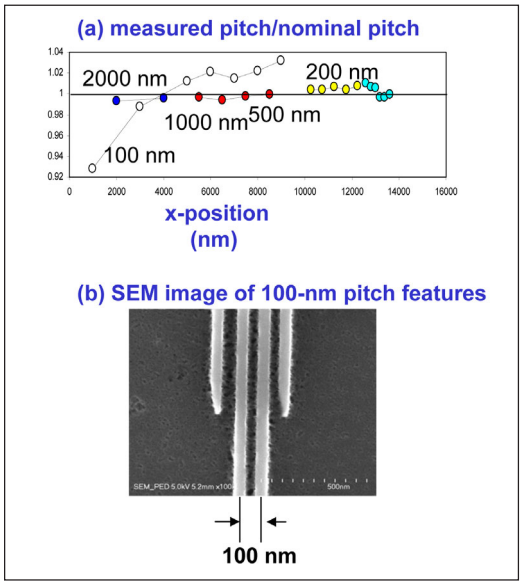

Figure 4. (a) Calibrated pitch measurements from SEM and optical analysis demonstrating 3-4 nm absolute pattern placement accuracy for etched SPM oxide features patterned on a silicon substrate.

Recent Publications

N. G. Orji, M. I. Sanchez, J. Raja, and T. Vorburger, "AFM Characterization of Semiconductor Line Edge Roughness," *Applied Scanning Probe Methods* (in press).

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X. Zhao, T. V. Vorburger, J. Fu, J. Song, and C. V. Nguyen, "A Model for Step Height, Edge Slope and Linewidth Measurements Using AFM," Proc. 2003 ULSI Conference (to be published).

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F. Perez-Murano, C. Martin, N. Barniol, H. Kuramochi, H. Yokoyama, and J.A. Dagata, "Measuring electrical current during scanning probe oxidation," Appl. Phys. Lett., May 2003, in press.

C. Harrison and J. A. Dagata, "Lithography with Self-assembled Copolymer Microdomains," in *Self-Assembly* (tent.), I. Hamley, ed., (John Wiley, NY, 2003), in press.

N. Farkas, G. Zhang, E. A. Evans, R. D. Ramsier, and J. A. Dagata, "Nanoscale Oxidation of Zirconium Surfaces: Kinetics and Mechanism," J. Vac. Sci. Technol. B, in press.

N. Farkas, G. Zhang, K. M. Donnelly, E. A. Evans, R. D. Ramsier, and J. A. Dagata, "The role of subsurface oxygen in the local oxidation of zirconium and zirconium nitride thin films," Thin Solid Films, submitted.

J. Jun, F. S. Chien, W. F. Hsieh, S. Gwo, R. M. Silver, A. E. Vladar, and J. A. Dagata, "Calibration of a Prototype Silicon Pitch Standard by Scanning Probe Oxidation and Anisotropic Etching," J. Res. NIST, in preparation.

Electrical-Based Dimensional Metrology

Goals

Develop test-structure-based electrical metrology methods and related reference materials with emphasis on linewidth and overlay metrology-tool calibration; contribute to standards organizations supporting the development of metrology standards for the semiconductor tool industry; target the specific near-term goal of fabricating a quantity of reference-features with nominal critical dimensions (CDs) in the range 70 nm to 100 nm having CD uniformities of 1 nanometer per micrometer by June 2003.

Figure 1. Christine Murabito using a hot plate to do a post-exposure bake during the photolithography process.

Customer Needs

The Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors *(ITRS)* states that it is critically important to have suitable reference materials for lithography support available when on-wafer measurements are made as a new technology generation in integrated circuit (IC) manufacturing is introduced, and particularly during development of advanced materials and process tools. Each generation of ICs is characterized by the transistor gate length whose control to specifications during IC fabrication is a primary determinant of manufacturing success. The SIA projects the decrease of gate linewidths used in state-of-the-art IC manufacturing from present levels of up to 250 nm to below 70 nm within several years. Scanning electron microscopes (SEMs) and other systems used for traditional linewidth metrology exhibit measurement uncertainties exceeding *ITRS*-specified tolerances for these applications. It is widely believed that these uncertainties can be at least partially managed through the use of reference materials with linewidths traceable to nanometer-level uncertainties. Until now, such reference materials have been unavailable because the technology needed for their fabrication and certification has not been available.

It is also widely believed that the usefulness of SEM metrology for monitoring wafers in advanced development and production may become inadequate at some future IC generation. Thus, there exists a need for new methodology to meet future metrology requirements.

Technical Strategy

The technology that the project staff have developed for fabricating linewidth and overlay reference materials is known as the Single-Crystal CD Reference-Material implementation. Patterning with lattice-plane selective etches of the kind used in silicon micro-machining provides reference features with quasi-atomically planar sidewalls over local length segments of the reference feature, typically extending to several micrometers. This unique attribute is highly desirable for the intended applications, particularly if the quasi-atomically planar sidewall smoothness can be further extended to reference-feature segment lengths of up to 10 micrometers. Essential elements of the technology implementation include starting silicon wafers having a (110) orientation; alignment of the reference features to specific lattice vectors; and lithographic patterning with lattice-plane selective etches of the kind used in silicon micro-machining.

The traceability path for dimensional certification is provided by High-Resolution Transmission Electron Microscopy (HRTEM) imaging. This method provides nanometer-level accuracy, but is sample-destructive and thus is impractical on a 100 % basis. The project's traceability strategy has thus featured the sub-nanometer repeatability of electrical CD metrology as a secondary reference means. Low-cost, whole-wafer electrical measurements are effectively calibrated with a limited number of HRTEM lattice-plane image counts made on a selection of reference features that are replicated on other chips on the same wafer. Typical reference features are several-hundred lattice planes wide. A technique of making lattice-plane

Technical Contact:
Michael W. Cresswell

I would like to thank you and NIST for your pioneering work on silicon pocket wafer technology. We have now incorporated this technology in one of our products. We also regard very highly your work on the single crystal linewidth standard. We see this as the first and only attempt by anyone in the world to produce a linewidth standard traceable to the fundamental units of measure, in the sub-100 nm range, for use in the semiconductor industry.

This work is of technical and economic importance to the semiconductor industry, because the ability to correctly size ever smaller lateral dimensions on silicon substrates is key to the manufacturing yield of silicon chips.

We look forward to a continuing technical relationship between VLSI Standards and NIST."

Marco Tortonese, Ph.D., Engineering Manager, VLSI Standards, Inc.

"The three-way partnership between International SEMATECH, VLSI Standards, and NIST is driving towards creating a CD standard which is critically needed as the industry goes below 65 nm."

Hal Bogardus, International SEMATECH

image counts, by automated analysis of HRTEM phase-contrast images, was developed in order to minimize the uncertainties of the linewidths of the standards due to lattice-plane counting.

An important metric of the progress and success of the project is the level of uncertainty attributed to the product CD reference features. The units that were delivered to International SEMATECH (ISMT) last year, per contractual arrangements, typically exhibited 14 nm uncertainty. This level is considered by the industry to be four to five times higher than what is desired for the roadmap out years. Therefore, the main target of the project during the current year is reducing uncertainty to 4 nm or better.

Our recent results have indicated that a significant portion of the uncertainty in the certified linewidth of the finished product is attributable to variations, which are typically up to tens of nanometers, in the physical linewidth of the features over segment lengths of typically ten micrometers. Since electrical CD metrology effectively extracts the average width of a reference feature, it is insensitive to these physical CD variations. Consequently, it can contribute commensurate uncertainties of local linewidths of the finished product. The current year's effort has therefore focused on reducing the macroscopic variations of the physical CDs of the reference features by refinements to the starting-material specifications and to the wafer-fabrication process.

The technical strategy has to be responsive to industry's requirement for reference materials to have the physical properties of standard 200 mm wafers. Since 200 mm (110) starting material is virtually unobtainable at an acceptable cost, this project's technical strategy has been to dice each 150 mm (110) wafer after lithography and to mount the separate chips in micro-machined standard 200 mm wafers to accommodate the test chips. The result is that finished units are rendered metrology-tool-compatible at an acceptable cost. The entire fabrication and certification process is planned to be transferred to a commercial standards vendor.

However, some leading semiconductor manufacturers are now requesting single full-wafer implementations at the 200 mm and 300 mm diameter levels. Accordingly, the current year's effort has also addressed this issue.

In the current year, project researchers have set up a chip-level reference-material patterning facility at the ISMT facility in Austin. One leading motivation for this effort was the ready availability of SEM imaging facilities having a capability to inspect the high volume of reference-material chips being generated by processing variations. The latter are directed at reducing single-feature CD variation to below the several-nanometer level. In addition, qualified operating staff were also made generously available. ISMT has been contributing 20 to 40 hours of SEM machine time per week, with operators. In addition, the project has access to a state-of-the-art dual-beam focused ion beam (FIB) inspection tool and operator staff for necessary cross section measurements on an as-needed basis.

Figure 2. Richard Allen and Michael Cresswell discuss SEM measurements of prototype reference materials with Laurie, an International SEMATECH staff member, in Austin, Texas.

A second motivation for setting up the reference-material patterning facility at the ISMT facility in Austin was essential proximity to the Advanced Technology Development Facility (ATDF), which is being operated by a NIST assignee from the Manufacturing Engineering Laboratory in ISMT's clean room. Our current year's CD-variation control effort has depended exclusively on this one-of-a-kind world-class installation and the unique skills of the NIST assignee. As stated previously, the atomic force microscope (AFM) facility is intended also to serve as an alternative transfer-calibration tool.

The lithography for the wafers that have been used during the current year to facilitate our uncertainty-reduction experiments was conducted at the Microelectronics Development Sandia Laboratory at Sandia National Laboratories and at the Scottish Micro-electronics Centre of the

University of Edinburgh. These activities were funded by ISMT, but the technical direction was provided by project staff at NIST.

The member companies of the project's major client, ISMT, insist that transfer of the Single-Crystal CD Reference-Material (SCCDRM) technology to a commercial standards manufacturing and marketing company organization be an integral part of the project. Therefore, ISMT and NIST have agreed that VLSI Standards, Inc., of San Jose, California, be invited to contribute to the new phase of the project that is described below. One immediate outcome has been that we have honored a request to incorporate scatterometry targets in the next design iteration.

DELIVERABLES: Design improved Single-Crystal Silicon-on-Insulator and bulk CD reference materials, procure photomasks and starting materials, and deliver to ISMT and its contractor for CD reference-material fabrication. Include scatterometry target grids in the layout. 2Q 2003

DELIVERABLES: Develop patterning processes capable of replicating reference features in bulk and Silicon-on-Insulator (SOI) with line-edge roughness below 5 nanometers extending up to 10 micrometer feature lengths. Patterning processes are to include procedures for removing particles and precipitates having low-single nanometer dimensions that are typically produced by the patterning-process chemistry. In addition, develop decontamination procedures for removing organic side-wall residues that are not detectable by electron-beam imaging but adversely affect AFM transfer metrology. 3Q 2003

DELIVERABLES: Evaluate new vertical etch-stop implementations to enhance reference-feature straightness, edge roughness, and side-wall quality. In particular, design, fabricate, and evaluate buried boron profiles. Also, replicate reference features in high-resistivity epitaxial silicon device layers grown on highly-doped boron substrates. Include evaluation of stencil-mask based sub-tenth micro-meter lithography techniques being sponsored by ISMT and respond to requests by member companies to develop a single full 200 mm wafer implementation. 4Q 2003

DELIVERABLES: Fabricate and calibrate scatterometry targets using the single-crystal reference-material implementation. Invite industry partners to evaluate performance benefits produced by alternative starting-material etch stops. Fabricate a selection of reference materials having features replicated in metal and polysilicon with built-in rulers provided by HRTEM illumination. 1Q 2004

Accomplishments

■ *A selection of SIMOX (Separation by Implantation of Oxygen) and bulk (110) 150 mm wafers was procured, pre-processed, and delivered to Sandia National Laboratories for lithography on behalf of client ISMT. NIST project staff also designed a new reference-feature layout and procured the 5X mask that was used for this Sandia operation.* The lot-split processing was specified by this project and featured pre-patterning by reactive-ion etching for reference-feature dimensional uniformity and plasma etching of the SIMOX-wafer buried oxides to investigate control of substrate contamination during SEM inspection. The Sandia work was funded by ISMT. The finished wafers were delivered to NIST for dicing prior to being taken to ISMT for completion of processing at the chip level.

■ *A collection of 75 mm (110) wafers was procured, re-flatted at NIST to meet orientation requirements, and, after implant pre-processing, delivered to the Scottish Microelectronics Centre (SMC) at the University of Edinburgh for silicon-nitride hard-mask deposition and patterning by g-line stepper to our specifications.* The lot-split processing was specified by this project and featured SOI as well as p^+np and n^+p buried junctions to isolate the patterned layers electrically. This work was also funded by ISMT. A subset of wafers was patterned collaboratively at the SMC by NIST, SMC, and ISMT staff before being returned to NIST for dicing and then to ISMT for pattern-transfer from the hard mask.

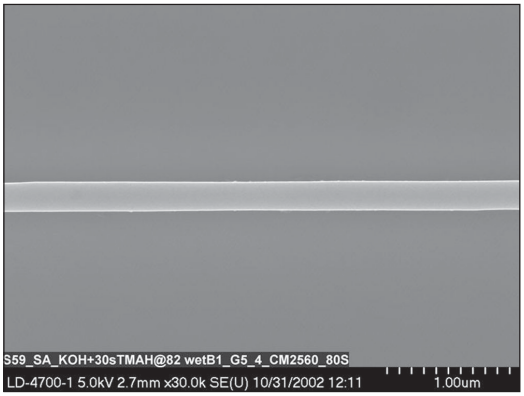

Figure 3. This image of a S59-SA-G5-4 feature, patterned by hybrid KOH/TMAH etching, was taken prior to cleaning. It is estimated to be uniform to within less than 3 nm over 4 micrometers.

■ *A facility for patterning individual reference-feature chips was set up and operated at ISMT. Processes, including cleaning protocols, for silicon pattern-transfer and nitride hard-mask removal at the chip level were established and documented.* Chemical variables that were optimized for pattern-transfer include TMAH-etch immersion time and temperature for the various available substrate boron-doping levels. The variables that were optimized for nitride hard-mask stripping include immersion-time and phosphoric-acid temperature and concentration. Comparisons between straight TMAH and hybrid TMAH/KOH etching processes were also investigated and reported.

■ *Protocols for SEM imaging and evaluation of large quantities of reference features by ISMT operators were established and implemented.* The problem addressed was screening and inspecting thousands of top-down reference-feature images for fabrication-process development purposes and for selecting reference features for AFM and HRTEM imaging, both of which are very costly and time-consuming operations. In order to maintain the inspection budget below $20K per month, a hybrid optical/SEM inspection process was implemented and interfaced with a database that has been designed by project staff. In addition, image-analysis software was purchased and modified to allow off-line, large-sample, CD extraction from high-density SEM images of single features. This result was facilitated through collaboration with Hitachi Instruments, FEI, Inc., Image-Pro Company, Leeds Instrument Company, and SEM image-analysis specialists at NIST/MEL and ISMT.

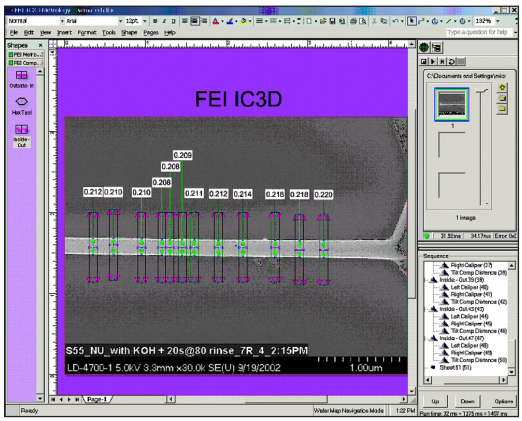

Figure 4. This image, as analyzed by FEI Inc., indicates a 4 nm CD range over 2 µm of feature length.

■ *Chip-patterning processes to reduce line-edge roughness developed and demonstrated.* The accomplishments listed above were applied to the identification of a hybrid TMAH/KOH etching process that reduces average line-edge roughness from last year's 14 nm to typically 6 nm on SOI material. This is a very important result because it is a prerequisite for the reduction in final-product uncertainty to levels consistent with requirements of the 70 nm node. Key contributions to achieving this result were made by the staff of the Failure-Analysis Laboratory and numerous other professional staffers at ISMT in Austin.

■ *The project's selected technology-transfer partner, VLSI Standards, Inc., of San Jose, California, has formally agreed to support the project by making its 150 mm wafer clean room, which is equipped with an i-line stepper, available for performing the lithography for the project's next generation of SCCDRMs.* The collaborative agreement, which was recently concluded, provides for project staff at NIST to design the reference features which will include a novel set of scatterometry targets. The NIST project team has also written the starting-material specifications, scheduled the pre-processing ion implants, and taken responsibility for the technical management of the next phase of the three-way collaborative project phase. ISMT will provide the chip-level processing facilities and the AFM transfer-calibration measurements, and will fund the HRTEM microscopy.

FY Outputs

Collaborations

■ International SEMATECH member companies (AMD, Compaq, Conexant, Hewlett Packard, IBM, Intel, Lucent Technologies, Motorola, Texas Instruments, Hyundai, Infineon Technologies, Philips, STMicroelectronics, TSMC), Development of single-crystal critical dimension reference materials (Michael W. Cresswell and Richard A. Allen).

■ International SEMATECH, Development of single-crystal critical dimension reference materials (Michael W. Cresswell and Richard A. Allen).

■ NIST Division 821, Bill Penzes, Development of electrically calibratable stage micrometer (Richard A. Allen).

- Photronics, Development of optical/electrical hybrid critical dimension measurement for photomasks (Richard A. Allen and Michael W. Cresswell).

- Sandia National Laboratories Microelectronics Development Laboratory, Sandia National Laboratories Compound Semiconductor Research Laboratory, Sandia National Laboratories Integrated Materials Research Laboratory, NIST ITL, MSEL, MEL, and International SEMATECH on Fabrication and certification of reference materials for linewidth and overlay metrology (Michael W. Cresswell, Loren W. Linholm, and Richard A. Allen).

- Sandia National Labs, NIST Divisions 898, 855, and 821, University of Central Florida, and International SEMATECH, Reference artifacts for critical dimension measurements (Michael W. Cresswell, Loren W. Linholm, and Richard A. Allen).

- University of Edinburgh, U.K., and International SEMATECH, Process development for single-crystal critical dimension reference materials (Michael W. Cresswell, Loren W. Linholm, and Richard A. Allen).

- VLSI Standards, Development of single-crystal critical dimension and overlay reference materials (Michael W. Cresswell and Richard A. Allen).

- VLSI Standards, Inc., and ISMT, Development of commercial architecture and distribution plan for single-crystal CD reference materials (Michael W. Cresswell and Richard A. Allen).

- VTT Finland and George Washington University, Develop non-contact test structures and methods (Richard A. Allen, Michael W. Cresswell, and Loren W. Linholm).

- VTT Finland, Design and fabrication of capacitance sensors based on co-fired ceramic technology (Michael W. Cresswell).

Standards Committee Participation

- Electrical Test Structures Task Force, Co-Chair (Richard A. Allen).

- SEMI International Standards Microlithography Committee, member (Richard A. Allen).

External Recognition

- Senior Member, IEEE, elected Jun. 2002 (Richard A. Allen).

Recent Publications

M. W. Cresswell, J. E. Bonevich, R. A. Allen, N. M. Guillaume, L. A. Giannuzzi, S. C. Everist, C. E. Murabito, P. J. Shea, L. W. Linholm, "Electrical Linewidth Test Structures Patterned in (100) Silicon-on-Insulator for Use as CD Standards," IEEE Transactions on Semiconductor Manufacturing, Vol. 14, No. 4, pp. 356-364, (01-NOV-2001).

R. A. Allen, M. W. Cresswell, C. E. Murabito, W. F. Guthrie, L. W. Linholm, C. H. Ellenwood, E. H. Bogardus, "Test Structures for Referencing Electronics Linewidth Measurements to Silicon Lattice Parameters Using HRTEM," Proceedings of the 2002 ICMTS, IEEE 2002 International Conference on Microelectronic Test Structures, Apr 09-11, 2002, Cork, Ireland, pp. 13-18, (08-APR-2002).

B. A. am Ende, M. W. Cresswell, R. A. Allen, T. J. Headley, W. F. Guthrie, L. W. Linholm, E. H. Bogardus, C. E. Murabito, "Measurement of the Linewidth of Electrical Test-Structure Reference Features By Automated Phase-Contrast Image Analysis," Proceedings of the 2002 ICMTS, IEEE 2002 International Conference on Microelectronic Test Structures, Cork, Ireland, Vol. 15, pp. 1-5, (01-APR-2002).

M. W. Cresswell, E. H. Bogardus, J. V. Martinez de Pinillos, M. H. Bennett, R. A. Allen, W. F. Guthrie, C. E. Murabito, B. A. am Ende, L. W. Linholm, "CD Reference Materials for Sub-Tenth Micrometer Applications," Proceedings of the SPIE, SPIE's 27th Annual International Symposium and Education Program on Micro-lithography, Mar 03-08, 2002, Santa Clara, California, Vol. 4689, pp. 116-127, (01-JUN-2002).

N. M. Guillaume, M. Lahti, M. W. Cresswell, R. A. Allen, L. W. Linholm, M. E. Zaghloul, "Non-contact Electrical Critical Dimensions Metrology Sensor for Chrome Photomasks," SPIE, 21st Annual BACUS Symposium on Photomask Technology, Oct 02-05, 2001, Monterey, California, Vol. 4562, (30-NOV-2001).

R. Schlaf, Y. Emirov, J. A. Bieber, A. Sikder, J. Kohlscheen, D. A. Walters, M. R. Islam, B. Metha, Z. F. Ren, T. L. Shofner, B. B. Rossi, M. W. Cresswell, "Using Carbon Nanotube Cantilevers in Scanning Probe Metrology," Proceedings of the SPIE, SPIE's 27th Annual International Symposium and Education Program on Microlithography, Mar 03-08, 2002, Santa Clara, California, p. 53, (01-JUN-2002).

Small Angle X-ray Scattering (SAXS)-Based Dimensional Metrology

Technical Contacts:
Ronald L. Jones
Tengjiao Hu
Eric K. Lin
Wen-li Wu

Goals

To develop a new SAXS-based methodology to quickly, quantitatively, and non-destructively measure critical dimensions and feature shape with sub-nanometer resolution on production scale test samples. Quantities of interest include critical dimension, sidewall angle, and statistical deviations across large areas. Of particular focus is delivering an absolute determination of parameters contributing to line edge roughness, such as fluctuations in critical dimension over large areas and correlations in these fluctuations along a sidewall. In addition to addressing the metrological needs of future technology nodes, the sub-Angstrom wavelengths utilized by SAXS based measurements offer the possibility of calibration and testing of current metrological tools based on light scatterometry, SEM, and AFM.

Customer Needs

The drive to reduce feature sizes to the sub 100 nm regime outlined by the ISMT Roadmap continues to challenge metrology techniques for pattern characterization. As pattern sizes decrease, existing techniques such as CD-SEM face significant technical hurdles in imaging quantities such as Line Edge Roughness (LER). Emerging metrologies based on techniques such as atomic force microscopy are still being evaluated, providing a lack of clear definition in suitable metrology for standardized measurements of both organic and inorganic structures. To address these issues, NIST is evaluating the potential application of x-ray scattering as a metrology tool for both fundamental photoresist research and in the production of standards for industrially practiced metrologies such as CD-SEM.

Technical Strategy

1. The implementation of 157 nm wavelength exposure tools and resists expected by 2005 will further restrict the critical dimension (CD) budget, requiring control of CD to within 10 nanometers. Further reductions will demand sub-nanometer precision. These requirements will challenge traditional methods including CD-SEM, AFM, and light scatterometry. We are developing a transmission scattering based method capable of angstrom level precision in critical dimension evaluation over large (50 µm x 50 µm) arrays of periodic structures. In contrast to light scatterometry, SAXS is performed in transmission (see Fig. 1) using a sub-Angstrom wavelength. With a wavelength more than an order of magnitude smaller than the pattern size, the patterns are characterized using methods employed in crystallographic diffraction. The high energy of the x-ray allows the beam to pass through a production quality silicon wafer, and is therefore amenable to process line characterization. As with light scatterometry, the measurements are performed in ambient conditions, minimizing time required for sample preparation. The current capabilities of commercially available x-ray sources and detectors suggest that the technique is portable to a laboratory scale device capable of high precision measurements.

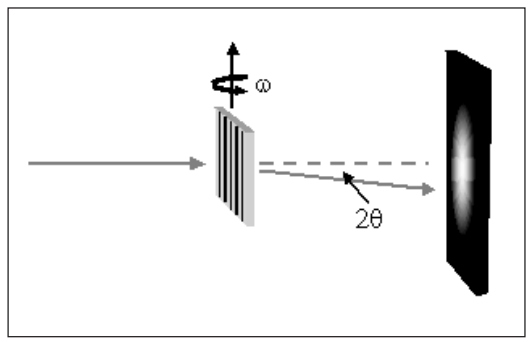

Figure 1. Schematic of the SAXS transmission geometry. Shown is the x-ray beam (solid line) as it passes through the patterned sample and scattered at an angle 2θ. For a precisely aligned sample with known composition, a 3-d lineshape is obtained in one transmission measurement. Unknown samples with less alignment precision can also be characterized through measurements at a variety of sample angles, ω.

While a laboratory scale device is technically feasible, we have chosen to develop the technique using a synchotron x-ray source. The synchotron provides a tunable energy and a wide array of optical components that enhance our ability to determine optimal configurations. At present, however, the high flux of the x-ray source is not deemed a requirement of the technique.

DELIVERABLES: Provide SAXS measurements of Critical Dimension and Linewidth with sub-nanometer precision in a patterned oxide grating. 3Q 2003

DELIVERABLES: Investigate specifications required for general apparatus, including laboratory scale device, including wavelength, incident flux, and detectable background. 3Q 2003

2. Characterization of pattern quality includes shape factors indicating the slope of the line edge and curvature. Using the above protocol for scattering, measurements taken at a series of angles of incidence allows the reconstruction of the line shape in a manner similar to microscopic tomography. We have performed an initial set of tests using multiple angles on a test grating and determined an ability to measure sidewall angle to within 1°. Ongoing analysis and technique refinement will provide additional shape factors, allowing determination of more complex shape information such as sidewall curvature. Fluctuations in critical dimension result from both mask related issues, such as overlay or defects, and factors related to the image development within the photoresist, such as acid diffusion. Fluctuations in CD are observed through spreading of the Bragg diffraction peaks, requiring a precise determination of resolution smearing effects. Using a 2-D detector, the entire projected shape of structures such as via pads and contact holes are obtained in one measurement.

DELIVERABLES: Provide measurements of line shape in terms of simple trapezoidal model for grating patterns. 3Q 2003

DELIVERABLES: Provide 2-D measurements of via-pad patterns etched in oxide including pitch and pattern sizes along each dimension in one measurement. 4Q 2003

3. Current Line Edge Roughness (LER) and CD specification of LER in CD budgets requires high precision metrology for both quality control by vendors as well as quality assessment by customers. Metrologies such as CD-SEM, a top down technique, measure qualitatively different quantities compared to that of light scatterometry and AFM. Our approach is to provide metrology of sidewall roughness, where sidewall roughness is defined by deviations from the average sidewall plane on length scales smaller than the CD. These measurements can then be connected to varying definitions of LER through cross measurement of samples with, for instance, CD-SEM. In the case of photoresists, we are employing AFM to provide the appropriate wavevector range, or frequency spectrum, over which correlations exist. These data are being used to develop the appropriate neutron and x-ray optical configurations for sidewall roughness characterization. Our goal is to produce techniques applicable to a wide range of roughness types and size scales.

DELIVERABLES: Provide relevant wavevector range for sidewall roughness scattering measurements. 4Q 2003

DELIVERABLES: Develop metrology of sidewall roughness based on small angle scattering. 1Q 2004

4. A general technique for pattern characterization in the microelectronic industry involves the evaluation of patterns constructed from metals, oxides, low-k dielectrics, and polymers. The application of SAXS to this wide range of materials is possible due to the large disparity in electron density between all of these materials and air. Sufficient contrast is also present for some combinations of materials, including copper interconnects buried in a low-k matrix. The transmission geometry allows the probing of densely packed structures whether buried or exposed, providing maximum measurement flexibility. A systematic series of tests will be performed on structures produced from various materials from different stages of circuit production. Plans include measurements of patterns from initial photoresist at the gate level through double-damascene and the second metal deposition.

DELIVERABLES: Direct comparisons of photoresist patterns and the resulting etched low-k matrix. 1Q 2004

DELIVERABLES: Measurement of a copper pattern in a low-k matrix. 1Q 2004

Accomplishments

- We provided the first measurements of critical dimension using small angle x-ray scattering (SAXS). Using a series of etched oxide gratings produced at International SEMATECH (W. Chism), transmission SAXS was performed using the ID-9 Beamline at the Advanced Photon Source (Argonne National Laboratory). The 1-dimensional Bragg diffraction pattern shown in Fig. 2 is characteristic of a uniformly spaced grating, where the orientation of the lines is perpendicular to the diffraction axis. Prior studies with neutron scattering have demonstrated the

effectiveness of using data measured at multiple angles (designated by the angle ω in the schematic in Fig. 1). The data below indicate a dramatic reduction in Bragg scattering as the sample is rotated from 0 deg (left) to 2.5 deg (middle) and 5.0 deg (right). In contrast to prior work with neutron scattering, the beam size is comparable to current test structures used for light scatterometry (< 100 µm), with further reductions possible down to 30 µm using traditional optical elements to define the beam. The large number of diffraction peaks is indicative of the highly correlated order of the repeating pattern. In addition, the line broadening of each diffraction spot perpendicular to diffraction axis is directly related to line roughness.

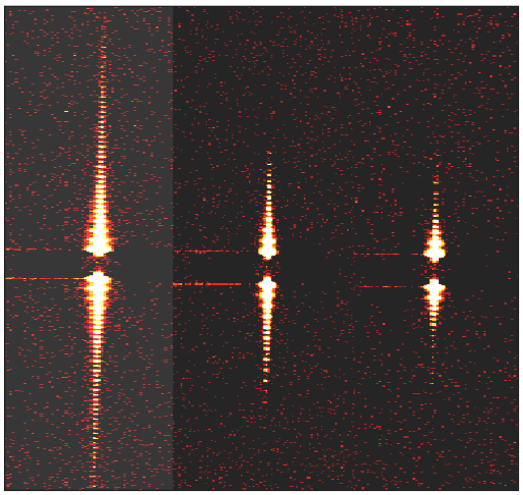

Figure 2. SAXS transmission scattering measured on a 2-D detector of a dense line oxide pattern. Shown are the same sample measured at three orientations: 0.0º (left), 2.5º (middle), 5.0º (right).

■ SAXS measurements of a series of "via-pad" patterns etched in oxide (produced by ISMT, W. Chism) provided a simultaneous characterization of the complete 2-dimensional pattern projection as seen in Fig. 3. In contrast to the line patterns shown in Fig. 2, the shape of the via-pad, effectively a rectangle with rounded corners, results in a series of Bragg diffraction peaks along orthogonal axes. The larger number of peaks along one axis suggests a higher level of pattern definition and less deviation from the average pitch in this direction. In addition, the asymmetry of the peak spacing suggests the ratio of the lengths of the sides. As an example, a rectangular pattern would have equivalent Bragg spacing along both axes.

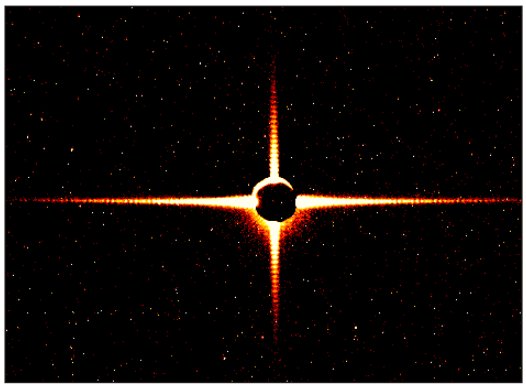

Figure 3. 2-D scattering pattern from a repeating pattern of rectangular "via-pads" etched into the oxide layer. Diffraction peaks are observed along two orthogonal axes.

■ SAXS measurements of test oxide line gratings have demonstrated sub-nanometer precision in both average pitch and average line width. The precision of this measurement is in part dictated by the number of observable diffraction orders, which is in turn limited by the wavelength resolution and pattern quality. Using a pair of crystal monochromators and two bent mirrors, the resolution of the SAXS measurement was increased to produce more than 30 orders of observed diffraction orders. A linear fit of their position as a function of their order provides a slope inversely proportional to the average repeat distance, or pitch (see Fig. 4). Ongoing studies will compare these results with measurements from light scatterometry, atomic force microscopy, and scanning electron microscopy.

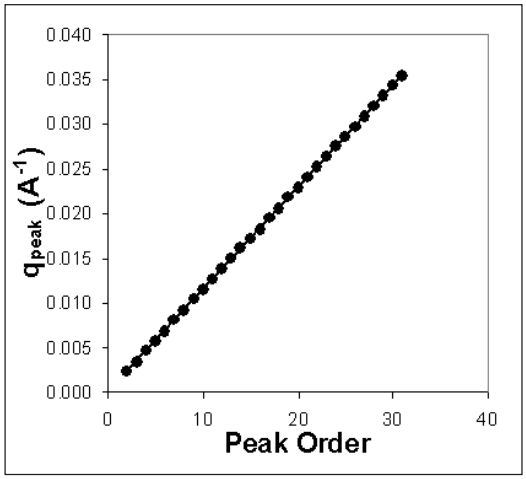

Figure 4. Position of diffraction peak in q-space (proportional to scattering angle 2θ) as a function of peak order. The slope is inversely proportional to repeat distance of the pattern, or pitch. Sub-nanometer precision is obtained from the 30 orders produced by the oxide test grating.

Collaborations

International SEMATECH, Will Chism, Pattern production and correlation to light scatterometry.

IBM Yorktown Heights, Arpan Mahorowala, Transfer of Line Edge Roughness in 193 nm Photoresists to the Underlying Substrate during RIE.

IBM Yorktown Heights, Dario Goldfarb, Marie Angelopolous, Contributions to Line Edge Roughness.

Shipley, Inc., Patrick Boulton, George Barclay, Photoresist Patterning.

Advanced Photon Source, Argonne National Laboratory, Diego M. Casa, Small Angle X-ray Scattering Instrumentation Development.

ExxonMobil, Inc., Rainer Kolb, Small Angle X-ray Scattering Instrumentation Development.

Recent Publications

R. L. Jones, T. Hu, D. M. Casa, Eric K. Lin, W.-L. Wu, P. J. Bolton, G. G. Barclay, "Small Angle X-ray Scattering for sub 100 nm Pattern Characterization," Appl. Phys. Lett. Submitted (2003).

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W. Wu, E. K. Lin, Q. Lin, and M. Angelopolous, "Small Angle Neutron Scattering Measurements of Nanoscale Lithographic Features," J. Appl. Phys. **88**, 7298 (2000).

Model-Based Linewidth Metrology

Technical Contacts:
John Villarrubia
András Vladár

"[The] theoretical work on the behavior of the probe-sample interaction has had a profound influence on our ability to quantitatively analyze probe microscope images."

—Joseph Griffith, Bell Labs, Lucent Technologies

"The modeling work … for electrical CD, AFM, and CDSEM is of value to us ... The current crisis in CD offset uncertainty may be partially answered by this work."

—Anonymous industry feedback to NIST.

Goals

The goal of this project is to address the metrology needs of industry, particularly the U.S. semiconductor industry, for linewidth metrology with uncertainties of a few nanometers.

Customer Needs

"Lithography metrology continues to be challenged by rapid advancement of patterning technology. Critical dimension measurement capability does not meet precision requirements which comprehend measurement variation from individual tool reproducibility and tool to tool matching…CD measurement must be extended to line shape determination." **International Technology Roadmap for Semiconductors, Metrology Section, p. 7 (2001).**

Due to the changing aspect ratios of IC features, besides the traditional lateral feature size, e.g. linewidth measurement, full three-dimensional shape measurements are gaining importance and should be available inline. Development of new metrology methods that use and take the full advantage of advanced digital image processing and analysis techniques and networked measurement tools will be needed to meet the requirements of near future IC technologies. **International Technology Roadmap for Semiconductors, Metrology Section, p. 6 (2001).**

"…the exponential rise in value of each nanometer, as nominal gate dimensions shrink, can be estimated… Under these assumptions, the value of CD control for the 180 nm generation of microprocessors exceeds $10 per nanometer." **C. P. Ausschnitt and M. E. Lagus, IBM Advanced Semiconductor Technology Center, Proc. SPIE Vol. 3332, p. 212 (1998).**

A feature's width is one of its fundamental dimensional characteristics. Width measurement is important in a number of industries including the semiconductor electronics industry, which had approximately $138 billion in worldwide sales in 2002.[1] As a measure of its importance in that industry, consider that the term "critical dimension" or "CD" is used there nearly interchangeably with "linewidth," and semiconductor device generations are known according to the characteristic width of the features, as in "the 90 nm generation."

Existing linewidth standards are optical photomask standards, the minimum linewidth of which is 0.25 µm with a combined expanded uncertainty of ≈10 nm (coverage factor 2). To support present and future semiconductor technologies, industry needs to measure gate widths with total uncertainties, as identified in the International Technology Roadmap for Semiconductors (ITRS), of less than 10 nm and with measurement repeatabilities of better than 1 nm. Neither NIST nor any other national laboratory presently offers a wafer linewidth measurement service or SRM with this level of accuracy.

A line's width must generally be determined from its image. However, the image is not an exact replica of the line. The scanning electron microscope (SEM), scanning probe microscope (SPM), and optical microscope all have image artifacts that are important at the relevant size scales. Physical linewidth determination therefore requires modeling of the probe/sample interaction in order to correct image artifacts and identify edge locations. Barriers to accurate linewidth determination include inadequate confidence in existing models, the complexity and consequent expense of using some models, inadequately quantified methods divergence, and ignorance of best measurement practices.

Technical Strategy

The scope of the model-based linewidth metrology project includes the development and improvement of computational models to simulate the artifacts introduced by measuring instruments, inversion of these models (to the extent possible) to deduce the sample geometry that produced a measured image, validation of models by appropriate experiments, development and testing of measurement processes that provide the necessary inputs for model-based deduction of sample width and shape, estimation of uncertainties for the measurement process, assistance to industry linewidth measurement by communication of best practices, and laying of the necessary research groundwork for a future linewidth and/or line shape Standard Reference Material.

1 Computed using statistics compiled by the Semiconductor Industry Association.

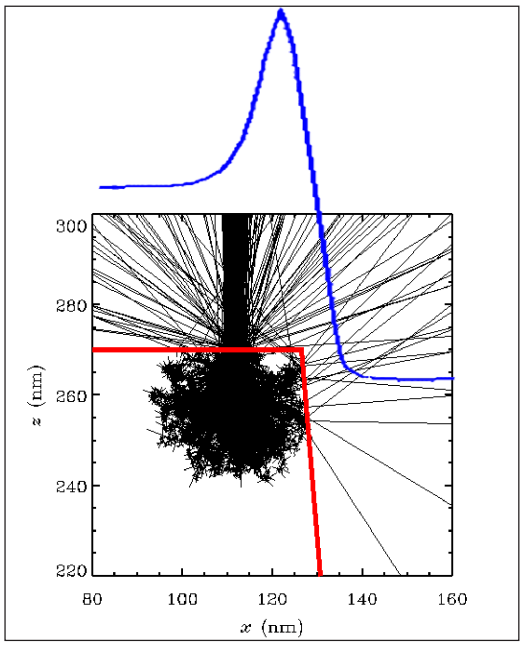

Figure 1. The SEM image may be calculated for a given edge geometry by using a Monte Carlo algorithm that follows a number of representative electron trajectories.

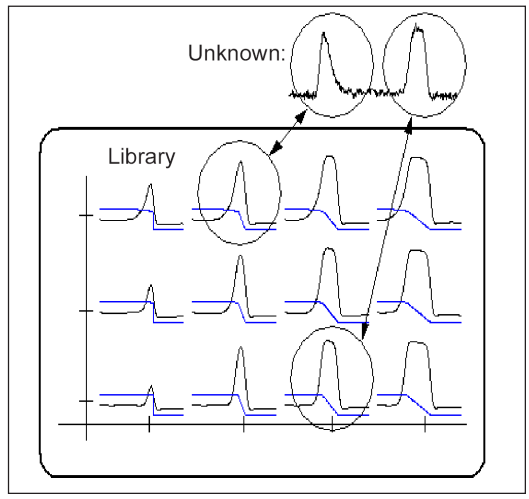

Figure 2. Concept of metrology using a model-based library. The measured left and right edges are compared to a library of images calculated for a range of possible edge shapes. The shape of the unknown structure that gave rise to the measured image is assigned to be the line shape corresponding to the image that most closely matches the measured one.

NIST is uniquely positioned to execute such a project. NIST is a center of expertise in the instrument models to be tested, with optical, SEM Monte Carlo, and SPM tip and sample reconstruction models all having been developed at NIST. Also, because NIST's standards function necessitates concern for accuracy, the NIST measurement tools are among the best characterized anywhere. For example, transmission optical measurements can be made here with the same instrument used to calibrate standard reference materials, and scale calibrations can be assisted by the NIST linescale interferometer.

We have been developing a model-based library method of determining line width and line shape from top-down SEM images. The top-down measurement configuration is the one employed by industry CD-SEMs. Edge locations tell us the line's width (the "CD" desired by industry). However, lines with different sidewall geometries appear to have different widths when measured using algorithms that are standard today on CD-SEMs. That is, sidewall variation masquerades as width variation. Accordingly, our method is a model-based algorithm that explicitly accounts for the physics of the interaction of the electron beam with the sample and the effect of sidewall geometry.

The method works like this: A set of parameters for describing edge geometry is chosen. These parameters might be, for example, sidewall angle and corner radius. For a given set of parameter values, the expected image is calculated using a Monte Carlo algorithm that simulates electron trajectories (Fig. 1). This calculation is repeated for other choices of edge parameters at discrete intervals representative of the range of shapes that one is likely to encounter in a measurement. The resulting actual shape / calculated image pairs form a library, or database. To determine the shape of an unknown sample, its measured image is compared to computed images in the database to find the closest match. The corresponding line shape is assigned to the unknown (Fig. 2). In practice there may be more than two parameters, and the library may be interpolated.

In 2002 we reported encouraging results for this method for polycrystalline Si (poly-Si) samples imaged in our laboratory SEM (Fig. 3a). We also established the level of agreement under the somewhat different imaging conditions in an industrial CD-SEM (Fig. 3b).

Measurements like these on poly-Si are industrially relevant after etch, and are also important as a prerequisite for the calibration of wafer linewidth standards. Such standards are likely to be fabricated in Si rather than resist because resist geometry is too unstable for a long-

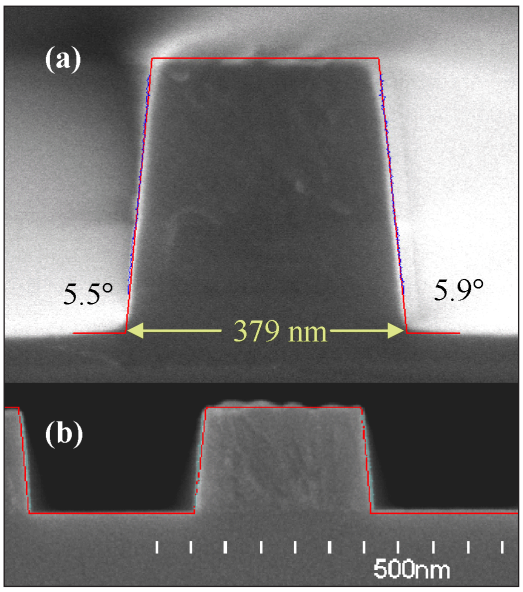

Figure. 3 Agreement between MBL and cross section measurement: (a) on NIST laboratory SEM (b) on commercial CD-SEM in a fabrication facility at International SEMATECH. The MBL results are red and the cross-section edge assignments blue.

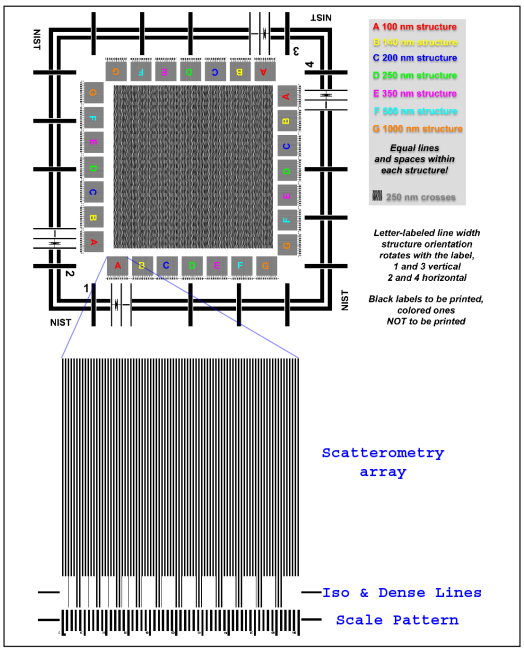

Figure 4. NIST 2090 SEM test pattern. The detail (shown at the bottom) consists of isolated and dense (1:1) nominally 100 nm lines suitable for measurement using a variety of tools.

term standard. However, a capability to measure resist would also be industrially useful for pre-etch process control measurements. The effects of contamination and charging when imaging non-conducting resists may result in poorer accuracy for resist samples than for Si samples. In 2003 we are investigating the applicability of MBL to resist measurements by performing MBL vs. cross-section comparisons on the resist test patterns shown in Fig. 4.

DELIVERABLES: Top-down model-based library analysis of resist lines will be compared to cross sections of those lines. The accuracy of the MBL method on such resist lines will be reported. 4Q 2003

The Fig. 4 pattern will also be fabricated in polysilicon for MBL vs. cross-section measurements in that material, for the purpose of establishing the suitability of MBL for calibrating wafer linewidth standards.

DELIVERABLES: A candidate linewidth standard (the NIST 2120 test pattern) will be measured using the MBL method and compared to cross section images. The suitability of MBL for calibrating a linewidth standard will be assessed and reported. 4Q 2003

Accomplishments

- A new linewidth test pattern (Fig. 4) was designed and included on an International SEMATECH mask.

- CD-SEMs differ from the laboratory SEM on which our initial measurements were performed in that they employ extraction fields intended to collect nearly all of the secondary electrons that escape a sample's surface. A capability to model full extraction (the CD-SEM case), no extraction (as in a laboratory SEM), or intermediate cases (as in a CD-SEM with low extraction field) was developed.

- We employed the new modeling capability to obtain linewidth and line shape information from top-down CD-SEM images acquired with a commercial CD-SEM under typical industrial measurement conditions. We compared these results to cross-sectional images of the same lines (Fig. 3b).

- We used the modeling capability to conduct an industry-requested study of repeatability and bias in the CD-SEM. The results indicated that measurement repeatability is most strongly affected by noise level, electron beam size, sample sidewall angle, and choice of measurement algorithm. The results also indicate that sample-dependent measurement bias is likely to contribute a significant component of measurement resolution—a component unmeasured with current industry tests of instrument precision. Results were reported to International

SEMATECH and at the SPIE Microlithography meeting.

- MBL software was installed on a computer at International SEMATECH. Software to construct libraries was distributed to interested CD-SEM manufacturers.

- We reported our progress in developing this measurement method to International SEMATECH. We reported also to the semiconductor metrology community and public generally via oral presentation at the SPIE Micrometrology Symposium and publication in the symposium proceedings.

Collaborations

International SEMATECH, Benjamin Bunday, Michael Bishop and Applied Materials, John Swyers: CD-SEM data acquisition.

International SEMATECH, Benjamin Bunday and Michael Bishop: linewidth test pattern sample fabrication.

Recent Publications

"Scanning electron microscope analog of scatterometry," J. S. Villarrubia, A. E. Vladár, J. R. Lowney, and M. T. Postek, *Proc. SPIE* **4689**, pp. 304-312 (2002).

"Test of CD-SEM Shape-Sensitive Linewidth Measurement," J. S. Villarrubia, A. E. Vladár, and M. T. Postek, final report to International SEMATECH, January 2003, available to member companies at SEMATECH web site.

"Exploring and Extending the Limits of SEMs' Resolution," A. E. Vladár, J. S. Villarrubia, and M. T. Postek, final report to International SEMATECH, November 2002, available to member companies at SEMATECH web site.

"A Simulation Study of Repeatability and Bias in the CD-SEM," J. S. Villarrubia, A. E. Vladár, and M. T. Postek, Proc. SPIE **5038**, 2003, in press.

"Tip Characterization for Dimensional Nanometrology," J. S. Villarrubia, in *Applied Scanning Probe Methods,* eds. B. Bhushan, H. Fuchs, and S. Hosaka (Springer Verlag) 2003, in press.

Thin Film and Shallow Junction Metrology Program

The dimensions of the active transistor areas are approaching the spacing between dopant atoms, the stochastic regime, complicating both modeling and doping gradient measurements. Thin dielectric and conducting films are approaching monolayer thicknesses.

As device dimensions continue to shrink, junctions and critical film thicknesses approach the realm of several atoms thick, challenging gradient, thickness and roughness metrology as well as electrical and reliability characteristics. The gate dielectric, traditionally SiO_2, has been replaced with silicon oxynitrides, and more advanced high dielectric constant materials are being actively explored.. The overall task is to provide suitable metrology and reference materials for thin dielectrics and conducting barrier films, including electrical characterization, gradient, thickness and roughness metrology and overall reliability metrology.

Two- and Three-Dimensional Dopant Profiling

Goals

To provide industry with the metrology infrastructure needed to measure two- and three-dimensional dopant/carrier profiles in the ultra-shallow junction regime. The project is divided into two thrusts (SIMS and SCM):

1) Improve the capabilities for compositional depth-profiling by defining optimum procedures for ultra-high depth resolution by Secondary Ion Mass Spectrometry (SIMS), developing depth-profiling reference materials needed by the semiconductor industry, and improving the uncertainty of implant dose measurements by SIMS.

2) Provide measurement methodologies, theoretical models, and data interpretation software necessary to make the Scanning Capacitance Microscope (SCM) a useful two-dimensional dopant-profiling tool.

Customer Needs

Since source/drain dopant profiles are a critical factor determining the performance of a transistor, dopant profiling has always been needed by the silicon integrated circuit industry. One-dimensional dopant profiles from SIMS or electrical techniques remain an important process control tool. As transistors are scaled to ever-smaller dimensions, the variation of dopant profiles in two- and three-dimensions also begin to influence device operation. Two- and three-dimensional dopant profiles are now needed to validate models of the processes used to produce ultra-shallow junctions and for accurate device simulations.

SIMS is most likely to provide the solution to precision requirements for 1-D dopant concentration measurements. These goals can be achieved by careful control of SIMS depth-profiling conditions and by developing and making available implant reference materials for common dopant elements. Scanning Capacitance Microscopy (SCM) has emerged as a leading contender to provide two-dimensional carrier profiles. Relatively accurate 2-D profiles of the dopant concentration can be obtained when SCM images are combined with SIMS measurements.

Metrology needs for Doping Technology are discussed in the 2002 Update of The International Technology Roadmap for Semiconductors. The ITRS requirements are for 2-D dopant profile concentration measurements improving from a spatial resolution of 2 nm and precision of 4 % in 2003 to 1 nm and 2 % by 2016. Complete specifications are given for the short term in Table 100a on page 139 and for the long term in Table 100b on page 140 of the Metrology section. Three-dimensional dopant profiling is identified as one of five difficult challenges < 65 nm beyond 2007, in Table 96 on page 134. Requirements for reference materials and the NIST role are discussed on pp. 23-24 of the 2001 ITRS, with a specific reference to dopant profiling. Additional discussion about dopant profile fabrication and measurement needs can be found in the Front End Processes and Modeling and Simulation sections.

Technical Strategy

1. Secondary ion mass spectrometry (SIMS) has demonstrated the capability to meet the ITRS dopant profiling requirements for B, As, and P. However, the detailed analytical protocols required to achieve these goals have not been completely specified. We are working in a collaboration with Agere Systems to investigate the parameters that must be controlled to make highly repeatable dose measurements of As and P implants in Si with magnetic sector SIMS instruments. In addition to improved repeatability for dopants, the ITRS roadmap also requires increased SIMS detection limits for trace metal contamination analysis of semiconductor devices. We are also working on novel methods to enhance detection limits for common metal contaminants by increasing the ionization efficiency during the SIMS sputtering process.

DELIVERABLES: Develop experimental protocols for high repeatability analysis of As and P implants in silicon. Develop methods for improving the detection sensitivity of trace metals by SIMS. 3Q 2002

2. Shrinking semiconductor device dimensions require increased depth resolution for depth profiling analysis. Typically, the highest depth resolution is achieved by using ultra-low energy primary ion bombardment. However, this capability is not available on most commercial SIMS instruments. In instruments where low energy analysis is available, slow sample erosion rates can result in prohibitively long analysis times. We are exploring an alternate approach that involves using a high energy, focused ion

Technical Contact:
Greg Gillen (SIMS)
David Simons (SIMS)
Joseph Kopanski (SCM)
Jay Marchiando (SCM)

"SIMS is still a recognized champion in dopant characterization. However, profiling of active dopant components is a must for good work on dopant characterization today. A progress in "conventional" 2-D dopant characterization techniques such as scanning capacitance microscopy (SCM) and scanning spreading resistance microscopy (SSRM) took many by surprise. SCM and SSRM on beveled cross sections promise ITRS desired nanometer and beyond spatial resolution for 2-D dopant profiling. Significant progress (has been) made in SCM and SSRM data interpretation."

Vladimir Ukraintsev,
Texas Instruments

beam to rapidly mill a beveled cross-section in the sample under examination. The "altered layer" produced by the high energy milling beam can be removed by subsequent bombardment in a special gaseous cluster ion beam sputtering instrument. The cross section prepared in this fashion is then analyzed using high resolution imaging Auger and SIMS analysis.

DELIVERABLES: Develop new 2-D image depth profiling technique for high depth resolution SIMS and Auger depth profiling. 4Q 2003

3. Some thin-film materials such as metals do not sputter as uniformly as silicon under ion bombardment. The initial surface topography of the metal surface or topography induced by the sputtering process itself often limits the achievable depth resolution. We are exploring a mechanical thinning method that will allow SIMS depth profiling from the backside silicon through the interface with the top layer. This will allow subtle diffusion effects to be distinguished and will eliminate degradation in depth resolution from surface or sputter-induced topography. This method relies on a commercial polishing system that allows precise adjustment of the parallelism between the sample surface and the platen containing the polishing material. Silicon is removed by mechanical grinding using a series of diamond lapping films of decreasing abrasive size. This approach is being applied to the depth profiling analysis of blanket films (copper metallization on silicon) as well as PMOS patterned wafers in collaboration with International SEMATECH.

DELIVERABLES: Develop sample preparation for SIMS Backside SIMS Depth Profiling. 4Q 2003

4. Cluster primary ion beam SIMS offers several advantages for the analysis of semiconductor materials. Compared to conventional SIMS analysis using monoatomic primary ions, cluster bombardment SIMS offers improvements in depth resolution (Fig. 1), higher sputter rates, and increased sensitivity for some elemental species. Also, greater sensitivity for organic species may greatly increase our ability to detect organic contamination on silicon surfaces. We are exploring various applications of this technique and attempting to develop new, low cost cluster ion beam sources to promote more widespread use of the technique.

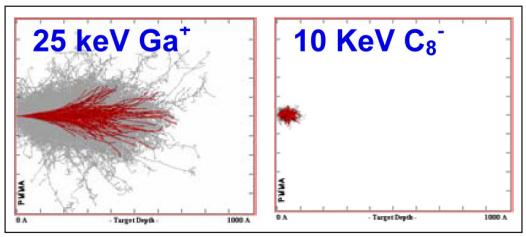

Figure 1. Computer simulation of subsurface damage created by a 25 keV Ga^+ ion compared to a cluster projectile. Target is a photoresist.

DELIVERABLES: Continue development of cluster SIMS technique for depth profiling of semiconductors. 4Q 2003

5. Development of ion implanted reference materials for the semiconductor industry has been given a high priority by the International SEMATECH Analytical Lab Managers Working group. Previous ion implant NIST standards include B in silicon (SRM 2137) and As in silicon (SRM 2134), which was released in FY 2000. Current efforts are focused on development of a P ion implant standard in silicon.

DELIVERABLES: Development of ion implant reference materials. 1Q 2003

The Scanning-Probe Microscope Metrology part of the project is developing tools that are intended to enable scanning capacitance microscopes to function as two-dimensional dopant profiling tools. This work is divided into three tasks. Task 1 is to develop SCM measurement methodologies. Best measurement practices are being determined via collaborative projects with industrial users and research into the physics of the silicon surface preparation. Task 2 is to develop theoretical models of the SCM. The focus of our modeling effort has been to develop 2-D and 3-D finite-element solutions of Poisson's equation for the SCM geometry. Task 3 is interpretation of SCM data and technology transfer. Our expertise with interpreting SCM images is being transferred to industry through our software program *FASTC2D*. The program features an easy to use interface, rapid profile extraction, and operation in a Windows environment.

6. Currently, the spatial resolution of 2-D dopant profiles measured with SCM is limited by the tip size and by the data interpretation techniques. One way to overcome the tip size limitation may be to bevel the sample on a cross-section, producing magnification both in depth and laterally. We have begun to investigate SCM measurements on beveled samples. While it is

straightforward to produce a beveled cross-section, carrier redistribution may raise new interpretation issues.

The version of *FASTC2D* currently available utilizes a calibration curve, determined from a database of pre-calculated solutions, which can very rapidly determine a 2-D carrier profile from an SCM image. When used in conjunction with SIMS measurements or a reference sample, relatively accurate profiles can be obtained, see Fig. 2. We have produced a series of tutorial samples, Fig. 3, that are intended to be used with *FASTC2D* to teach best measurement and data interpretation procedures.

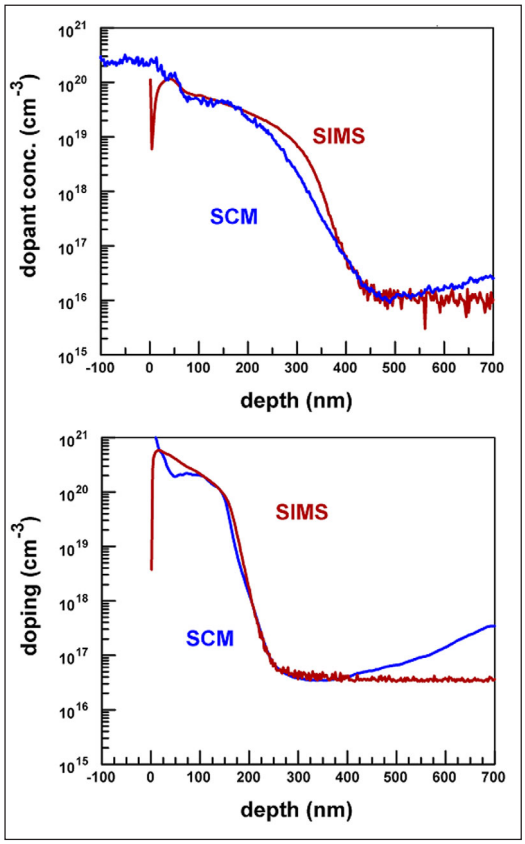

Figure 2. SIMS and SCM depth profiles of boron in the P+ region of a test pad on the SCM tutorial sample (top). SIMS and SCM depth profiles of arsenic in the N+ region of a test pad on the SCM tutorial sample (bottom).

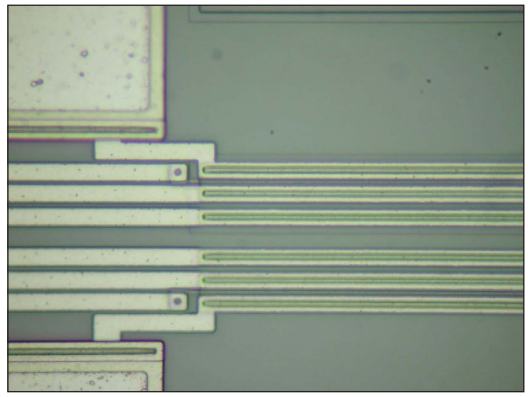

Figure 3. Prototype tutorial sample for SCM. Extended length transistor-like devices for easy cross sectioning, containing structures both with and without p-n junctions.

DELIVERABLES: Improve spatial resolution of SCM measured dopant profiles by developing techniques to produce precisely beveled samples and techniques for their interpretation. 4Q 2003

7. A physically accurate 3-D model and determination of the dopant profile by an inverse solution are required to meet industrial needs for 2-D dopant profiling to the end of the ITRS. We have previously developed a quasi-3-D model of the SCM that predicts the essential behavior of the SCM measurement. However, for the required dopant profiling performance goals, a more rigorous approach is necessary. Towards this end, the finite element method has been employed to solve Poisson's Equation for the SCM geometry in three-dimensions. Accuracy requirements may also force the consideration of quantum mechanical effects, necessitating the solution of the coupled Poisson and Schrödinger Equations. We are developing improved 3-D Poisson solvers using the LaGriT grid management toolbox in collaboration with Los Alamos National Laboratories.

DELIVERABLES: Demonstrate optimized 3-D calculations of the SCM signal across dopant gradients and junctions. 2Q 2004

8. An inverse solution of the SCM requires repeated solutions of the forward problem; i.e., calculation of the SCM signal from candidate carrier profiles. The candidate active dopant profile is adjusted until a dopant profile is found that yields a calculated SCM signal that agrees with the measured SCM signal. Project staff have developed a regression procedure, in Fig. 4, to do this with a 2-D solver. The final level of refinement is to use the full 3-D model as the basis of inverse solutions of the SCM. However, the

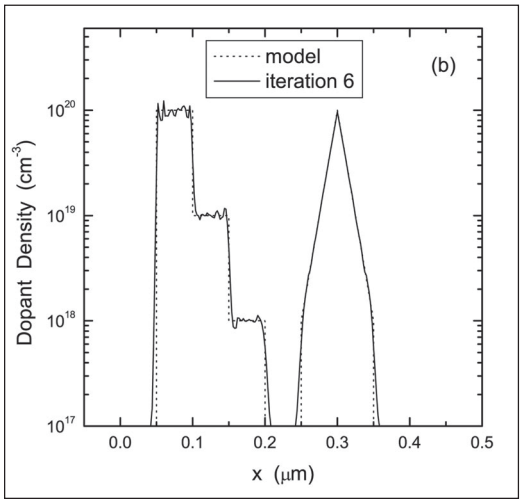

Figure 4. SCM regression solution matched to theoretical dopant profile. Regression solutions provided enhanced spatial resolution and accuracy over calibration curve methods.

volume of data to be processed and the time required for calculation makes this intractable for routine profile extraction. Practical application requires finding shortcuts that will achieve the 3-D result without having to complete the entire round of 3-D simulations.

DELIVERABLES: Make available to users a computationally efficient method of determining carrier profiles from SCM images using inverse solutions based on 3-D models. Q4, 2005.

Accomplishments

■ **High Repeatability SIMS Measurements** – We collaborated with Agere Systems to investigate the parameters that must be controlled to make highly repeatable dose measurements of As and P implants in Si with magnetic sector SIMS instruments. With optimized settings, we demonstrated the ability to distinguish As or P implant doses differing by 5 % with an RSD of less than 0.5 % in favorable cases. As the level of required precision for SIMS dopant concentration measurements continues to increase, consideration must also be given to more subtle effects that may affect the measurement. In particular, the behavior of the secondary ion detection system (electron multiplier) may become a significant factor. Typically, the detector settings used in routine analyses are those set by the tool manufacturer. However, these are not always optimal for high precision measurements. We have found that the detection sensitivity for elements such as Si and B can change by a factor of 2 depending on the energy of the detected secondary ion and the settings of the detection system. We have developed a system at NIST that allows for reproducible detector setup and optimization. We hope this may allow us to achieve even higher levels of precision for dopant concentration measurements.

■ **Enhanced Detection Limits for Trace Elements** – Secondary ion signals in SIMS are strongly dependent on the local chemistry of the sample. Oxygen gas backfilling of the analytical chamber is often used to enhance positive secondary ion yields for many metals of interest in semiconductor metrology. In some cases, the use of halogen containing gases, rather than oxygen, may lead to further sensitivity enhancements. To address this issue, pure metal and ion implant standards have been examined using freon gas backfilling of the sample chamber. Preliminary data suggests that Cu and Zn are less enhanced under freon exposure as compared with oxygen. The ion yields for Al, Ti, Fe, and Ni are similar under freon and oxygen, but the ion yields for V, Cr, Mn, Zr, Nb, Mo, Ag, and under freon enhancement is several times higher than that of oxygen. The sputtering rate under freon flooding is about 2.5 times greater than oxygen flooding under similar sputtering conditions.

■ **Bevel Image Depth Profiling** – The NIST magnetic sector SIMS instrument has been modified to create custom ion-milled bevel cross sections in multilayer test structures, Fig. 5, using 19.5 keV O_2^+ bombardment. The use of an oxygen primary ion beam was found to minimize sputter rate variations between layers and to

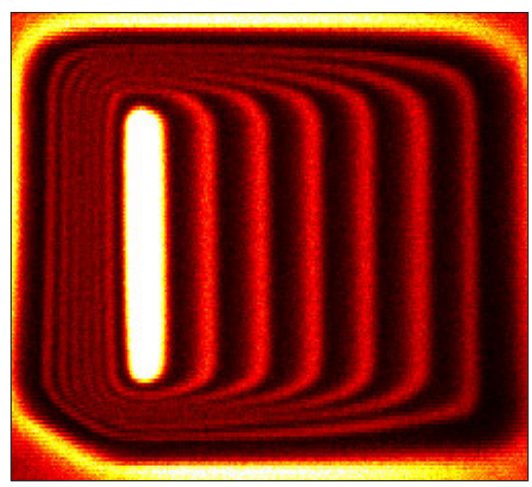

Figure 5. SIMS Image of SiO_2^- secondary ion signals from a bevel cross-section cut into a depth profiling reference material of alternating SiO_2 delta layers in Ta_2O_5.

reduce sputter-induced topography. Subsequent removal of the implanted oxygen and subsurface mixed zone is accomplished using low energy Ar^+ bombardment or a gaseous cluster ion beam sputter system. This approach may provide a means to produce depth profiles that have higher depth resolution than is possible using conventional SIMS analysis using higher energy primary ion beams.

■ **Standard Reference Material Ion Implant Development** – A new ion implant reference material for phosphorus has been developed and is now available as Standard Reference Material 2133 a phosphorus Implant in Silicon Depth Profile Standard for SIMS calibration. SRM 2133 is a 1 cm x 1 cm piece of silicon containing a 100 keV implant of P-31 with a certified dose of 9.58E14 atoms/sq cm with an expanded uncertainty (95 % confidence interval) of +/- 1.7 %. It was certified by radiochemical neutron activation analysis that was calibrated with phosphorus reference solutions. Other ion-implanted SRMs are also available from NIST as SIMS calibration standards. SRM 2134 is a 100 keV arsenic implant in silicon with a certified dose of 7.33E14 atoms/sq cm and expanded uncertainty of 0.38 %, and SRM 2137 is a 50 keV boron-10 implant in silicon with a certified dose of 1.018E15 atoms/sq cm and expanded uncertainty of 3.4 %.

■ **Polyatomic Primary Ion Beam SIMS** – Studies of polyatomic primary ion beam sources for high depth resolution SIMS dopant profiling are continuing. Collaborations with international SEMATECH have focused on depth profiling of novel ZrO_2 films, Fig. 6, on both magnetic sector and TOF-SIMS instruments. A new polyatomic ion source has been designed and constructed that features an externally removable reaction chamber that will allow for use either as a standard duoplasmatron or as an SF_5^+ source. A special lens system was ordered that would allow higher cluster ion currents to be extracted from the source.

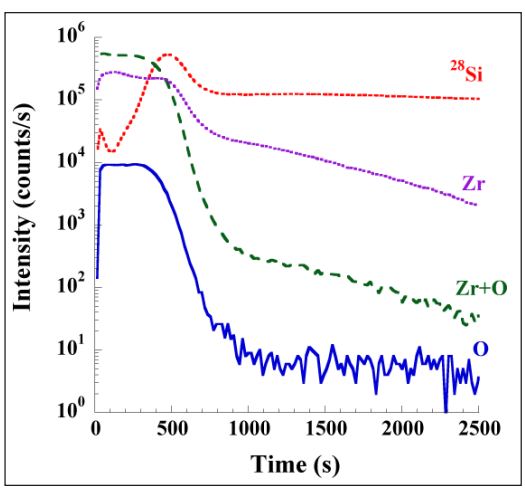

Figure 6. SIMS depth profile of ZrO_2 oxide layer (6 nm thickness) with SF_5^+ depth profiling.

■ **Developed a set of tutorial samples** – for 2-D dopant profiling with the SCM. These samples have large source/drain (S/D) spacing (1.5 µm), so that any user of SCM should be able to easily image them and extract 2-D dopant profiles from the image using the *FASTC2D* software. The sample contains four types of transistors-like structures: the usual CMOS pair (n+ S/D regions in p-substrate and p+ S/D in a n-well) and a pair with the type of the source/drain reversed (that is, p+ S/D in the p-substrate and n+ S/D in the n-well). These samples are to be used in a tutorial with the *FASTC2D* software to teach users how to acquire SCM data suitable for extraction of quantitative dopant profiles and proper use of the *FASTC2D* software, Fig. 7.

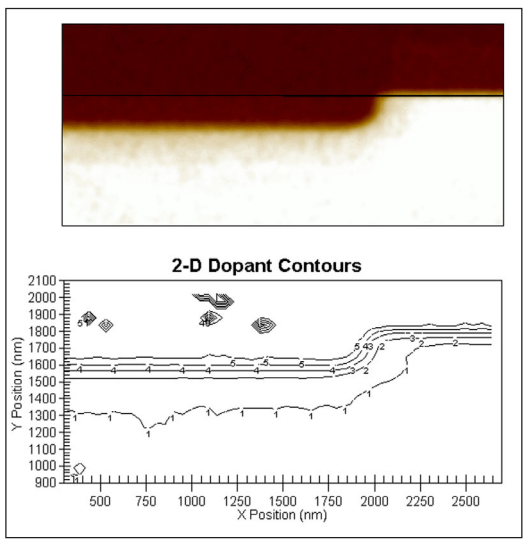

Figure 7. Typical SCM image and extracted 2-D dopant contours for Boron (p-type) implant tutorial sample.

■ **Progress in development of SCM 3-D regression solutions** – Developed a methodology for calculating the SCM signal by using the oxide-capacitance distribution to specify a natural boundary condition along the probed surface of the semiconductor sample, so that only the semiconductor substrate region needs to be discretized. This approach may lead to an increase in the speed for which 3-D solutions can be obtained.

■ **Developed techniques to optically pump scanning probe microscopes –** Dr. Gyoung-Ho Buh, guest researcher from the University of Seoul, Korea has developed techniques to optically pump scanning probe microscopes. The technique encompasses a GUI interface written in Visual C++ to control a laser, lock-in amplifier, and digital oscilloscope to measure optically induced capacitance transients. Carrier lifetime can be deduced from the capacitance transient in response to a change in illumination. Publications and a patent application are pending.

■ **Implemented advanced MOS models in *FASTC2D* –** Implemented new routines to calculate the SCM capacitance-voltage curve database using Fermi-Dirac statistics and either a classical and quantum mechanical model. This is the first implementation of a quantum mechanical correction to the C-V response for SCM data interpretation. Since SCM usually uses a very thin oxide this is an important extension to previous practice.

■ **Developed software to simulate the dopant profile exposed on a beveled cross-section –** The *BASSAR* (for Bevel and Section Simulation and Reconstruction) software can: 1) simulate 2-D profiles from input model parameters, 2) predict profiles that would be exposed at specified cross-sectioning and bevel angles, and 3) recover the normal profile (to 0th order) from an input profile measured on a beveled cross-section.

■ **Completed study on factors influencing the reproducibility of SCM measurements –** The effects of stray light from the AFM laser and stray capacitance from sample geometry have been quantified. Chi Tran, guest researcher from the University of California, Berkley and Dr. Buh conducted PSPICE simulations of an RCA style capacitance sensor confirming several previously unverified assumptions about the behavior of the SCM.

Collaborations

AMD – Metal film depth-profiling by SIMS.

Atolytics Inc, Paul Weiss – Phase II SBIR to develop a commercial version of their scanning microwave microscope.

FM Technologies – High brightness oxygen source for 2D dopant profiling by SIMS.

Imago Scientific Instruments Corporation, Madison, WI, Tom Kelly, Evaluation of position sensitive atom probe.

International SEMATECH, Joe Bennett – Thin oxide depth-profiling by SIMS.

Los Alamos National Laboratory, Denise George and Andrew Kuprat – Development of next generation 3-D Poisson simulators using the LaGrit grid management toolbox.

Manufacturing Instrumentation Consultant Co – Phase II SBIR to develop co-axial shielded scanning probe microscope tips.

North Carolina State University, Fred Stevie – Dose repeatability of SIMS measurements.

Peabody Scientific – Ion source development for SIMS.

Samsung Electronics Co., Gyoung Ho Buh – Characterization of ultra-shallow junctions and optically pumped SPM measurements.

University of Queensland, Brisbane, Australia, Tong Yeow – A PhD student will be a guest researcher at NIST summer 2003 to take data with the SCM and learn about our modeling effort.

Recent Publications

G. Gillen, S. Wight, P. Chi, A. Fahey, J. Verkouteren, E. Windsor and D. B. Fenner, "Bevel Depth Profiling SIMS for Analysis of Layered Structures," in Characterization and Metrology for ULSI Technology 2003, D.G. Seiler et al., eds., AIP Press, Accepted for publication 2003.

N. Jin, S.-Y. Chung, A. T. Rice, P. R. Berger, P. E. Thompson, C. Rivas, R. Lake, S. Sudirgo, J. J. Kempisty, B. Curanovic, S. L. Rommel, K. D. Hirschman, S. K. Kurinec, P. H. Chi, and D. S. Simons "Diffusion Barrier Cladding in Si/SiGe Resonant Interband Tunneling Diodes And Their Patterned Growth on PMOS Source/Drain Regions," Accepted for publication in special issue on Transient Enhanced Diffusion, J. Appl. Phys. (2003).

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J. F. Marchiando and J. J. Kopanski, "Regression procedure for determining the dopant profile in semiconductors from scanning capacitance microscopy data," J. Appl. Phys. **92**, 5798-5809 (2002).

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G. Gillen, S. Roberson, A. Fahey, M. Walker, J. Bennett and R. T. Lareau, "Cluster Primary Ion Beam Secondary Ion Mass Spectrometry for Semiconductor Characterization," in Characterization and Metrology for ULSI Technology, D. G. Seiler et al., eds., AIP Press, pp. 687-691 (2001).

D. E. McBride, J. J. Kopanski, and B. J. Belzer, "Gate Oxide Formation Under Mild Conditions for Scanning Capacitance Microscopy," in Characterization and Metrology for ULSI Technology, D. G. Seiler et al., eds., A.I.P Press, pp. 657-661 (2001).

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B. G. Rennex, J. J. Kopanski, and J. F. Marchiando, "*FASTC2D*: Software for Extracting 2D Carrier Profiles from Scanning Capacitance Microscopy Images," in Characterization and Metrology for ULSI Technology, D. G. Seiler et al., eds., A.I.P Press, pp. 635-640 (2001).

E.R. Fuoco, G. Gillen, M. B. J. Wijesundara, B. Wallace, and L. Hanley, "Surface analysis studies of yield enhancements in secondary ion mass spectrometry by polyatomic projectiles," J Phys. Chem **B 105**(18), 3950-3956 (May 10 2001).

G. Gillen. L. King, B. Freibaum, et al., "Negative cesium sputter ion source for generating cluster primary ion beams for secondary ion mass spectrometry analysis," J. Vac. Sci. Technol. **A 19**(2), 568-575 (Mar-Apr 2001).

K. D. Hobart, P. E. Thompson, S. L. Rommel, T. E. Dillon, P. R. Berger, D. S. Simons, and P. H. Chi, "p-on-n Si interband tunnel diode grown by molecular beam epitaxy," J. Vac. Sci. Technol. **B 19**(1), 290-293 (Jan-Feb 2001).

Recent Talks

J. J. Kopanski, "Two-Dimensional Dopant Profiling of Semiconductors using the Scanning Capacitance Microscope," E. O. Lawrence Berkeley Laboratory Seminar, Berkeley, CA, May 2, 2003. (INVITED)

G. H. Buh, C. Tran, and J. J. Kopanski, "PSPICE analysis of a scanning capacitance microscope sensor," 7th Intl. Workshop on Fabrication, Characterization, and Modeling of Ultra-Shallow Doping Profiles in Semiconductors, Santa Cruz, CA, April 29, 2003.

J. J. Kopanski, J. F. Marchiando, B. G. Rennex, D. Simons, and Q. Chau, "Towards reproducible SCM image interpretation," 7th Intl. Workshop on Fabrication, Characterization, and Modeling of Ultra-Shallow Doping Profiles in Semiconductors, Santa Cruz, CA, April 29, 2003.

J. F. Marchiando and J. J. Kopanski, "On calculating the dopant profile in semiconductors from scanning capacitance microscopy data," 7th Intl. Workshop on Fabrication, Characterization, and Modeling of Ultra-Shallow Doping Profiles in Semiconductors, Santa Cruz, CA, April 29, 2003.

G. Gillen, S. Wight, P. Chi, A. Fahey, J. Verkouteren, E. Windsor and D.B. Fenner, "Bevel Depth Profiling SIMS for Analysis of Layered Structures," in Characterization and Meterology for ULSI Technology 2003 Conference, Austin, TX, April, 2003.

J. J. Kopanski, "Scanning Probe Microscopes for the Electrical Characterization of Semiconductors," March 2003 Meeting of the American Physical Society, Austin, TX, March 4, 2003. (INVITED)

M. Matarazzo and J. J. Kopanski, "High Spatial Resolution Automatic Resistivity Mapping of Semiconductors," March 2003 Meeting of the American Physical Society, Austin, TX, March 4, 2003.

J. J. Kopanski, "Update on NIST's 2D dopant profiling project," SEMATECH Analytical Lab Mangers Working Group on Two-Dimensional Dopant Profiling, San Jose, CA, Dec. 13, 2002.

S. Wight, G. Gillen, P. Chi, A. Fahey, A. Roshko, K. Bertness, "Bevel Crater SIMS for Auger Analysis of Laterally Oxidized AlGaAs/GaAs Multilayers," American Vacuum Society 49th International Symposium, Denver Colorado, Nov. 5, 2002.

D. Simons, E. Steel, R. Marinenko, J. Armstrong, S. Turner, J. McKinley and F. Stevie, "Si-Ge Interactive Reference Materials," 15th Annual SIMS Workshop, Clearwater, FL, May 1, 2002.

G. Gillen, A. Fahey and S. Wight, "Bevel Depth Profiling SIMS of Oxidized AlGaAs Superlattice Samples," 15th Annual SIMS Workshop, Clearwater, FL, May 1, 2002.

P. Chi and G. Gillen, "Preliminary Evaluation of Positive Secondary Ion Yield Enhancements Using Chlorodifluoromethane Backfilling," 15th Annual SIMS Workshop, Clearwater, FL, May 1, 2002.

D. Simons, "Development of a Phosphorus-Implant-in-Silicon Calibration Standard for SIMS," 13th International Conference on Secondary Ion Mass Spectrometry, Nara, Japan, November 13, 2001.

D. Simons, "Reference Materials for SIMS: Philosophy, Development, and Results," AVS 48th International Symposium and IUVSTA 15th International Vacuum Congress, San Francisco, CA, October 30, 2001. (INVITED)

D. Simons, "Reference Materials for SIMS - What We Have Now and What We Need," 14th Annual SIMS Workshop, Scottsdale, AZ, May 14, 2001.

A. Fahey and G. Gillen, "Characterization of Electron Multiplier Post Acceleration using Pulse Height Distributions," 14th Annual SIMS Workshop, Scottsdale, AZ, May 14, 2001.

P. Chi, "Roughness Reduction on Depth Profiling of Cu Films with Sample Rotation," 14th Annual SIMS Workshop, Scottsdale, AZ, May 14, 2001.

J. Kopanski, "Comparison of Experimental and Theoretical Scanning Capacitance Microscope Signals and Their Impact on the Accuracy of Determined Two-Dimensional Carrier Profiles," Sixth International Workshop on the Fabrication, Characterization and Modeling of Ultra Shallow Doping Profiles in Semiconductors," Napa, CA, April 22-26, 2001.

G. Gillen, "Secondary Ion Mass Spectrometry Using Cluster Ion Beams," National Security Agency and University of Maryland, April 4, 2001. (INVITED)

G. Gillen, "SIMS Depth Profiling with Cluster Primary Ion Beams," Surface Analysis 2001 Meeting, Orlando, FL, March 12-14, 2001.

G. Gillen, "Surface Analysis with Energetic Cluster Ion Beams," PITTCON, New Orleans, LA, March 5, 2001.

Gate Dielectric Metrology

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N. Nguyen
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Goals

Develop new and improved optical and electrical measurements, models, data and reference materials to enable better and more accurate measurements of select, critical, thin film parameters for silicon CMOS technology. Major focus is placed on high-k materials for the gate dielectric. Additional work is being done on films and layers for silicon-on-insulator and strained silicon-germanium layer upgrades of CMOS device fabrication.

To address needs in composition and thickness measurements for thin films and interfaces including high- and low-k materials from gate dielectrics to polymers. This project develops new methods and standards as well as characterizes the accuracy and reliability of existing methods using analytical electron, x-ray, and laser probes. This year the project has five main components:

- Apply spectroscopic ellipsometry characterization to novel high-k dielectric materials and correlate results with measurements from Grazing Incidence X-ray Photoelectron Spectroscopy (GIXPS), High Resolution Transmission Electron Microscopy (HRTEM), X-Ray Absorption Fine Structure (EXAFS), and Electron Energy Loss Spectroscopy (EELS).
- Develop GIXPS for the measurement of silicon oxide and oxynitride films and determining the uncertainty of this method.
- Characterize the accuracy of HRTEM for thickness measurements of ultra-thin gate dielectrics.
- Apply extended EXAFS and EELS to characterize compositional homogeneity and local-scale structure in ultrathin (< 10 nm) dielectric films.
- To provide electrical and reliability measurement techniques, data, physical models, and fundamental understanding for ultra-thin silicon dioxide and alternate gate dielectrics in future MOS devices. To increase the understanding of the relationship between the gate dielectric material/interface properties and device electrical and reliability measurements.

Test wafer being loaded on wafer prober for long-term dielectric testing.

Customer Needs

The evolving decrease of the gate dielectric film thickness to an oxide-equivalent value of 2 nm is identified as a critical front-end technology issue in the ITRS with effective thickness values of 1.4 nm, or less, being projected in 2004, dropping to 0.8 nm or less by 2010. For effective gate dielectric thicknesses below ~ 2.0 nm, SiO_2 is being replaced, initially by oxynitrides or oxide/nitride stacks, and then by either metal-oxides or compounds such as metal-silicates or metal silicates. Process control tolerance needs for dielectric thickness are projected as ±4 % (3 σs), which translates to less than 0.1 nm for 2 nm films. Requirements for process control measurements are a factor of ten smaller still.

Spectroscopic ellipsometry (SE) is expected to continue as a preferred measurement for process monitoring of future gate dielectric films. IC fabrication metrology needs not only improved methods to determine film thickness accurately, but also: (1) techniques to determine the structure of the individual films and the interfaces between them; (2) an improved understanding of the relationship between physical, electrical, and optical determinations of film properties; and (3) mechanisms, for enabling traceability of measurements to NIST.

In order for SE to meet process control requirements of film thickness and the determination of film composition and morphology, the optical properties of these advanced dielectric film systems must be characterized and understood.

The microelectronics industry has a high demand for reliable thin film measurement methods that

yield composition and dimension information with known accuracy and precision.The metrology section of the ITRS 1999 metrology section clearly states the needs for "reference materials and standard measurement method-ology for new, high-k gate and capacitor dielec-trics with interface layers, thin films such as interconnect barrier and low-k dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. The same is true for measurement of barrier layers."

As semiconductor processing and devices move to smaller dimensions and new materials, the characterization of the device thin film thickness, composition, and interface quality become ever more critical to device operation and reliability.

The ITRS indicates that the equivalent thickness of the gate dielectric will need to be 1.0 nm to 1.5 nm by 2004. Due to increased power consumption, intrinsic device reliability and circuit instabilities associated with SiO_2 of this thickness, a high permitivity gate dielectric (e.g., Si_3N_4, $HfSi_xO_y$, ZrO_2) with low leakage current and at least equivalent capacitance, performance, and reliability will be required. The physics of failure and traditional reliability testing techniques must be reexamined for ultra-thin gate oxides that exhibit excessive tunneling currents and soft breakdown. Electrical characterization of Metal Oxide Semiconductor (MOS) capacitors and Field Effect Transistors (FET) has historically been used to determine device and gate dielectric properties such as insulator thickness, defect densities, mobility, substrate doping, bandgap, and reliability. Electrical and reliability characterization methodologies need to be developed and enhanced to address issues associated with both ultra-thin SiO_2 and alternate dielectrics including large leakage currents, quantum effects, and thickness dependent properties. As compared to SiO_2, very little is known about the physical or electrical properties of high dielectric constant gate dielectrics in MOS devices. The use of these films in CMOS technology requires a fundamental understanding of the relationship between the gate dielectric material/interface and device electrical and reliability measurements. *"The 2001 ITRS identifies the gate dielectric as being one of the most difficult challenges for future device scaling," p. 19 of the Front End Processes Section.*

Technical Strategy

This project focuses on the issues of: (1) identifying structural models and developing preferred optical index dispersion functions or data for improved ellipsometric analysis of future-generation gate dielectric film systems; (2) correlating optical, electrical, and physical measurements of thickness, composition, and interface structure; and (3) developing and providing the basis for traceability to NIST for film measurements, particularly for thickness.

Structural and optical models for ellipsometry

A custom-built, high-accuracy spectroscopic ellipsometer, Fig. 1, with a spectral range of 1.5 eV 6.2 eV and a commercial VUV ellipsometer which extends the measurement range to 9.5 eV, are being used for this task. Project staff are working with International SEMATECH, IC industry companies, and SRC university staff to obtain and optically characterize advanced oxynitrides, oxide/nitride stacks, and metal-oxide, and more complex compounds such as hafnium silicon oxynitride and hafnium-aluminum silicate, Fig. 2.

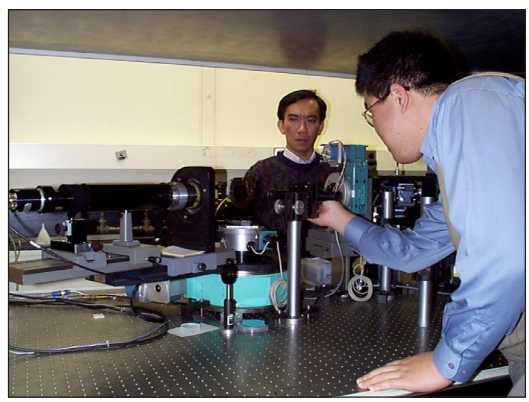

Figure 1. Researchers align sample on custom-built high-accuracy spectroscopic ellipsometer.

Since many of these materials have optical bandgaps just below 6 eV, the additional measurement range obtainable with the VUV ellipsometer enables the investigation of important processing related structure in the index of refraction (dielectric constant) of these materials which shows up in the absorbing region above the bandgap energy. Project work is directed at determining preferred structural models, spectroscopic index of refraction values, or preferred optical dispersion functions for each of these film systems, and, where possible, the variability of these parameters due to differences in film fabrication processes. Work is also directed

at extraction of accurate bandgap values and at interpreting the processing-related structure found in the dielectric function. Analysis has been done primarily with software developed by NIST for spectroscopic ellipsometry. This software allows maximum flexibility for addition of the latest published or custom-developed optical response models as appropriate for each material system investigated, and has allowed maximum transparency of analytical procedures employed.

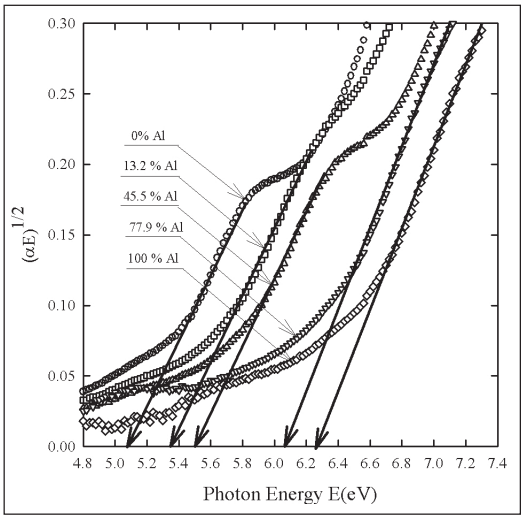

Figure 2. Tauc plots for determining band-gaps of HfAlO films with differing aluminum concentrations from analysis of ellipsometrically determined dielectric function.

DELIVERABLES: Determine mechanism for changes in dielectric function of HfAlO films vs. anneal temperature by correlation with physical measurements such as HRTEM and EELS. 4Q 2003

Relation between optical, electrical and physical measurements of thickness

Through collaborations with International SEMATECH, IC industry companies, and SRC university staff, as well as with key researchers in other parts of NIST, Project staff are leading and participating in a number of multimethod comparison studies of various ultra-thin gate dielectric films. These multimethod studies utilize techniques such as x-ray and neutron reflectivity, high resolution TEM, EELS, angle-resolved XPS, SIMS, C-V and I-V analysis, as well as spectroscopic ellipsometry and reflectivity. Examples of such comparisons are shown in Fig. 3. and Fig. 4. The results of these multimethod studies improve the general understanding of state-of-the-art (SOA) measurement capability for very thin films, and also allow Project staff to assess the results of various optical models being applied to the analysis of these films with respect to interface layers and structural composition, morphology, and uniformity. SOA C-V and I-V measurement capability for gate films has been established in the Project. Advanced 1-D analysis software from commercial and university sources has been established and benchmarked to determine the effect of model and algorithm sophistication on oxide film thickness values calculated from C-V and I-V data.

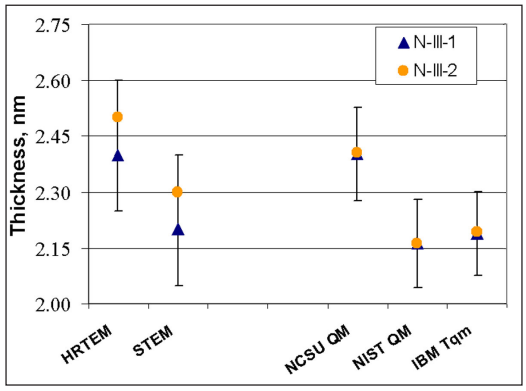

Figure 3. Thickness Value Comparison for TEM and C-V Measurements on 2 nm SiO_2 films being studied in conjunction with NC State Univ. and International SEMATECH.

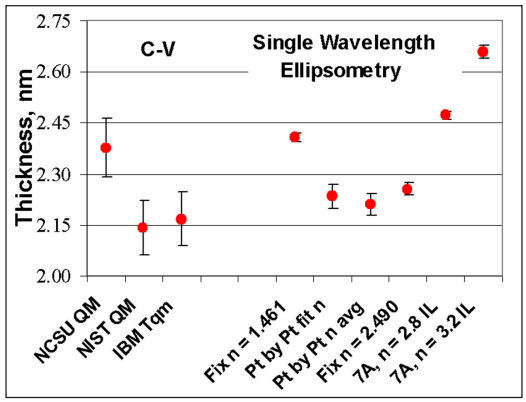

Figure 4. Thickness Values from Spectroscopic Ellipsometry Measurements and Various Analysis Models Compared with C-V Measurement Results.

DELIVERABLES: Develop evaluation of accuracy of NIST ellipsometry measurements of oxide thickness in range 2nm to 8nm based on results of international study sponsored by ISO CCQM. 3Q 2004

Establish and transfer basis of accuracy for thin dielectric films

Industry requirements for future thin dielectric film optical measurements and calibration standards have been identified at a NIST-sponsored workshop. Core ellipsometry measurement capability is being expanded and strengthened to meet these requirements. An

investigation has been started into cleaning and recontamination issues for film calibration standards to determine whether a NIST workshop's expressed goal of 0.015 nm long-term reproducibility of reference artifact values is obtainable. Results showing drift in apparent thickness after thermal desorption of accumulated residue is shown in Fig. 5. Procedures are being developed to enable traceability of instrument accuracy to NIST for suppliers of secondary thin-film reference materials without requiring volume production of NIST standard reference materials.

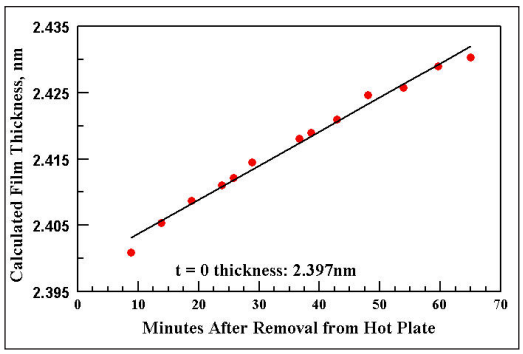

Figure 5. Apparent change thickness change with time for a 2 nm SiO_2 film as determined from ellipsometry measurements following a thermal desorption of previously accumulated contamination.

DELIVERABLES: Develop set of alternatives, with operating requirements, for possible traceability of optical, or electrical measurements of film thickness or other properties, consistent with ITRS needs.
4Q 2003

Many of the existing and innovative analytical procedures for the analysis of thin films such as x-ray photoelectron spectroscopy (XPS), non-linear optical spectroscopies (NLO), high resolution (HRTEM) and analytical electron microscopy (AEM) with x-ray and electron energy loss spectroscopies, low voltage scanning electron microscopy x-ray analysis, and Auger spectroscopy must be significantly improved to obtain accurate quantitative composition measurements on films with thicknesses below 10 nm. Our goals are to develop the necessary methods, analytical correction procedures, standard data and materials to determine realistically achievable accuracy levels for analysis of thin films by these techniques. Films for these measurement activities are obtained from industrial sources and fabricated in-house by spin coating metalorganic solutions.

Grazing incidence XPS allows both depth and chemical information to be attained from very thin (less than 10 nm) films. Using a NIST designed, built, and patented device on the Brookhaven synchrotron we have been developing the necessary instrumentation and data interpretation procedures to characterize International SEMATECH silicon oxynitride films, Fig. 6.

One of the more common methods of evaluating film thickness and composition is through the use of HRTEM and Analytical TEM, respectively. But the uncertainty of these approaches has only recently been looked at quantitatively. Films of dielectric materials grown on silicon were obtained from SEMATECH and analyzed to determine the accuracy of this HRTEM and AEM approach. Comparisons across many methods were made to determine the relative accuracy and precision of these approaches.

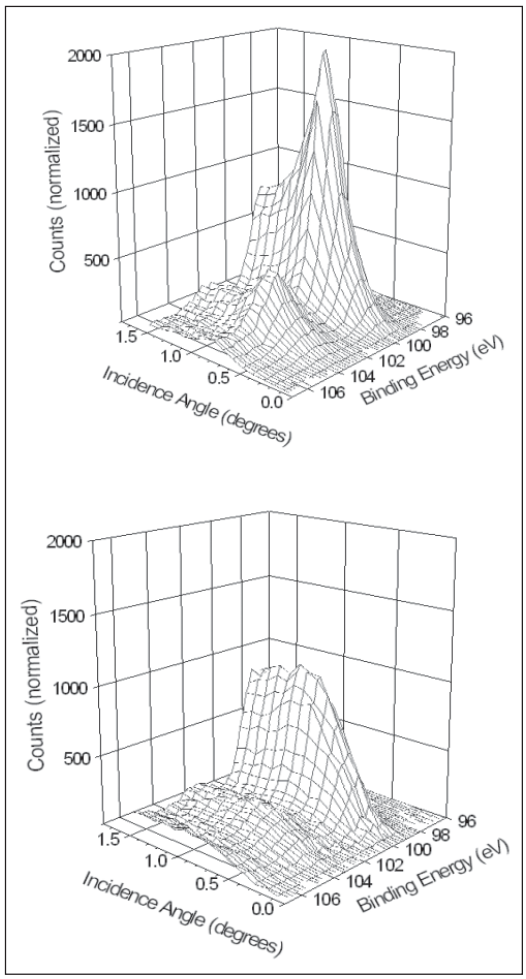

Figure 6. Comparison of Si 2p XPS spectra with angle taken at 1823 eV (top) and 1844 eV (bottom) from the same sample. The changes in the spectra reflect changes in the index of refraction across the Si K edge at 1839 eV.

GIXPS has been employed successfully as a novel means to analyze the depth, density, and chemical composition of the ultrathin dielectric layers being researched for future semiconductor devices. Serious discrepancies exist among the traditional methods of measuring these layers below 10 nm thickness. An important consideration has therefore been a determination of the accuracy of this new method and its potential sources of error. Discrepancies may also exist because of differences between phenomeno-logical and discrete (i.e. atomic) measurements. We have addressed the first question by studying the dependence of the results obtained from the GIXPS method on the accuracy of the physical parameters required as inputs. We are studying the second question by comparison with scattering measurements by short wavelength probes like x-rays and neutrons.

DELIVERABLES: Compare Grazing Incidence X-ray Photoelectron Spectroscopy (GIXPS) with neutron reflectivity and Ellipsometry for the measurement of silicon oxide and oxynitride films and determine the uncertainty of this method. 3Q 2003

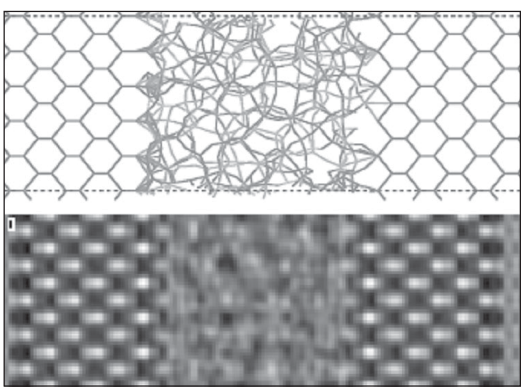

Figure 7. Molecular model of a gate stack (top) and one frame from an HRTEM simulation movie (bottom) showing changes in apparent thickness with changing imaging conditions.

The ability of HRTEM to measure the thickness of sub-4 nm gate di-electric films is in question, pending a quantitative understanding of the errors and uncertainties in the measurement process. The goal of this work is to quantify the accuracy of HRTEM as a technique for measuring the thickness of such films. Because device performance is very sensitive to the dielectric thickness, semiconductor device manufacturers consider this a critical fabrication parameter and are keenly interested in its accurate measurement. To address this problem, a suite of computer modeling tools was developed to build virtual gate stacks, Fig. 7 and simulate HRTEM micrographs from these stacks. Using these new tools, several hundred images of amorphous SiO_2 films between Si substrates were calculated, covering a range of imaging conditions and sample parameters. Combining the apparent thickness from the micrograph (measured value) and the known thickness from the model (true value), calculation of the accuracy as a function of the input variables is possible. A quantitative understanding of the errors in HRTEM thickness measurements plays an important role in improving the quality and yield of semiconductor electronic device fabrication.

DELIVERABLES: Determine uncertainty budget for the characterization the accuracy of High Resolution Transmission Electron Microscopy (HRTEM) for thickness measurements of ultra-thin gate dielectrics. 3Q 2003

EXAFS is a synchrotron x-ray spectroscopy tool that determines the average short-range (about 0.5 nm) local structural information around an atom that has absorbed an x-ray photon. Since the separate local structure around each atomic type present in a material can be measured, the technique is chemically sensitive. We are investigating the applicability of EXAFS to study crystallization and chemical bonding in gate dielectric films.

DELIVERABLES: Measure crystallinity in ZrO_2 films by EXAFS. 1Q 2003

The strategy of this effort will be to obtain or fabricate both device samples and blanket films, to perform reliability and electrical characterization of the devices, and to collaborate with other researchers to perform analytical characterization. Many issues such as tunnel/leakage current and spatially dependent properties associated with metal oxide and silicate dielectrics are also present in ultra-thin oxide and oxide-nitride stacked dielectrics. Therefore, many of the characterization schemes will first be developed on the simpler ultra-thin oxide and oxide-nitride dielectrics and then be applied to the metal oxide and silicate dielectrics.

There are two main focus areas for this project. The first focus area investigates the physics of failure and the reliability testing techniques for ultra-thin SiO_2 and high dielectric constant gate dielectrics. The physical mechanism responsible for “soft” or “quasi” breakdown modes in ultra-thin SiO_2 films and its implications for device

reliability will be investigated as a function of test conditions and temperature. Long-term time-dependent-dielectric breakdown tests will be conducted on SiO_2 films as thin as 1.5 nm at electric fields close to operating conditions. These tests will be used to determine the thermal and electrical acceleration parameters of device breakdown.

DELIVERABLES: Experimental results of charge stability and trapping in HfO_2 films including defect generation rates due to constant voltage stress. 2Q 2003

Experiments will be conducted to investigate Negative Bias Temperature Instability (NBTI) in p-channel MOSFET devices. NBTI has become a serious reliability problem in advanced microelectronic devices with ultra-thin gate dielectrics.

DELIVERABLES: Complete study of Negative Bias Instability (NBTI) of p-channel MOSFETs with 1.2 and 2.2 nm thick gate oxides under pulsed bias conditions. Determine time constants of defect generation and determine effect on circuit operation. 4Q 2003

The understanding generated in this research will be used to continue generating standard measurements through a NIST coordinated collaboration between EIA-JEDEC (Electronic Industries Association Joint Electron Device Engineering Council) and the American Society for Testing and Materials (ASTM). Studies on the reliability of high dielectric constant dielectrics such as oxide-nitride stacks will also be performed.

DELIVERABLES: A new JEDEC standard including guidelines for performing CV, GV and charge pumping measurements on ultra-thin SiO_2 and high-k films for extracting parameters such as Eot, Dit, V_{FB}, etc. Q3 2004

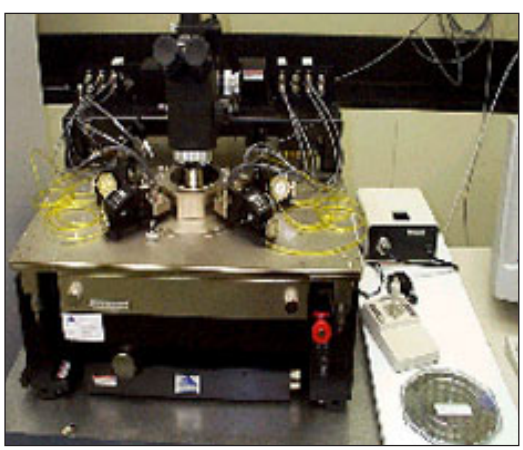

Figure 8. A low-noise (fA), high temperature (300 °C) probe station is used for electrical characterization of devices.

The second focus area is to investigate electrical measurement techniques, procedures and analysis associated with devices having thin oxide and alternate gate dielectrics. An example of a measurement instrument used in this work is shown in Fig. 8. The electrical measurement techniques that we are investigating include capacitance-conductance characterization, dielectric tunnel and leakage current characterization and defect density measurements such as charge pumping and conductance. Furthermore, standard properties and mechanisms/correlations for these dielectrics including defect centers, dielectric constant, defect generation rates, and leakage/tunnel current will be characterized.

High-k gate dielectric films will be obtained from key industrial and university groups. Electrical characterization methodologies will be developed to address various issues associated with these films, including large leakage currents, quantum effects, thickness dependent properties, large trap densities, transient (non-steady state) behavior, unknown physical properties, and the lack of physical models.

Examples of measurement problems that are being addressed include modifying and verifying electrical defect density measurement techniques, including conductance-frequency, capacitance-voltage, and charge-pumping.

DELIVERABLES: Studies of the long-term wear-out and breakdown of advanced high-k dielectrics. 3Q 2004

Accomplishments

- Brought commercial spectroscopic ellipsometer on-line with the capability of measuring out to 9.5eV. This instrument has been used extensively to investigate high-k dielectric materials. It's utility has been established by the ability to acquire enough data at higher energies to enable evaluation of the optical band-gap of the materials being studied. In addition, the higher energy spectral data has revealed significant structure in the refractive index (dielectric function) of the materials above the band-gap. This additional detail is generally attributed to processing-related effects on the material such as the onset of crystallization, and the segragation of ternary compounds into regions of different chemical compositions. These observations have led to the development of collaborations with scientists in other portions of NIST in order to develop localized structure and composition

information using such techniques as High Resolution TEM (HRTEM), Electron Energy Loss Spectroscopy and Grazing Incidence X-ray Diffraction. It is expected that the additional information from such techniques will enable the identification of specific dielectric function features with specific defects in the desired uniform amorphous film structure. The result may be the rapid identification of onset for various unwanted material defects and so serve as a valuable process monitoring improvement.

■ Investigated a set of Hafnium aluminate and titanium aluminate dielectric films with a range of aluminum concentrations from Yale Univ. The films were measured with the VUV ellipsometer from 1eV to 9.5eV. The generalized Tauc-Lorentz dispersion function, recently developed at NIST, was the primary dispersion function employed in the analysis. Film thicknesses and dielectric functions, determined from the analyses, showed clear trends in dielectic function values and shapes for the different films in the set, Fig. 9. These trends, as well as optical bandgaps were found to correlate very well with the aluminum concentration as determined by XPS measurements. However there were clear differences in the two types of films as determined from the ellipsometric modeling. For the as-grown HfAlO films, an optical model consisting of two layers of different film densities was found to be in excellent agreement with the experimental data. For the TiAlO films, only one film was needed in the model to fit the data.

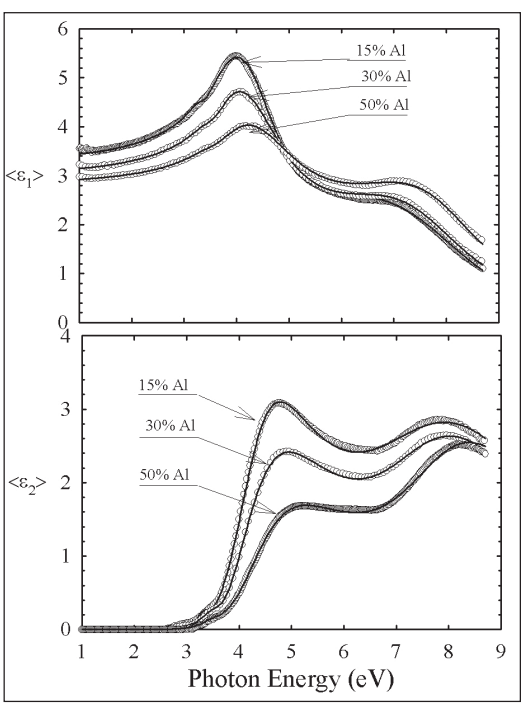

Figure 9. Testing the ability to fit ellipsometry measurement data of TiAlO films with GTL dispersion functions by comparison with a direct data inversion technique.

The experimentally determined dielectric function of HfAlO samples above 80% Al concentration showed a single peak in the dielectric function above the bandgap, while the films with lesser aluminum concentration showed an additional satellite peak. The optical bandgaps determined by Tauc-plots for HfAlO are seen to increase, meanwhile the relative film densities decrease, with the increase of Al in the films. In addition, the optical dielectric functions shift to the higher energy and decrease in their magnitudes as the films become more insulating. As a result, the Al appears to be mixed at the atomic level instead of forming a phase separation between HfO_2 and Al_2O_3. For TiAlO, there were similar results except that the fundamental optical bandgap was not strongly affected by the amount of Al incorporated in the films. To further the understanding of the physical properties in relation with the dielectric functions, all these films were subjected to various high temperature annealing and the optical properties were then measured and analyzed. The correlations between the dielectric function, the film structures such as densities and thicknesses will be established with the annealing temperatures.

■ Completed a study of thickness measurements of 2 nm SiO_2 films. A set of wafers, fabricates by low pressure thermal oxidation at NC State Univ. was used in the study. Ellipsometry, capacitance-voltage and HRTEM were used for the thickness evaluations. Single-wavelength ellipsometry measurements were taken on planar oxide wafers immediately following a thermal desorption cycle to remove accumulated surface contamination. Capacitance-voltage (C-V) measurements were taken on two wafers from the set that had a large array of fabricated capacitors, and HRTEM and EELS measurements were done on capacitor cross sections from both capacitor wafers. Ellipsometry measurements were analyzed with a variety of simple models of the oxide structure, including the transition interlayer model that had been used for previous NIST oxide thickness SRMs greater than 10 nm thick. The capacitance votage data was analyzed by several of the available quantum-mechanics based algorithms formulated to correct

for capacitance due to 2-D quantum states in the silicon substrate and for depletion in the polysilicon electrode. The purpose of the study was to determine the consistency of thickness values determined with the primary optical, electrical and physical measurements of thickness used in the industry for research, performance testing and process control of gate dielectric films.

Results showed a range of thicknesses resulting from all three techniques. The spread in ellipsometry and C-V results were primarily due to the choice of model or algorithm used to analyze the data while the spread in HRTEM and EELS results was almost exclusively due to the roughness of the upper and lower interfaces of the oxide films. Most of the overall spread was less than the thickness of one structural unit of SiO_2, however, it is clearly more than needed within the industry for process control purposes.

■ An extensive comparison of the most advanced Quantum Mechanical CV simulators was extended in a number of aspects. A systematic comparison of QM simulators for p-channel (n-substrate) devices was performed. The number of 1-D simulators in the test ensemble was extended to seven. Quantitative differences in the accumulation capacitance with ultrathin gate dielectric films were up to 20 % – similar to previously reported differences for n-channel devices. Some of the underlying physical and modeling differences leading to these differences were identified, investigated and reported; a complex interplay of a number of factors was found.

A method to extend the comparison to include 2-D simulators was also investigated and demonstrated. A model test structure was developed, refined and calibrated for use with Medici, a commercial 2-D simulator, to ensure that a quasi-1-D device was being simulated. Requests have been received for permission to use figures from this work in manuscripts, presentations and a University MOSFET class.

■ We performed an analysis of the effects of errors in physical input parameters (e.g., x-ray cross-sections, atomic form factors, electron mean free paths) on the results obtained for films of different thicknesses. This allowed us to identify the sensitivity of the results to certain inputs. We were able to test one of these dependences experimentally on the tunable NIST beamline X-24A at the National Synchrotron Light Source. By performing the same photoemission experiment with x-rays of slightly different energies about the K excitation edge of Si, the physical performance of the same sample was dramatically changed. An extensive analysis showed that the two results for the same sample differed by 16 %, which is a good indicator of the accuracy level of the optical parameters used in the determination.

■ A suite of computer modeling tools was developed to build virtual gate stacks and simulate HRTEM micro-graphs from these stacks. Using these new tools, several hundred images of amorphous SiO_2 films between Si substrates were calculated, covering a range of imaging conditions and sample parameters. Combining the apparent thickness from the micro-graph (measured value) and the known thickness from the model (true value) allows calculation of the accuracy as a function of the input variables. This revealed that measured thickness depends strongly on defocus and astigmatism. Using the Tcl scripting language, a graphical user interface was written to enhance the tools, improve efficiency, and simplify the database interface needed to manage the large amount of data that was generated.

■ EXAFS: The instrument at beamline X23A2 at the National Synchrotron Light Source in Brookhaven was configured in grazing incidence mode to measure 5 nm thick ZrO_2 gate dielectric films. Two series of films were measured: atomic layer chemical vapor deposited (ALCVD) films annealed at (825 to 900) °C in air, oxygen, nitrogen or vacuum (courtesy of J. Chang, UCLA); and spin-coated films annealed in air at temperatures of (200 to 800) °C (NIST). The degree of crystallinity in the films was estimated from the measured Zr-O-Zr bond angle spread $\Delta\theta^2$ in the EXAFS results. ALCVD films annealed at temperatures comparable to the thermal budget required for device fabrication (825 to 900) °C exhibited the same degree of crystallinity, $\Delta\theta^2 < 1°$, regardless of annealing atmosphere. Crystallinity in the spin-coated films decreased from $\Delta\theta^2 > 6°$ for the as-deposited films (200 °C) to $\Delta\theta^2 = 2\text{-}4°$ for films annealed above 600 °C.

■ Test samples: ZrO_2 thin films with thicknesses ranging from 2.5 nm to 10 nm were deposited by spin coating metalorganic zirconium acetate-based solutions onto (100) Si wafers. Processes were developed for depositing zirconium silicate films from zirconium acetate/tetraethoxysilane and zirconium nitrate/

tetraethoxysilane solutions. Silicate films with thicknesses of 10 nm to 15 nm and SiO_2/ZrO_2 ratios of 1:1 to 4:1 were fabricated; the composition of these films is being measured by EELS.

■ *New JEDEC document including noise-based test procedures for TDDB standard of sub-2 nm films.* The document includes new test methodologies for detecting soft or noisy break down events in ultra-thin gate dielectrics and is expected to be effective in detecting breakdown in films as thin as 1.5 nm. It has been approved by the JEDEC JC-14.2 Committee and by the JEDEC Board of Directors. A round-robin experiment is currently being planned to investigate the effectiveness of the test procedure.

■ *Negative bias temperature instability studied for deep sub-micro p-MOS devices under pulsed bias stress.* Bias Temperature Instability (BTI) has become a serious reliability problem in deep sub-micron *p*-MOSFETs as device dimensions are continually scaled down. The ΔV_{th} of NBTI was observed to be significantly reduced for pulsed bias repetition frequencies greater than 10 KHz implying an important role of hole trapping and detrapping. However, ΔV_{th} of PBTI was almost independent of frequency. The ΔV_{th} did not show significant channel length dependency. These results suggested that there are different mechanisms for ΔV_{th} of NBTI and NBTI and the reliability specifications of NBTI could possibly be relaxed under certain pulsed operation conditions.

■ *A study was performed to investigate defect generation in ultra-thin silicon dioxide films over large fluence ranges.* The defect generation rate (P_g) during constant voltage stress is investigated by using short-time voltage pulses over a large fluence range. It is found that P_g is not constant as a function of injected charge and the voltage acceleration of P_g in the linear defect generation regime is similar to that of the reciprocal of Q_{BD}. The change of carrier capture cross (σ) during defect generation was speculated as one of the reasons responsible for the change of P_g value. However, from this preliminary report, we have determined that the change of P_g can not be explained by the change of σ.

■ *A Visual Basic MOS simulation code was developed based on first-order approximations for the QM effects.* The code permits us to quickly evaluate experimental and simulation parameters on CV characteristics was developed. Comparisons with full Schroedinger-Poisson solvers (UTQuant) showed good agreement over a large range of experimental conditions (t_{OX} = 1.0 nm to 2.0 nm, $N_{sub} = 10^{15}$ cm^{-3} to 10^{18} cm^{-3}). The results show that a model based on the modification of the total semiconductor charge can be used to simulate QM CV characteristics of polysilicon-gated MOS devices.

The effects of a distribution of interface states with energy on the CV characteristics can be simulated. Further work on the impact of bulk insulator defects (slow states), EOT extraction, etc. can now begin. The code is currently being used in collaboration with J. Kopanski in *FASTC2D* applications and was transferred to SEMATECH to simulate the effects of interface trap density on CV characteristics. A manuscript detailing the code was prepared and accepted by *Solid State Electronics.*

Collaborations

■ Transfer of beta version of NIST-developed "SE Studio" software for analysis of spectroscopic ellipsometry data: Applied Materials and Korean Research Institute of Standards and Science

■ Development and characterization of 2 nm thick oxide reference materials, NC State Univ., KLA-Tencor and International SEMATECH; Measurement traceability experiments for SiO_2 and Si_3N_4 film thickness, VLSI Standards Inc. and Rudolph Technologies Inc.

■ Studies of optical, electrical and physical measurements and properties of oxynitrides and high-k dielectric films, NIST Divisions 837, 842, 852; Univ. Maryland, Univ. Minnesota, NC State Univ., Univ. Texas-Austin, UCLA, Yale Univ; IBM, Solid State Measurements, Texas Instruments, International SEMATECH.

■ Development and transfer of ellipsometer techniques and models for analysis, Penn State University and Univ. Maryland.

■ Spectroscopic ellipsometry characterization of low-K SiO_2 thin films, Division 854 and International SEMATECH

■ We collaborated on measurements on high quality SiO_2/Si samples by x-ray reflectivity at high momentum transfer at the Advanced Photon Source. The Fourier inversion of the reflectivities yields electron density with depth. Similarly, we have measured the neutron reflectivity from the same samples on a cold neutron beamline at the NIST Reactor. We are in the process of extracting

mass densities from the data with depth. These determinations allow us to calibrate the electron densities and mass densities used in layer thickness fits by GIXPS, which may differ greatly in thin films from the quoted values in the literature for bulk compounds. This type of verification has not been readily available.

- Based on simulated HRTEM micrographs at three different objective lens defocus values and three different specimen tilt angles, their results suggested (surprisingly) that minimum contrast defocus yields more accurate film thickness measurements than Scherzer defocus, and that a 25 mrad specimen tilt was more accurate that no tilt. Also, as expected, eliminating the spherical aberration of the objective lens improves the measurement considerably. Because of their sparse sampling of the parameter space (12 simulations to characterize changes in 6 variables), they were unable to quantify the results or confirm these promising anomalies. By using hundreds of simulations chosen to systematically sample the parameter space, this work seeks to extend their result and quantitatively characterize the error of the measurement as a function of the input variables. Optimum conditions for performing gate dielectric thickness measurements can then be chosen with confidence, and the inevitable effects of experimental variation in the measurement process can be assessed and managed.

- We have demonstrated the use of a multilayer thin film stack to selectively measure the VR-SFG signal from buried interfaces through the manipulation of Fresnel factors. We expect this technique to be broadly applicable to polymer/polymer and polymer/dielectric interfaces. The study of molecular orientation at buried polymer interfaces and its influence on adhesion has been demonstrated. The influence of molecular orientation on the functional properties of a wide range of transparent media can now be explored.

- Advanced Micro Devices, ultra-thin oxide reliability (John S. Suehle)

- Agere Technologies, ultra-thin gate oxide reliability (John S. Suehle)

- Analog Devices, ultra-thin gate oxide reliability (John S. Suehle)

- CSTL/Process Measurements Division, microhotplate-based sensor arrays (John S. Suehle and Michael Gaitan)

- Division 836, 837, 838, Roger Van Zee, et al., spectroscopic Ellipsometry of molecular electronics (Nhan V. Nguyen, Curt A. Richter, and John S. Suehle)

- Divisions 836, 837, 838, Dr. Roger van Zee et al., Molecular Electronics Competence Project (Curt A. Richter and John S. Suehle)

- Fairchild Semiconductor, ultra-thin gate oxide reliability (John S. Suehle)

- George Washington University, microhotplate-based chemical sensors (John S. Suehle)

- IBM, Alternative Gate Dielectrics (Eric M. Vogel)

- ISO TC202, Microbeam Analysis, Ryna Marinenko (EPMA), John Henry Scott (AEM), John Small (SEM), Dale Newbury (Nomenclature)

- JEDEC JC14.2 Committee on Wafer-Level Reliability, Dielectric Working Group, Chairman (John S. Suehle)

- N.C. State University (oxynitrides, nitrides, ultra-thin SiO_2), alternative gate dielectrics (Eric M. Vogel)

- National Semiconductor, ultra-thin gate oxide reliability (John S. Suehle)

- Penn State University, ultra-thin gate oxide reliability (John S. Suehle)

- SEMATECH, Alain Diebold, Gate Oxide Metrology Task FEP Z001 (Eric M. Vogel, James R. Ehrstein, Nhan V. Nguyen, and Curt Richter)

- Sharp Microelectronics, Dr. John Conley, characterization of Hafnium-oxide dielectric films, summer 2000 to summer 2003 (James R. Ehrstein and John S. Suehle)

- Texas Instruments, electrical and reliability characterization of ultra-thin gate oxides (John S. Suehle and Curt A. Richter)

- The Pennsylvania State University, Molecular Electronics (Curt A. Richter and John S. Suehle)

- University of Delaware, alternative dielectrics (John S. Suehle)

- University of Maryland, College Park, microhotplate-based chemical sensors (John S. Suehle)

- University of Maryland, College Park, ultra-thin gate oxide reliability (John S. Suehle and Eric M. Vogel)

- University of Minnesota, Alternate Gate Dielectrics, (Eric M. Vogel)
- Yale University, Alternative Gate Dielectrics (Eric M. Vogel)

Standards Committee Participation

- ASTM F-1 on Electronics, Membership Secretary and Member of Executive Subcommittee, (James R. Ehrstein)
- ASTM F-1 on Electronics, Subcommittee F1.06 on Silicon Materials and Process Control, Chairman and Ballot Coordinator (James R. Ehrstein)
- ASTM F-1 on Electronics, Subcommittee F1.06, Section B on Thin Film Characterization, Section Chair, (James R. Ehrstein)
- ITRS Conference, SEMICON West 2001, San Francisco, CA, July 13-18, 2001 (Barbara J. Belzer)
- JEDEC JC14.2 Committee on Wafer-Level Reliability, Dielectric Working Group, Chairman (John S. Suehle)

Recent Publications

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Chemical Metrology of Materials & Particle Contamination

Technical Contacts:
E. B. Steel
C. J. Powell

"Researchers in the Microanalysis Research Group continue to drive the commercialization of new x-ray detectors for materials microanalysis. The new silicon drift detectors, whose development is being supported and encouraged by the group, will allow unprecedented high-count x-ray detection. The semiconductor industry eagerly awaits the availability of commercial instrumentation, first for laboratory analysis applications, then eventually for online defect identification and classification."

Anne Testoni,
KLA-Tencor

Goals

Develop methods, standard materials and data for the characterization of the elemental composition, crystallographic phase, and chemical structure of microelectronic thin films and particle contaminants at nanometer spatial resolution. We develop and test x-ray, Field Emission Gun Scanning Electron Microscopy (FEGSEM), Transmission Electron Microscopy (TEM), X-ray Photoelectron Spectroscopy (XPS), Auger-Electron Spectroscopy (AES), Scanning Probe Microscopy (SPM) and diffraction methods to characterize the chemical composition and phase of microelectronic components and particle contaminants. Standard materials and data are developed to support these methods and enable improved accuracy and applicability of these methods to microelectronic devices.

Customer Needs

The constant introduction of new materials (SiGe, oxynitride, novel high-κ, low-κ, Cu, etc.) and decreasing dimension size in semiconductor fabrication cause increasing demands for new, selective, quantitative, interface and thin film metrology tools. Typically, many of these same measurement tools are applied to identify particle contaminants in the Fabs. There is a critical need to attain better speed and accuracy of chemical information from thin and chemically complex layered materials. The development of faster methods with known accuracy and the development of standards to demonstrate and maintain the quality of chemical analysis methods is critical to the continuous advancement of semiconductor technology.

The challenges and needs are outlined in the metrology section of the 2001 International Technology Roadmap for Semiconductors on page 21. "The rapid introduction of new materials, reduced feature size, new device structures, and low temperature processing continues to challenge materials characterization and contamination analysis. Correlation of appropriate offline characterization methods with each other and with inline physical and electrical methods should be accelerated. Use of characterization methods to provide more accurate information such as layer thickness or elemental concentration will continue. Characterization methods will continue to move toward whole wafer measurement capability and clean room compatibility."

Technical Strategy

1. SiGe thin film compositional standards – After the need for SiGe compositional standards was discussed at the 14th Annual Workshop on Secondary Ion Mass Spectroscopy (SIMS) in 2001, NIST contacted fabrication and analytical laboratory facilities to develop a reference material using an interactive approach. The typical time-frame for an NIST SRM is many years to develop, characterize, and bring to market. The need for SiGe standards was seen as an immediate need, because the current calibration method of Rutherford Backscattering is only accurate to 5–10 % relative and this is insufficient for reliable device production. NIST is collaborating with several semiconductor facilities and analytical laboratories to develop a suite of SiGe compositional standard films. Using an interactive data collection mechanism with collaborators and publishing the data on the web, a faster approach to standard materials production is being developed. This will allow materials to be used and compared even while reference data are being developed.

DELIVERABLES: Provide two interactive reference materials (Ge-Si thin films) for analysis by collaborating laboratories. 3Q 2004

2. Reference Data for AES and XPS – chemical characterization using AES and XPS depends on reference data for interpretation of measurements and an understanding of the physics of x-ray and electron interactions with semiconductor materials for modeling AES and XPS experiments with complex structures.

Standard Reference Database (SRD) 20 provides identification of unknown spectral lines in user measurements, retrieval of data for selected elements, retrieval of data for selected compounds, and retrieval of data by scientific citation.

SRD 64 provides values of differential elastic-scattering cross sections, total elastic-scattering cross sections, phase shifts, and transport cross

sections for elements with atomic numbers from 1 to 96 and for electron energies between 50 eV and 300 keV. These data are needed for modeling the transport of signal electrons in AES and XPS; in addition, they can be used for modeling electron transport in resists utilized in electron-beam lithography.

SRD 71 provides values of electron inelastic mean free paths (IMFPs), generally for electron energies between 50 eV and 2,000 eV. IMFPs are needed for quantitative analyses by AES and XPS, for deducing the surface sensitivity, and for modeling the transport of the signal electrons.

SRD 82 provides values of electron effective attenuation lengths (EALs) and related data for AES and XPS. EALs are needed mainly for measurements of thicknesses of overlayer films. Since XPS is being used to an increasing extent for the characterization of new gate-oxide materials, EALs have been computed from SRD 82 for zirconium dioxide, zirconium silicate, hafnium dioxide, and hafnium silicate for common XPS measurement conditions.

NIST is developing a new database (SRD 100: Simulation of Electron Spectra for Surface Analysis (SESSA)) to be used for AES and XPS analyses of thin-film structures. This database includes data from SRD 64 and SRD 71 and additional data describing x-ray and electron interactions with solids. SESSA will enable comparisons to be made of measured and simulated spectra for user-specified specimen morphologies and analytical conditions.

DELIVERABLES: Develop new database for interpreting AES and XPS data from thin-film structures. 2Q 2004

3. New X-ray Technology – Silicon Drift Detectors: A prototype of a silicon drift detector energy dispersive x-ray spectrometer (SDD-EDS) developed by Photon Imaging, Inc. of Los Angeles under a NIST Phase II SBIR grant is being tested on a scanning electron microscope (SEM) at NIST, Fig. 1. Conventional silicon (lithium) EDS forms the backbone of x-ray microanalysis systems implemented on more than 25,000 SEMs worldwide. Conventional EDS is limited to a maximum count rate of approximately 25,000 per second and is usually cooled with liquid nitrogen. The new SDD-EDS technology is capable of limiting count rates of 1MHz with 150 eV energy resolution and operates at -70 C, which is achieved with Peltier cooling. The SDD-EDS detection area is also physically large. Individual detector chips are 50 mm^2, and assemblies of multiple chips are possible. The combination of a large solid angle and a high-count rate are expected to lead to increased efficiency for SEM/x-ray microanalysis. The high count rate capability of SDD-EDS will be especially important for elemental mapping, where the number of photons counted per image pixel defines the concentration level that can be detected.

DELIVERABLES: Install and test second generation SDD detector system on UHV Auger microscope. Q1 2004

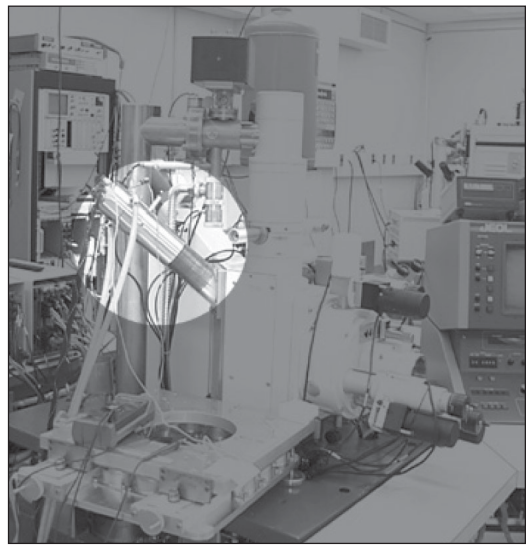

Figure 1. Silicon drift x-ray detector (highlighted oval) on conventional SEM.

4. New X-ray Technology – Microcalorimeter-EDS: The microanalysis laboratory at NIST Gaithersburg is working as a Beta-test site for the NIST-Boulder µcal EDS system (discussed elsewhere.) The system has been outfitted with a second-generation Cu-Mo thermometer rather than the first-generation Al-Ag. Immediately after installation of the new detector, the NIST Boulder staff obtained 7 eV resolution on Al. The NIST Gaithersburg staff was then instructed on the operation and maintenance of the cryogenic systems and the adjustment of the cryoelectronics, including the SQUID array, that are critical to obtaining optimum performance.

The initial thrust of the research for the application of this high resolution x-ray detector is in the development of fundamental x-ray data including x-ray weights of lines and peak shape and energy shifts. While the characteristic x-ray energies above about 3 keV are reasonably well known, the energy and especially the relative intensity of lower energy x-ray lines in L and M shell x-rays

are not well known and causes significant uncertainty and bias when analyzing complex thin film systems, e.g. W-Si. The characteristic peak energy can shift and peak shape can change as a function of chemical bonding allowing the possibility of chemical compound identification and mapping using the microcalorimeter. A feasibility study of a new database for chemical x-ray data is being initiated.

The development of these standard x-ray data systems requires that we first establish a reproducible response function in intensity and energy for the detector.

DELIVERABLES: Test modifications to the microcalorimeter temperature regulation system to determine if they improve detector stability. 1Q 2004

5. Characterization of particles: We are developing two areas of metrology for particles – quantitative chemical analysis using electron and x-ray spectroscopies and quantifying morphology through image analysis of electron microscope images.

The quantitative elemental characterization and identification of nanometer and micrometer-sized particles is critical to defect control. In the chemical analysis of particles with electron-beam instruments, the size and shape of the particle often results in large analytical errors associated with x-ray emission and absorption. Over the years, several different researchers have developed correction procedures to minimize the uncertainties associated with particle analysis. Although these correction procedures reduce the effects of particle geometry, elemental concentrations determined from the quantitative analysis of particles by these methods are often accompanied by errors on the order of 10 % to 50 % relative compared to 3 % to 5 % relative errors for the analysis of conventional samples. We are investigating the advantages and disadvantages of low voltage electron beam analysis, schematically shown in Fig. 2.

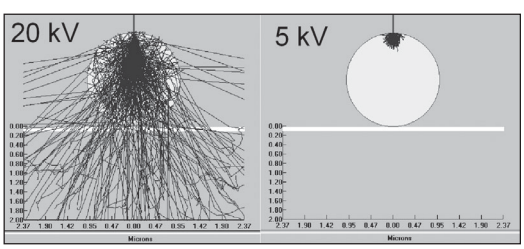

Figure 2. Schematic results of Monte Carlo calculation of electron beam interaction with a two micrometer particle sitting on substrate.

In addition to using chemical composition to classify particles, the shape and surface texture of a particle can help to classify or identify it and may also be indicative of its chemical composition or the process through which it was created. Shape and texture are used routinely by humans viewing objects, while many image analysis approaches currently only use a handful of parameters, such as roundness or root mean square roughness. Since the fractal dimension of a boundary or surface seems visually related to its roughness or tortuosity respectively, we are investigating the applicability of these dimensions for the description of the shape and texture of individual grains of particulate matter. These physical objects by their very nature do not have true fractal shapes, but we hope that they do exhibit fractal-like behavior in a limited size range (the "local fractal dimension" or LFD). After investigation of some image processing methods in the literature, we have chosen and refined two, to characterize the LFD of the projected boundary of a particle and the LFD of an averaged brightness profile representing the surface. These measurements require the particle to be segmented from background, a tedious task to perform manually and a problematic one to do automatically. We have developed operator-aided segmenting methods that are designed for the image data sets under study.

DELIVERABLES: Develop an accurate quantitative analysis procedure for high-angle x-ray emission spectroscopy to allow simultaneous combined x-ray/EBSD phase mapping and x-ray elemental analysis.

Accomplishments

- Electron Probe Microanalysis – Wavelength Dispersive Spectrometry (EPMA-WDS) was used to test the heterogeneity of bulk SiGe wafers for use as primary standards in subsequent characterization of SiGe thin films on Si. Two different commercially available SiGe single-crystal boules (nominal compositions of 14 atomic % Ge in Si and 6.5 atomic % Ge in Si) were evaluated for the extent of micro- and macroheterogeneity. The expanded uncertainties for the two SiGe wafers and for pure Si and Ge wafers were determined. The SiGe14 wafer was found to be a suitable bulk standard with a measured heterogeneity about twice that of the pure Si and Ge wafers.

- During the past year, a new version of the popular NIST X-Ray Photoelectron Spectroscopy Database (SRD 20) was released, a new version

of the NIST Electron Elastic-Scattering Cross-Section Database (SRD 64) was released, and work advanced on a new NIST database for Simulation of Electron Spectra for Surface Analysis (SESSA).

■ Calculations have been made of electron effective attenuation lengths (EALs) for zirconium dioxide, zirconium silicate, hafnium oxide, and hafnium silicate using the NIST Electron Effective-Attenuation Length Database (SRD 82). These EALs were calculated for the principal photoelectron lines excited by Al Kα x-rays and for a range of film thicknesses and emission angles of practical relevance. The EALs were compared with the corresponding inelastic mean free paths to determine the magnitude of the correction for elastic-scattering effects on film-thickness measurements. For common measurement conditions, this correction varied between 12 % and 20 %.

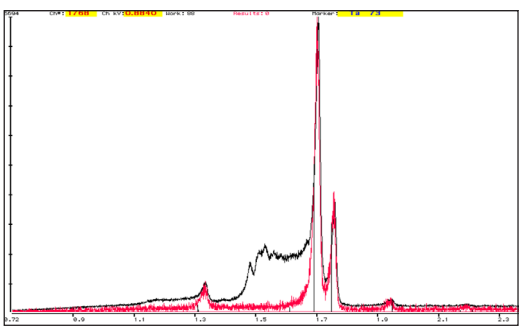

Figure 3. The two overlapped spectra above demonstrate the stable (red spectrum) and unstable (black spectrum) on the same tantalum elemental standard.

■ The NIST microcalorimeter energy dispersive x-ray spectrometer (μcal EDS) has been successfully transferred from NIST Boulder to an analytical microscopy environment at NIST Gaithersburg. Routine operation and maintenance of the cryogenic and cryoelectronic systems has been taken over by Division 837 staff. Resolution performance of 9 eV or better has been achieved for short (≈100 s) accumulations. Long term (>1000 s) measurements have been found to be subject to instability that limits accurate measurement of x-ray peaks, in Fig. 3. Division 837 researchers are currently working with NIST Boulder to diagnose the problem(s) and design corrective measures to improve the detector stability during long analysis times.

■ The Silicon Drift X-ray Detector has been used successfully to collect a 256x256 spectrum image with total mapping time of approximately 650 s. This compares to a collection time of approximately 2 hours using a conventional monolithic Si detector. We are actively working with Photon imaging to develop a faster pulse processing system.

■ We have evaluated the x-ray analysis of particles at low accelerating voltages (5 keV). Results indicate that the effects of particle morphology increase as a result of x-ray absorption requiring careful alignment of the particle under the electron beam to minimize the magnitude of the absorption.

Collaborations

Agere, Stevie (now at North Carolina State University), McKinley, SiGe thin film standards

Evans Analytical, Buyuklimanli, SiGe thin film standards

Institute of Physical Chemistry (Warsaw), Jablonski, development of databases for AES and XPS and calculations of effective attenuation lengths

Motorola, Christiansen, SiGe thin film standards

Photon Imaging, Iwanczyk, new x-ray detector technology

Recent Publications

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Thin Film X-ray Metrology for Microelectronics

Technical Contact:
Richard J. Matyi

Goals

Provide the semiconductor industry with high accuracy x-ray based measurement methods, reference materials, and data for the structural characterization of simple and complex thin film structures.

Customer Needs

Thin film thickness, density and interfacial roughness are critical to the performance of conducting and dielectric layers in semiconductor devices. Sensitive and accurate measurement of such properties are needed in the process development phase as well as in subsequent manufacturing practice. In the process development phase the needs are for structural properties that can be associated with the electrical performance characteristics of subsequently patterned device arrays. In the subsequent manufacturing phase the need is principally to calibrate the responses of on-line measurement tools that do not deliver first-principles based data. These tools have been developed to meet the needs for high measurement throughput and compatibility with the production environment. Such tools have material-dependent calibration requirements that lead end users and tool manufacturers to look for alternatives that are less sensitive to materials properties and process variability.

Technical Strategy

The sub-nanometer wavelengths and relatively weak interaction of x-ray probes make them a nearly ideal means for determining the geometry of the thin film and multilayer structures that underlie modern semiconductor manufacturing. As critical dimensions continue to shrink, the sizes of structures are becoming far smaller than optical wavelengths but are approaching the nanometer size of x-ray wavelengths. Thus x-ray probes are increasingly more favorable for advanced metrological applications. This fact has not been lost on the community of semiconductor tool suppliers – within the past two years there has been a significant increase in fab-compatible x-ray metrology instruments.

Our approach has been to develop advanced x-ray metrological capabilities including high performance instrumentation, advanced forms of modeling and analysis, and working with suppliers and users of x-ray metrology tools so that both communities receive the maximum benefit from these instruments.

Our specific technical goals are the following:

1. We have made advanced x-ray measurement capabilities available for applications to a considerable range of structural problems involving metallic interconnect layers, advanced dielectrics, and diffusion barrier films (see Fig. 1). By responding to currently urgent problems, principally, but not exclusively, mediated through SEMATECH, it has been possible to develop first-hand knowledge of industrial needs as well as of the level of timely responsiveness needed to provide useful input to these problems.

DELIVERABLE: Quantitative measurements of density, thickness, and roughness in thin film semiconductor materials (4Q 2003)

2. Our program develops and applies novel and advanced x-ray analytical methods to reveal the microstructure of thin film and multi-layer

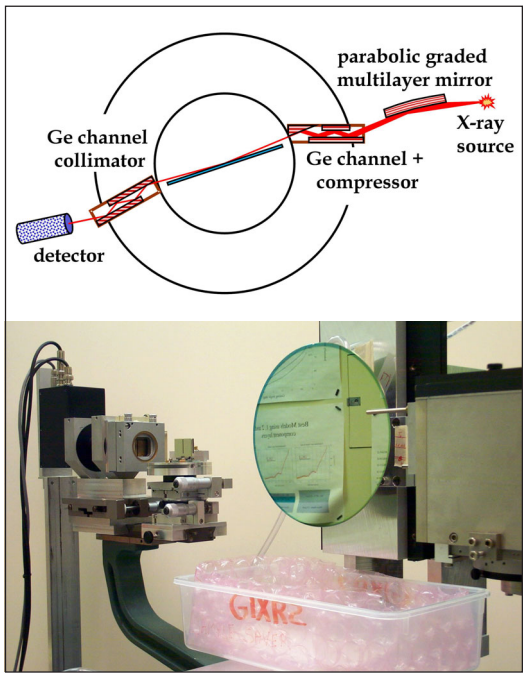

Figure 1. A high resolution x-ray reflectometry system (shown schematically above and in the photograph below) was designed and optimized for the routine analysis of complex thin film and multilayer structures that are of interest to the semiconductor industry.

structures produced by modern semiconductor manufacturing. To achieve this goal we must maintain close contact with SEMATECH, its member companies, and the semiconductor manufacturing environment in general to address the current critical needs of the industry and to anticipate future needs with x-ray tools.

The main components of this work are: (a) the development and application of high-resolution x-ray scattering techniques; (b) providing a rapid response to urgent problems identified by SEMATECH; and (c) working with the x-ray metrology tool users community to improve the utilization of x-ray measurement instruments for all. Both the details and the areas of emphasis of our program have evolved on the basis of this experience and guidance received during presentations to various specialized groups within the SEMATECH framework. Finally, we are in contact with commercial developers of x-ray instrumentation in order to facilitate interactions with customers through the documentation of best practices and the characterization of reference materials.

DELIVERABLE: Enlarge our knowledge base on the effects of systematic errors on the analysis of high resolution x-ray reflectometry analyses of semiconductor thin film structure (4Q 2003)

3. There are a variety of x-ray scattering tools that are not widely known in the semiconductor industry but have the potential to be very powerful tools for specific measurement problems. For instance, in thin film systems such as HfO_2, the development of polycrystalline structures is undesirable due to the impact of crystalline component on the electrical behavior of the film and its effect on measurement tools (*e.g.*, ellipsometry). However, the detection and measurement of the polycrystalline component of thin films (≈ 3 nm) in a laboratory setting is very difficult using conventional methods. We have proposed to explore the use of grazing incidence x-ray diffraction (GIXD), or diffraction under conditions of specular reflection, to probe the crystalline structure of thin HfO_2 materials. Other methods of interest to us is the use of quasi-forbidden or strictly forbidden x-ray reflections as a sensitive probe of damage and strain in ion implanted structures.

DELIVERABLES:. Demonstrate grazing incidence x-ray diffraction assessment of crystallinity in HfO_2 films (2Q 2003)

Accomplishments

■ High-k dielectric films – We have continued our program on the structural characteristics of HfO_2 high-k film structures by high resolution x-ray reflectometry followed by computer fitting of the reflectometry scans. Fig. 2 below shows a series of HfO_2 layers grown under a variety of conditions. In all cases, the x-ray reflectivity measurements showed that the structure assumed from the nominal growth conditions did a poor job of describing the experimental data. For instance, an HfO_2 layer with an expected thickness of 175 Å was found to be only 148 Å thick. All layers were well described by a stratified structure with a composition that varied with depth.

X-ray reflectivity calculations are robust; the theory of x-ray scattering is very well established, and comparisons between experimental data and calculated profiles have been proved to be a reliable method for performing structural analyses. While there may be questions regarding the "uniqueness" of x-ray analyses due to the noise that is inherent in x-ray scattering, we have emphasized to the semiconductor industry a simple yet accurate descriptor of the method – x-ray reflectivity may not be the best technique to reveal what a structure is, but it is excellent at showing what it cannot be.

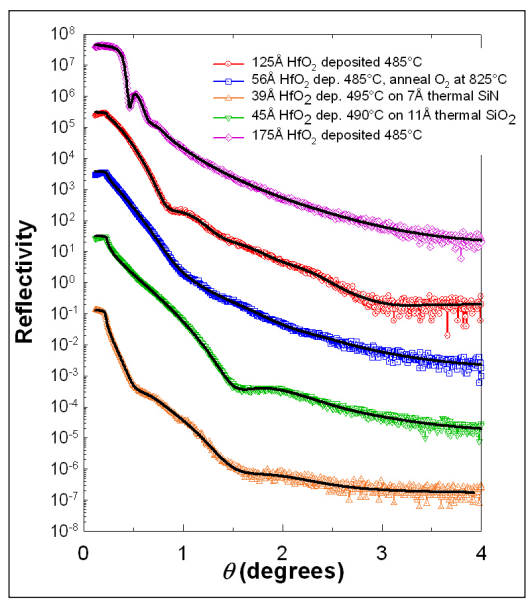

Figure 2. Comparison of experimental and fitted x-ray reflectometry data from a series of HfO_2 films processed under a variety of conditions.

■ Ta/TaN Cu diffusion barriers – We have examined thin (nominally 70 Å) Ta and TaN diffusion barriers with thick (≈750 Å) copper layers by high resolution x-ray reflectometry. X-ray methods are particularly useful for the analysis of complex metal systems, because the x-rays can "see" a thin buried layer that lies beneath a much thicker top layer. Data from these samples are shown in Fig. 3; the rapid oscillations seen at small angles in the experimental curves arise from the interference of the phases of the scattered x-rays from the thick Cu and the thin underlying Ta or TaN layers. The model fit of the experimental data shows excellent agreement between the two for an assumed structure consisting of a thin (approximately 15 Å) SiO_2 layer at the silicon substrate, Ta or TaN layers of 96 Å and 88 Å, respectively, and Cu with a top copper oxide layer.

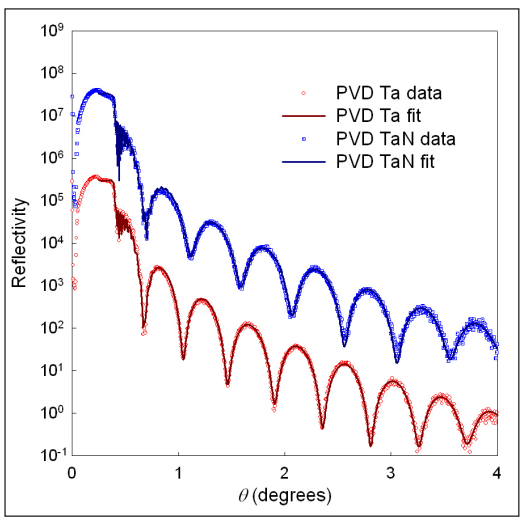

Figure 3. X-ray reflectometry analyses of Ta/Cu and TaN/Cu systems.

■ Errors in x-ray reflectivity analyses – We have initiated a research program to define the effect of a variety of systematic errors on the reliability of x-ray reflectometry analyses. Fig. 4. shows the effect of intentional misalignments on experimental x-ray reflectivity profiles from nominally bare silicon and ZrO_2/Si. These results clearly demonstrate that even small angular mis-sets in sample alignment can have a large effect on the resultant specular x-ray scan. We are currently performing theoretical analysis of the effects of various experimental aberrations on x-ray reflectivity data. This information should be useful to the vendors and users of fab-compatible x-ray reflectivity systems for estimating the effects of instrumental errors on reflectivity analyses.

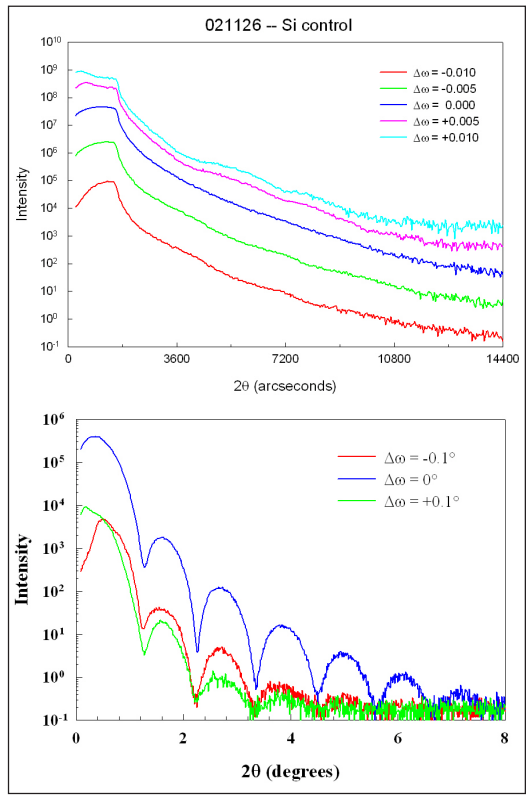

Figure 4. Effects of misalignment on x-ray reflectivity scans from nominally bare Si (top) and ZrO_2/Si (bottom).

In addition, we have significantly upgraded our experimental capability for x-ray reflectometry analyses. Construction and calibration has been completed on a novel "metrologically-sound" x-ray reflectometer that will permit quantitative analyses of the effects of misalignments on x-ray reflectivity analyses. Furthermore, we have installed various high-precision sample positioning fixtures that will both improve the accuracy of our own reflectivity measurements and permit quantitative analyses of systematic errors in reflectivity measurements to be performed.

■ Grazing incidence x-ray diffraction for crystallinity in high-k materials – As mentioned earlier, crystalline inclusions in otherwise amorphous HfO_2 could both alter the electrical characteristics of this high-k material and complicate other measurement techniques. To address this issue, we have developed a grazing incidence x-ray diffraction (GIXD) capability for the analysis of crystallinity in very thin films. Pictured below is a GIXD scan from a HfO_2 layer following a furnace anneal (560 °C, 2 h). The experimental GIXD scan (see Fig. 5) clearly shows crystalline peaks that apparently arise from

the monoclinic and ortho-rhombic phases of HfO_2. We are continuing to refine this technique and use its capabilities to rationalize various anomalies that have been observed in ellipsometry analyses of thin HfO_2 materials.

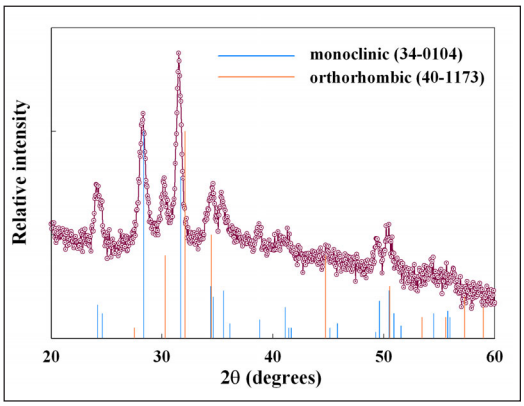

Figure 5. GIXD scan from HfO_2/Si with superimposed calculated peak positions and intensities for monoclinic and orthorhombic crystalline HfO_2.

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Interconnect and Packaging Metrology Program

Advances in interconnect and packaging technologies have introduced rapid successions of new materials and processes. Environmental pressures are leading to the reduction and eventual elimination of lead in solder used for attaching chips to packages and packages to circuit boards. The overall task of this program is to provide critical metrology and methodology for mechanical, chemical, metallurgical, electrical, thermal, and reliability evaluations of interconnect and packaging technologies.

The function of packaging is to connect the integrated circuit to the system or subsystem platform, such as circuit board, and to protect the integrated circuit from the environment. The increasing number of input/output (I/O) on circuits with vastly larger scale of integration is forcing ever smaller I/O pitches, the use of flip chip bonding, and the use of intermediary platforms called interposers. The integration of sensors and actuators onto integrated circuits through MEMS technology and the increasing use of low cost integrated circuits in harsh environments is increasing the complexity of the packaging task. Environmental concerns are forcing the need for development of reliable lead-free solder and other low environmental impact packaging materials.

System reliability requirements demand modeling, testing methods, and failure analysis of the integrated circuits before and after packaging. Metrology is a significant component of reliability evaluation.

Superconformal Deposition of Copper and Advanced Interconnect Materials

Technical Contacts:
T. P. Moffat
D. Josell

"We are very excited about the capabilities of this tool, and we want to put it to use ASAP!!! Yet another example of NIST innovation helping industrial competitiveness!!!"

Dennis Buss, Vice President, Silicon Technology Development, Texas Instruments

Goals

This project is developing solutions to metrology issues confronting integrated circuit manufacturers in the area of interconnect metallization. The main effort involves determining the essential process requirements for superconformal filling of high aspect ratio features. For electrodeposition this includes: determining measurement methods for characterizing electrolytes, quantifying kinetics for industrially relevant copper electrolytes, and direct assessment of the efficacy of electrolytes for trench and via filling. This project also seeks to explore the generality of the superconformal filling mechanism for metallizations other than copper and processes other than electro-deposition.

Customer Needs

Increasing information technology requirements have yielded a strong demand for faster logic circuits and higher-density memory chips. The low electrical resistivity of copper and the ability of electrodeposition to "superconformally" fill high aspect ratio features has made electrodeposited copper the interconnect material of choice. To support these efforts the National Institute of Standards and Technology (NIST) has a program focusing on the role of electrolyte additives on the superconformal filling process. Evaluation of prospective electrolytes will be greatly accelerated by NIST's recent development of a predictive capability for describing the influence of additives on superconformal deposition.

Interconnect metallization issues are discussed in the 2001 International Technology Roadmap for Semiconductors on Interconnect Section, page 11.

Technical Strategy

1. The semiconductor industry has steadily worked to reduce interconnect dimensions, while improving their electrical performance. As a result, metallization has changed from sputtered aluminum (copper) alloys to electrodeposited copper. To meet future industrial needs, we have developed the metrology and fully disclosed electrolytes that permit characterization of the ability of generic electrolytes to fill fine features. We are also developing electrolytes and metrology for deposition of advanced interconnect materials as well as alternative processing schemes such as chemical vapor deposition.

In FY 2003 we have:

- Established the generality of the Curvature Enhanced Accelerator Coverage (CEAC) mechanism for superfilling by electro-depositing copper, silver and other metals.
- Developed a new processing method for eliminating the delay time for superfill to begin during electrodeposition, thereby increasing the aspect ratio and decreasing the width of trenches that can be superfilled.
- Extended the CEAC mechanism to quantitatively predict superfill during chemical vapor deposition.
- Extended the diagnostic capability of voltammetry for monitoring electrolyte aging effects.
- Demonstrated the utility of using a cation selective membrane to minimize electrolyte aging effects.

Our current measurement and modeling effort is focused on copper and silver metallizations, the latter metal having the lowest resistivity of any element, thus having potential on-chip applications. Superconformal silver deposition was demonstrated in the past year in the Metallurgy Division and is the first example of superconformal feature filling with a metal other than copper. "Superfilling" is characterized by bottom-up deposition as shown in Fig. 1.

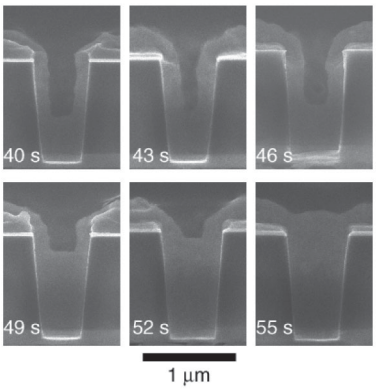

Figure 1. Superconformal electrodeposition of silver in vias. After a ~40 s incubation period of conformal filling, rapid bottom-to-top filling occurs.

DELIVERABLES: We will publish the first complete account of the electrochemical behavior of a model electrolyte for superconformal electrodeposition of copper. The kinetic model details both the adsorption and consumption dynamics of the catalytic additive. 4Q 2003

Our publications explain the mechanism behind the process of superconformal "bottom-to-top" filling (see Fig. 2). They also detail how it can be fully quantified using only experiments with planar substrates. Electrochemical and surface analytical measurements on planar substrates were used in FY2002 to establish a one-to-one correlation between catalyst coverage and the metal deposition rate. In the case of silver deposition, adsorbed selenium was found to catalyze the deposition rate. For the thiol/disulfide-polyether-halide additives used in copper superfilling, the sulfonate-end group of the thiol or disulfide molecules was found to destabilize the passivating polyether surface film thereby accelerating the local metal deposition rate.

DELIVERABLES: We will develop software for modeling superconformal feature filling as well as codes for describing roughness evolution during film growth on an arbitrary surface profile. 4Q 2003

Our model for the superconformal filling process has been implemented in computer code. Three different electrode shape change algorithms have been developed. They show excellent agreement with experimental results. These algorithms are available from the Metallurgy Division website, and are currently being examined by Texas Instruments and IMEC.

http://www.ctcms.nist.gov/~wd15/superfill/superfill.html

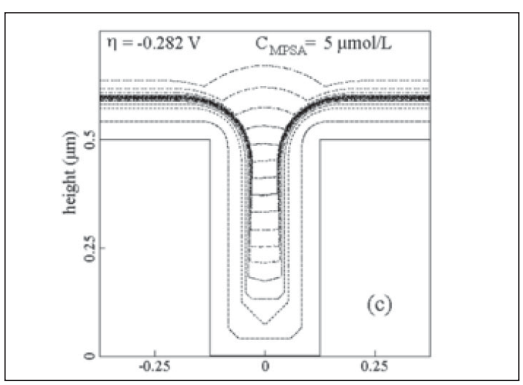

Figure 2. This simulation details the time-dependent filling of a trench (viewed in cross section). One observes the initial conformal deposition, bottom-to-top superconformal filling, and final creation of an overfill bump. All these phenomena are also observed industrially.

DELIVERABLES: We will publish an analysis quantifying how the mechanism that results in superconformal filling of fine features also yields bright deposits on planar surfaces. 4Q 2003

The insight provided by uncovering the CEAC mechanism has enabled the development of a new two-step process for superconformal film growth; in contrast to standard electrodeposition techniques, the catalyst is deposited on the substrate prior to the metallization step. Specifically, the patterned substrate is first "derivitized" or "dosed" with a submonolayer coverage of catalyst and then transferred for electroplating in an electrolyte that does not contain the catalyst.

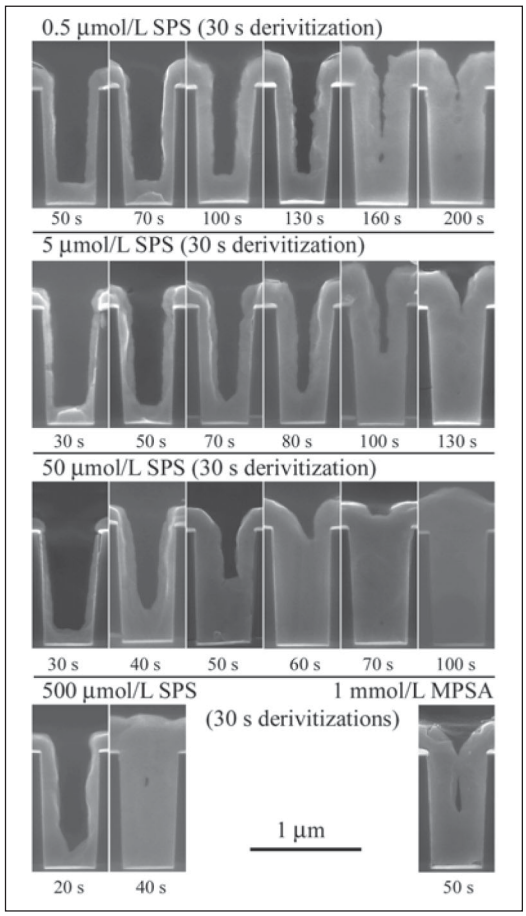

Figure 3. Time evolution of trench filling after different "derivitization" steps. The concentration of SPS or MPSA catalyst used for the 30 s surface derivitization steps are indicated. All specimens were transferred to a catalyst-free electrolyte for copper deposition.

For an optimum catalyst coverage, superconformal filling of trenches and vias occurs as shown in Fig. 3 (50 μmol/L SPS). If the catalyst coverage is too low or high, conformal or subconformal

deposition occurs, resulting in void formation during feature filling (0.5, 500 µmol/L SPS, 1mmol/L MPSA). The filling behavior is completely analogous to that obtained using a single (conventional) electrolyte containing both catalytic and inhibiting species. The new process provides unambiguous verification of the CEAC mechanism of superconformal film growth. Restricting the catalyst to the surface prior to metal deposition also enables the rate differentiation provided by the CEAC mechanism to be increased relative to the conventional process. From a technical perspective, the two step process offers an interesting solution to the difficult control issues associated with catalyst destruction and related aging effects which are known to occur in the "conventional" single-electrolyte superfilling process currently used in industry.

DELIVERABLES: We will quantify the effect of iodine catalyst on superconformal chemical vapor deposition of copper. 4Q 2002

The generality of the CEAC mechanism has now been extended to include the first quantitative prediction of superconformal chemical vapor deposition (CVD). More recently, this work has enabled a direct comparison of the CEAC mechanism with detailed experiment results on iodine catalyzed copper CVD as shown in Fig. 4.

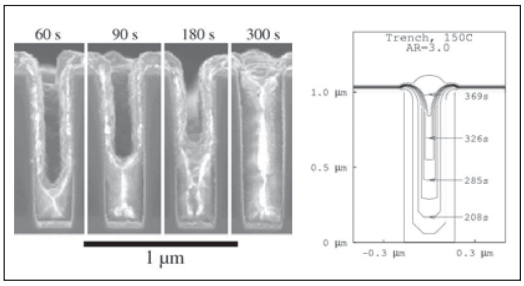

Figure 4. Superconformal filling of vias during iodine catalyzed chemical vapor deposition. Experimental via results are from Hynix Semiconductor and model predictions for a trench are from the Metallurgy Division of NIST.

2. In collaboration with William Egelhoff (MSEL) and Lee Richter (CSTL) we have quantified the impact of the catalyst on the superconformal filling process through electrochemical measurements as well as surface studies (XPS, FTIR).

DELIVERABLES: We anticipate several publication describing surface analytical measurements of catalyst evolution during superconformal copper and silver electrodeposition. 3Q 2002

3. Our publications note the link that can exist between electrolytes that provide "bright" deposits and those that yield superconformal filling of fine features.

DELIVERABLES: We will publish analysis quantifying how the mechanism that results in superconformal filling of fine features also yields bright deposits on planar surfaces. 4Q 2002

Accomplishments

- We have quantified the kinetics of catalyst adsorption and consumption during copper electrodeposition. The derived kinetics have been used to demonstrate a one to one correlation between experiments and simulation of superfilling ~100 nm features.

- We have applied this understanding to demonstrate silver electrodeposition and copper chemical vapor deposition.

- A new two step process has been developed which allows the difficulties associated with electrolyte aging effects to be avoided and enables optimum feature filling.

- In a similar manner, we have improved the stability of the "conventional" superfilling process by introducing a cation selective membrane into the electrochemical cell.

We have established the metrology for determining all kinetic parameters required to model superconformal feature filling from studies of deposition on planar substrates.

Collaborations

D. Wheeler, B. Baker, W.E. Egelhoff, Materials Science and Engineering Laboratory. L. Richter and C. Yang, Chemical Science and Technology Laboratory, NIST.

ISMT, Christian Witt; fabrication of patterned substrates.

Motorola, Bradley Melnik; Fabrication of patterned Substrates.

Recent Publications

B. C. Baker, C. Witt, D. Wheeler, D. Josell and T. P. Moffat, "Superconfromal Silver Deposition Using KSeCN Derivatized Substrates," Electochemical and Solid-State Letters, 6, C67-C69 (2003).

D. Wheeler, D. Josell and T. P. Moffat, "Modeling Superconformal Electrodeposition Using The Level Set Method," J. Electrochem. Soc., 150, C302-310 (2003).

D. Josell, S. Kim, D. Wheeler, T. P. Moffat, S. G. Pyo, "Superconformal Deposition by Iodine-Catalyzed Chemical Vapor Deposition," J. Electrochem Soc.,150, C368-C373 (2003).

T. P. Moffat, B. C. Baker, D. Wheeler and D. Josell, "Accelerator Aging Effects During Copper Electrodeposition," Electrochemical and Solid-State Letters, 6, C59-C62 (2003).

S. G. Pyo, S. Kim, D. Wheeler, T. P. Moffat and D. Josell, "Seam-free fabrication of submicrometer copper interconnects by iodine-catalyzed chemical vapor deposition," J. Appl. Phys., 93, 1257 (2003).

B. C. Baker, M. Freeman, B. Melnick, D. Wheeler, D. Josell, T.P. Moffat, "Superconformal Electrodeposition of Silver from a KAg(CN)2-KCN-KseCN Electrolyte," J. Electrochem. Soc., C61-C66 (2003).

T. P. Moffat, D. Wheeler, C. Witt and D. Josell, "Superconformal Electrodeposition using Derivitized Substrates," Electrochemical and Solid-State Letters, C110-C112 (2002).

D. Josell, B. Baker, C. Witt, D. Wheeler and T. P. Moffat, "Via Filling by Electrodeposition: Superconformal Silver and Copper and Conformal Nickel," J. Electrochem. Soc., 149, C637-C641 (2002).

T. P. Moffat, B. Baker, D. Wheeler, J.E. Bonevich, M. Edelstein, D. R. Kelly, L. Gan, G. R. Stafford, P. J. Chen, W. F. Egelhoff, and D. Josell, "Superconformal Electrodeposition of Silver in Submicron Features," J. Electrochem. Soc. 149, C423 (2002).

Our findings have also been conveyed to U.S. industry, academia and other national laboratories through more than eighteen external presentations in the last year.

Porous Thin Film Metrology for Low-k Dielectric

Technical Contacts:
Barry J. Bauer
Wen-li Wu

"The SANS/SXR measurements have become a key metric in our low-k dielectric materials characterization and screening process"

Jeffrey Wetzel – International SEMATECH

"The NIST x-ray reflectivity program is useful, perhaps even critical, to the industry"

Abner Bello – Applied Materials

Goals

In this project, we are developing measurement methods of morphological characteristics in porous thin films for low-k dielectric applications. We work closely with industrial collaborators to develop and apply these methods to advanced materials destined for integration in the next generation of integrated circuits. The unique measurement methods we apply include x-ray reflectivity (XR), small angle neutron scattering (SANS), Rutherford backscattering spectroscopy (RBS), and forward recoil elastic spectroscopy (FRES). Our efforts focus on two areas, providing high quality data and measurements of film thickness, coefficient of thermal expansion (CTE), moisture uptake, film connectivity, pore volume, pore size, and matrix density on films under development, and devising new measurement methods to characterize pore size distribution (PSD), pore connectivity, and matrix homogeneity.

Customer Needs

As integrated circuit (IC) feature sizes continue to shrink, new low-k interlevel dielectric materials are needed to address problems with power consumption, signal propagation delays, and cross talk between interconnects. One avenue to low-k dielectric materials is the introduction of nanometer scale pores into a solid film to lower its effective dielectric constant. However, the pore structure of these low-k dielectric materials strongly affects important material properties other than the dielectric constant such as mechanical strength, moisture uptake, coefficient of thermal expansion, and adhesion to different substrates. The characterization of the pore structure is needed by materials engineers to optimize and to develop future low-k materials and processes. Currently, there is no clear consensus among IC chip manufacturers for the selection of a class of material or a processing method of nanoporous films. Candidates include silica-based films, organic polymers, inorganic spin-on materials, chemical vapor deposited materials, and several others. With the large number of possible materials and processes, there is a strong need for high quality structural data to understand correlations between processing conditions and the resulting physical properties.

Technical Strategy

1. The small sample volume of 1 μm films and the desire to characterize the film structure on silicon wafers narrows the number of available measurement methods. A unique suite of measurement techniques, Fig. 1, has been developed at NIST using a combination of SANS, XR, RBS, and FRES to determine important structural and physical property information about thin porous films less than 1 μm thick deposited on a 1 mm thick substrate. These measurements are performed directly on films supported on silicon substrates so that processing effects can be investigated.

The elemental composition of the films is determined by RBS for silicon, carbon, and oxygen and FRES for hydrogen. In both techniques, a beam of highenergy ions is directed toward the sample surface. The number of scattered particles is counted as a function of their energy. Fits are performed on the scattered peaks to compute the relative fraction of each element. The atomic composition information is necessary to calculate the relative contrast factors for x-rays and neutrons.

The XR experiments are performed at grazing incident angles on a modified to θ–2θ x-ray diffractometer at the specular condition. With the modified configuration, reflectivity fringes can be observed from films up to 1.2 μm thick. High-resolution XR is a powerful experimental technique to accurately measure the structure of thin films in the direction normal to the film surface. In particular, the film thickness, film quality (roughness and uniformity) and average film density can be determined with a high degree of precision. In addition, changes in the density profile from processing or post-application treatments can be determined. The CTE is determined from measurements of the film thickness at different temperatures.

The SANS measurements are performed at the NIST Center for Neutron Research (NCNR). Up to 10 films are stacked to increase the SANS signal and the samples are placed in vacuum without any obstructions between the sample and the neutron detector. Scattering measurements are initially performed under ambient conditions to

determine the structural characteristics of the pore structure. The scattering data are initially analyzed using a simple random two-phase description of the film, the Debye model. This model is appropriate for a class of films having random pores that makes up a majority of the samples measured. Other models are applied where appropriate such as a polydisperse collection of non-overlapping spherical pores. An additional method has been developed in which the Debye model is extended to include more complex distributions of pore sizes that need not be spherical in shape.

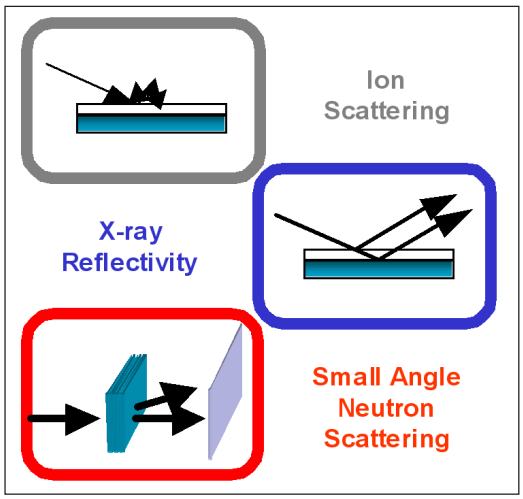

Figure 1. Three thin film measurements that are combined for complete characterization.

DELIVERABLES: Measure and report on up to 20 films for pore volume, pore size, and matrix density associated with ISMT. 3Q 2003.

2. Further developments in the determination of pore size distributions have focused on the adaptation of conventional probe molecule porosimetry methods to the NIST experimental techniques. For example, XR was done on films that have been measured in vacuum in a conventional way, and then exposed to saturated toluene vapor for several hours, Fig. 2. Capillary action fills the pores of the film. The XR critical edge where adsorption first begins gives an accurate value of the average mass density that is a combination of the walls and the solvent-filled pores. By comparing the results of the sample in air or vacuum with the toluene results, one can calculate the amount of toluene adsorbed, and hence the volume of open pores. Also, XR oscillations at higher angles provide a measurement of the total film thickness before and after exposure to toluene and gives a measure of the solvent resistance and rigidity of the walls.

The toluene infusion results confirm that the open pores of thin films can be filled by toluene supplied by saturated vapor and that XR can accurately measure the amount adsorbed. If the vapor pressure of the toluene or any other condensable solvent can be controlled at a partial pressure, standard porosimetry techniques may be applied to thin films. Data on the amount of solvent adsorption for a series of pressures could be converted to a PSD through the appropriate thermodynamic analysis.

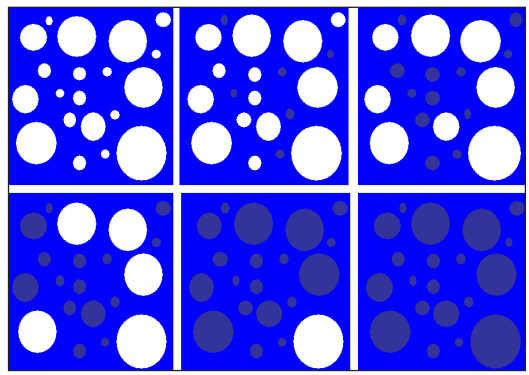

Figure 2. Schematic of the porosimetry measurement, increased solvent vapor pressure fills increased pore sizes.

DELIVERABLES: Identify strengths and weaknesses in XR porosimetry using varying methods of generating specific partial pressure environments. 3Q 2003

3. The use of deuterated and hydrogenated probe molecules enables the powerful use of contrast match methods with the SANS technique. This technique can be used for characterization of the porous thin films by filling the pores with various mixtures of toluene-h_8 and toluene-d_8. If the pores are accessible to the solvent and there are homogeneous walls, the wall density can be found. If the wall is heterogeneous, the average wall density could be found with information on the extent of heterogeneity also being possible. If closed pores exist that are inaccessible to solvent, closed pore porosity can be determined.

We have developed a combination of contrast match SANS and XR porosimetry. A match solvent mixture at controlled vapor pressures deposits the contrast match liquid in the pores through capillary action. SANS would provide an additional measure of PSD.

DELIVERABLES: Develop measurement methods and equipment for SANS contrast match technique and make measurements on IMST samples. 2Q 2003.

4. While very small pores lower the dielectric constant without significantly sacrificing electrical or physical properties, it has been speculated that a small number of very large pores or aggregated matrix material can form with sizes comparable to the film thickness. Such large "killer" defects could cause a chip to fail catastrophically and can potentially be a major source of chip rejection. Killer pores can be studied by the use of electron microscopy, but such methods cannot be used in a routine manner because the field of view of such techniques is relatively small and an extensive number of micrographs would be necessary to fully examine films. SANS, however, can sample relatively large areas of a film at once. The major difficulty is to obtain data at low enough scattering angles to reveal this information.

The Bonse-Hart-type, perfect channel-cut crystal diffractometer that came into full operation this year at the NCNR extends the measurement range of the SANS instrumentation at the NCNR by more than one order of magnitude, to over 5000 nm. This overlaps the range of the 30-m pinhole collimation SANS instruments so that together they provide continuous coverage of micro-structural features over 4 orders of magnitude (≈1 nm to >5000 nm). This new capability can be explored to identify the limits of "killer" pore detection with SANS.

DELIVERABLES: Measure and characterize pore structure development as a function of processing conditions in collaboration with Dow Chemical. 2Q 2003.

5. A practical method of transforming phase size distributions into density correlation functions and PSD's and into SANS or SAXS is being developed. Previous methods of calculating scattering from a PSD assume spherical pores, while important for a certain class of pores, are inappropriate for the majority of pore structures that are randomly interconnected. The Debye methodology assumes a random, interconnected type of pore structure, but is limited to a single distribution type. A new method has been developed to provide information on the size distributions of the pore and matrix phases based on the "chord length distribution" introduced by Tchoubar and Mering.

The transformation of scattered intensity into phase size distributions is possible by this method and has been demonstrated for bimodal distributions. Development of a computational scheme to fit data is underway.

DELIVERABLES: Develop data fitting methods for small angle scattering and present results at national meeting. 2Q 2003.

Accomplishments

- A project was completed with International SEMATECH (ISMT) in which 20 thin films have been characterized for film thickness, CTE, moisture uptake, film connectivity, pore volume, pore size, and matrix density by XR, SANS, RBS, and FRES. Quarterly reports were delivered on the results and distributed to member companies. Additional measurements were performed on specific samples for further analysis using methods such as additional SANS configurations or x-ray porosimetry.

- X-ray reflectivity measurements were used to assess depth-dependent phenomena in nanoporous thin films. Measurement of electron density profile can identify gradients in chemical composition or porosity. Measurements on low-k films exposed to either plasma or electron beam treatments show modified electron density profiles. Modeling of SXR data collected in air indicates that the film is densified near the top (air-film interface). When the film is exposed to saturated toluene vapor, an overall increase in electron density is noted due to the filling of pores with liquid toluene by capillary condensation. However, when the film is exposed to saturated water vapor, the SXR data clearly show that the topmost portion of the film fills with liquid water, whereas the lower portion remains essentially empty, indicating that the top portion is more hydrophilic. This information is vital to the screening of low-k materials because solvent uptake during processing can adversely affect device performance.

- X-ray porosimetry measurements have been implemented utilizing the controlled infusion of toluene into the open pores of a film through mass flow controllers and computer control. All of the connected open pores become filled with liquid toluene through capillary action. The critical edge measured by XR is used to calculate the total mass density and, hence, the total amount of adsorbed solvent and open pore content. This method allows calculation of the total open pore porosity that can be compared to the total combined open and closed pore porosity that is measured by the previous method that uses a combination of XR, SANS, RBS, and FRES. Further, pore size distributions may be extracted using conventional thermodynamic equations from obtained absorption/desorption curves.

■ A contrast match method using saturated solvent vapor was developed to provide an independent SANS measurement of pore volume, pore size, and matrix density as well as pore connectivity, and matrix homogeneity. The films in the SANS cell become saturated by the vapor and the pores become filled. Several solvent ratios are used and the SANS results of the saturated films along with SANS of the films in vacuum are used to calculate the exact match composition. The match composition is used to calculate the mass density of the matrix material and closed pores. This matrix density measurement is independent of the method that uses toluene infusion XR. The contrast match method offers improved accuracy of the final measured parameters. The matrix heterogeneity and the closed pore content can also be determined by the contrast match method. The contrast SANS method was further advanced by performing SANS porosimetry measurements to determine pore size distributions that may be compared with the x-ray porosimetry data.

■ The structural evolution of pore formation in low-k dielectric thin films (with a deuterated porogen) at various stages in processing was investigated using a combination of specular x-ray reflectivity (SXR) and small angle neutron scattering (SANS). SXR provides information as to the porosity and the density of the wall. SANS data show that the neutron scattering decreases during processing as the deuterated porogen degrades and pores are formed. The pore size and pore size distribution were estimated by fitting the SANS data to a structural model that describes the scattering intensity from a population of polydisperse spheres that includes hard sphere interactions between the particles and uses a Schultz distribution to describe the polydispersity. The porosity was found to decrease, while the pore size increased, during processing. A practical method of transforming phase size distributions into density correlation functions has been demonstrated. The computations are rapid and can produce density correlation functions, and hence scattered intensities to any necessary degree of accuracy. Phase size distributions other than the exponential ones described by Debye et al. can be transformed into density correlation. The transformation of scattered intensity into model phase size distributions is possible by this method.

Collaborations

Polymers Division, NIST – Hae-Jeong Lee, Christopher L. Soles, Ronald C. Hedden, Da-wei Liu, Michael Silverstein

Center for Neutron Research, NIST – John Barker, Charles J. Glinka, Derek L. Ho.

International SEMATECH – John Iacaponi, Youfan Liu

Rohm & Haas – Nick Pugliano

Dow Chemical – Brian Landes, John Lyons, Brandon Kerr, Jason Niu, Tom Kalantar

Axcelis – Carlo Waldfried, Orlando Escorcia, David Green

LG Chemicals – Minjin Ko

IBM T. J. Watson Research Center – Alfred Grill

Seoul National University – Kookheon Char, Do Yoon.

Lucent Technologies – Shu Yang

University of Michigan - David Gidley

Recent Publications

Lee, H. J., Lin, E. K., Bauer, B. J., Wu, W. L., Hwang, B. K., and Gray, W. D., "Characterization of Chemical-Vapor-Deposited Low-K Thin Films Using X-Ray Porosimetry," App. Phys.Lett., 28(7): 1084-1086 (2003)

Yang, S., Mirau, P. A., Pai, C. S., Nalamasu, O., Reichmanis, E., Pai, J. C., Obeng, Y. S., Seputro, J., Lin, E. K., Lee, H. J., Sun, J. N., and Gidley, D. W., "Nanoporous Ultralow Dielectric Constant Organosilicates Templated by Triblock Copolymers," Chem. Mater., 14(1): 369-374 (2002).

Lee, H. J., Lin, E. K., Wang, H., Wu, W. L., Chen, W., Deis, T. A., and Moyer, E. S., "Structural Comparison of Hydrogen Silsesquioxane Based Porous Low-k Thin Films Prepared With Varying Process Conditions," Chem. Mater., 14: 1845-1852 (2002).

Lin, E. K., Lee, H. J., Lynn, G. W., Wu, W. L., and O'Neill, M. L., "Structural Characterization of A Porous Low Dielectric Constant Thin Film with a Non-uniform Depth Profile," App. Phys. Lett., 81: 607-609 (2002).

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Bauer, B. J., Lin, E. K., Lee, H-J., Wang, H. and W, W-l, "Structure and Property Characterization of Low-k Dielectric Porous Thin Films," J. Electronic Materials, 30(4), p. 304 (2001).

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Lee, H. J., Lin, E. K., Wu, W. L., Fanconi, B. F., Liou, H. C., Lan, J. K., Cheng, Y. L., Wang, Y. L., Feng, M. S., and C. G. Chao, "X-ray Reflectivity Measurements of N2 Plasma Effects on the Density Profile of Hydrogen Silsesquioxane Thin Films," J. Electochem. Soc,148, F195 (2001).

Kohdoh, E., Baklanov, M. R., Lin, E. K., Gidley, D. W., and A. Nakashima, "Comparative Study of Pore Size of Low-Dielectric Constant Porous Spin-on-glass Films with Different Ways of Nondestructive Instrumentation," Japanese Journal of Applied Physics, 40, L323 (2001).

Electron Microscope Tomography of Electronic Materials

Technical Contacts:
Z. H. Levine
J. H. Scott

Goals

Enable the use of three-dimensional imaging for thick samples using commercial scanning transmission electron microscopes (STEM). Typical samples include porous low-k dielectrics, two-layer interconnect samples, and photonic band gap materials.

Customer Needs

The NTRS/ITRS has recognized the need for three-dimensional imaging of interconnects for several years. In this study, our principle objective is to determine the morphology of pores in low-k dielectric material. Two aspects of the pore distribution are critical: (a) the largest pores may lead to failure of the dielectric (e.g., short circuits), and (b) the connectivity of the pores is important to understand the transport of chemicals during the fabrication of the interconnect.

The potential solutions for interconnect are discussed in the 2001 International Technology Roadmap for Semiconductors on pages 9-10 and 24 of the Interconnect Section. "Two new measurement needs [include] the pore size distribution in porous low-k materials."

Technical Strategy

1. First, we will upgrade an existing commercial transmission electron microscope to be able to obtain high angle STEM images with a full quantitative understanding of the input and output signals. Noise reduction is also a key issue.

2. In parallel, we will develop theoretical and computational expertise for the understanding of STEM signals associated with multiple scattering of electrons.

3. We will obtain a tilt series and perform a tomographic — analysis of a photonic band gap system an artificially periodic polymer structure.

4. We will perform a similar analysis on a low-k dielectric material.

DELIVERABLES: Tomographic study of photonic band gap material. 4Q 2003

Three-dimensional images of a photolithographically patterned polymer photonic band gap material will be obtained after the STEM is upgraded.

DELIVERABLES: Tomographic study of a low-k dielectric material. 2Q 2004

The porous low-k dielectric will pose more of a challenge, particularly for alignment, because of its random nature. Hence, it will be studied second.

Accomplishments

- To date, we demonstrated the ability to obtain three-dimensional information using a scanning confocal transmission electron microscope on integrated interconnect samples several micrometers (Frigo, Levine, and Zaluzec, 2002) as well as the ability to obtain three-dimensional information on integrated circuit interconnect samples using a commercial scanning transmission electron microscope (Levine et al., 2003).

- We simulated the tomographic reconstruction using transmission electron microscopy of an 8-micrometer square sample of photonic band-gap material, see Fig. 1. This represents an order of magnitude increase in sample size compared to

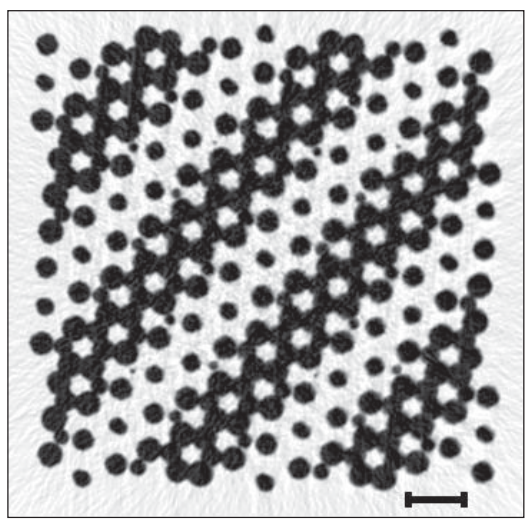

Figure 1. Tomographic reconstruction of a slice through a photonic band gap material from simulated scanning transmission electron microscope data. The scale bar is 1 micrometer, which also corresponds to the typical size of the largest samples used in TEM tomography in the scientific literature.

all TEM-based reconstructions in the scientific literature (to the best of our knowledge).

Collaborations

International Sematech, Brendan Foran, preparation of low-k samples, electron microscopy.

Lucent Technologies, Shu Yang; preparation of photonic band gap material.

Recent Publications

S, Frigo, Z. H. Levine, and N. J. Zaluzec., "Submicron imaging of buried integrated circuit structures using a scanning confocal electron microscope," Appl. Phys. Lett. **81,** 2112, (2002).

Z. H. Levine, J. A. Gao, S. Neogi, T. M. Levin, J. H. Scott, and S. Grantham, "Parallax measurements of an integrated circuit interconnect using a scanning transmission electron microscope", J. Appl. Phys. **93,** 2193 (2003).

Wire Bonding to Copper/Low-k Semiconductor Devices

Goals

The overall objective is to determine the best process method/top coating and support structures for wire bonding to copper/low-k chips. A two step gold deposition system is being developed and some thin inorganic films are also being studied as top-coating surfaces to prevent oxidation during bonding.

Customer Needs

The advent of copper metallization semiconductor chips has resulted in a requirement to wire-bond interconnect them in a manner similar to that used for 65 billion ICs. The process should be invisible to the current wire bonding machines. However, the copper bond pads oxidize, requiring a protective/bondable coating. When low-modulus low-dielectric materials lie below the pad, a support structure is necessary to prevent damage to the interconnection/dielectric layers. There are many approaches to solving these problems; the NIST program is attempting to optimize and develop new solutions where necessary.

Technical Strategy

1. One approach to protecting the copper is to coat the bond pads with a bondable gold layer. For this approach, the first objective is to determine the diffusion coefficients of copper through gold, because copper can diffuse to the surface and will oxidize, preventing a good bond. Literature values on various gold platings are contradicting and are being measured using deposits on actual damascene-process copper pads. A more classical approach, but also a more difficult process, using SIMS has been proposed. We have developed a two step (immersion + auto-catalytic gold) deposition process over the copper-low-k chips. This will be pursued at NIST. Even without the actual diffusion coefficients, a pragmatic approach is being carried out by heating gold coated samples and doing extensive wire bonding and evaluating with ball shear tests. A subset of this work will be to determine the minimum thickness of gold necessary to prevent copper diffusion/oxidation in normal bonding/processing temperatures. At the same time several inorganic coatings for protection are being evaluated. Sandia has applied thin deposited SiO_2 coatings on the copper wafers and they were evaluated. Results so far indicate that all of our coatings are nonuniform, but bonding did occur on the better pads. This evaluation is continuing, possibly by depositing a thick, uniform coating and then etching thinner.

2. Another objective is to measure the nano-hardness and modulus of the damascene copper in order to optimize bonding, [hardness should be minimized (80 Knoop to 100 Knoop)]. This has been accomplished with a series of annealing experiments made with copper chips, and pragmatically verified by actual bonding experiments. Values of measured nanohardness have been dependant on the annealing gas (argon is best) and have been as low as 60 GPa (about 120 unannealed) and the modulus as low as 20 GPa.

Problems have occurred when sawing the bare copper chips in which the saw particles stick to the bare copper. several approaches to curing this problem have been pursued. Copper damascene process samples have been supplied by International SEMATECH for this effort.

DELIVERABLES: Problems with the two-step gold deposition will be solved. Some pad lifting during gold deposition will be studied and an understanding obtained. The desired thickness of gold deposition will be determined, and hardness and modulus studies completed. A nickel strike coating also was developed.

Accomplishments

- One paper published, entitled "Wire Bonding To Advanced Copper-Low-K Integrated Circuits, the Metal/Dielectric Stacks, and Materials Considerations," by George G. Harman and Christian E. Johnson, Proc. 2001 IMAPS Symposium, Oct 9-11, 2001, Baltimore, MD, pp. 484-491. This paper won an award as an outstanding paper in the Symposium. An updated version of this was published in the IEEE Transactions on Components and Packaging Technologies, V-25, Number 4, Dec. 2002, pp. 677-683.

- The two step non-contact gold deposition process used on some of the original International SEMATECH (ISMT) wafer copper were etched in our processing, whereas other copper deposition methods were satisfactory and bonded well. Currently, wafers from another source with thicker copper are being acquired.

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Solders and Solderability Measurements for Microelectronics

Technical Contacts:
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Maureen Williams
Christian Johnson

"As a result of NIST's involvement, I feel NEMI has been successful in responsibly leading the effort to understand the implications of lead-free assembly in a way that is benefiting the entire electronics assembly industry."

— Edwin Bradley, Motorola and National Electronics Manufacturing Initiative

Goals

Solders and solderability are increasingly tenuous links in the assembly of microelectronics as a consequence of ever shrinking chip and package dimensions, the broadening use of flip-chip technology, and the movement toward environmentally friendly lead-free (Pb-free) solders. To support needs in this area, the goal of this project is to provide data and materials measurements of critical importance to solder interconnect technology for microelectronics assembly.

Customer Needs

The U.S. microelectronics industry has clearly articulated measurement needs for solderability and assembly, especially for Pb-free solders. For example, the urgency for materials data for Pb-free solders has been specified in the 2000 IPC Lead-Free Solder, 2001 ITRS, and 2002 NEMI Roadmaps. Pressure from the European Union and the Japanese consumer product market to produce lead-free microelectronics continues to increase. These industrial needs are addressed under this NIST project.

Additional needs have been identified through participation in the National Electronics Manufacturing Initiative (NEMI) working group on Pb-free solder alloys. It was learned that significant industrial problems had arisen due to contamination of Pb-free solders by the Pb contained in the protective solder coatings that are used on copper (Cu) leads. The protective layer deposited on Cu is usually referred to as a "pretinned" coating and is required to maintain solderability of the component during storage prior to assembly. Pb-free coatings of nearly pure tin (Sn) tend to grow "whiskers," however, which can cause shorts across leads. Thus the development of Pb-free alloy platings to replace Pb-containing protective layers is considered important, and tests which ascertain the tendency to form whiskers are much needed. NIST is a co-chair in the NEMI Sn Whisker Modeling Group and an active participate in the NEMI Accelerated Sn Whisker Test Group.

In the 2001 ITRS, Table 74 on page 321 "Assembly and Packaging Difficult Challenges," the need for Pb, Sb, and Br free packaging materials is specifically mentioned. In the 2002 NEMI Technology Roadmaps, Technology Designs, Environmentally Conscious Electronics, page 9, states "The NEMI Pb-Free Assembly and Rework Project is leading the North American effort to develop a lead-free second level assembly process utilizing current manufacturing equipment technology." In the Manufacturing Technologies, Board Assembly, on page 2, it states "In Transition to Pb-free production, it is important to understand the long-term reliability performance of Pb-free and eutectic solder joints."

Technical Strategy

We are providing the microelectronics industry with measurement tools and data to address solder interconnect problems. For example, a thermodynamic database has been publicly distributed for modeling the processing behavior of lead-free solder systems. We also work closely with industry groups on measurement tools needed for development of lead-free solders for use in harsh environments, and provide guidance for adoption of these solders into assembly processes through work with industrial standards organizations.

We will continue working with NEMI to establish suitability of particular lead-free solder compositions. In addition, solderability tests will be developed working with the IPC lead-free solder sub-committee. Databases for phase diagrams and thermodynamics critical to solder development and for mechanical properties of solder will be expanded and distributed via the web. In addition, a much-needed guide to interpretation of thermal analysis data will be produced.

It is well known that the use of pure Sn protective deposits has serious problems. Sn whiskers (filament type whiskers are typically 1 μm diameter and several mm long) can grow from the Sn plate and cause electrical shorts and failure. An example of a Sn whisker is shown in Fig. 1. Historically, Pb was added to Sn plate to prevent whisker growth as well as to lower cost. In the current research program, it was decided to focus this project on Pb-free Sn-rich deposits with alloying additions that would retard whisker formation. The Sn-Cu system was chosen for the surface finish, since

Sn-Cu-Ag is likely to be the Pb-free bulk solder of choice for industrial application. The basic idea is that the substitution of a different solute for Pb in the Sn-rich deposit will also retard whisker growth. A detailed micro-structural comparison of deposits with high and low whiskering tendency is being conducted. Sn grain size, shape, preferred orientation and residual stress will be measured. The dominant mechanism(s) for whisker growth will be determined.

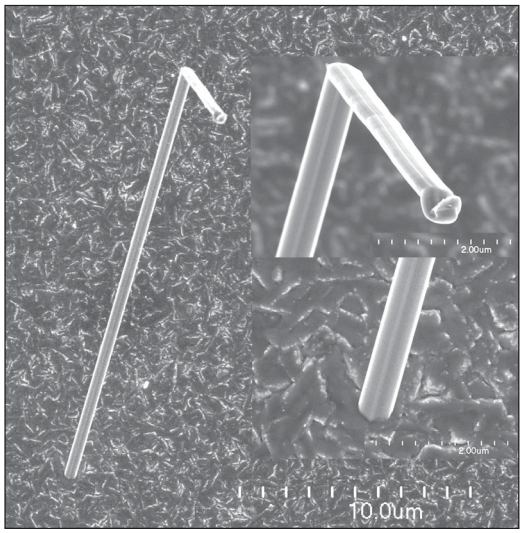

Figure 1. Typical whisker growing from electrodeposited tin surface.

DELIVERABLES: Perform wetting balance tests for the IPC solderability task group pilot study on Pb-free surface finishes and components. 4Q 2003, IPC solder study).

DELIVERABLES: Expand pages for phase diagram Metallurgy Division Webbook with emphasis on solder alloys. Add pages for constituent binary and ternary systems containing Sb. 3Q 2003.

DELIVERABLES: Perform x-ray and SEM analysis on electrodeposits for the NEMI Modeling Group to determine factors that influence Sn whisker propensity. 4Q 2003.

DELIVERABLES: Make simple phase equilibria software available for interactive use; make more complex programs available for downloads. 4Q 2003.

DELIVERABLES: Prepare draft Best Practice Guide for Differential Thermal Analysis. 4Q 2003.

Accomplishments

- NIST has taken a major role working with industry through a NEMI Task Force to identify and move Pb-free solders into practice. NIST co-chairs the NEMI alloy selection group that selected standard alloy compositions for U.S. microelectronics assembly.

- NIST has developed the database necessary to calculate multicomponent phase diagrams essential for Pb-free alloy development. The experimental determination of phase diagrams is a time-consuming, costly task requiring expert interpretation of results. The calculation of phase diagrams significantly reduces the effort required to determine phase evolution in multicomponent systems and can provide quantitative information that is frequently needed in other modeling efforts. During the past year antimony (Sb) containing systems were added to the current NIST thermodynamics database. This expands the applicability of the database to a wider range of solder alloys.

- An easy-to-use interface for phase equilibria software for the calculation of liquidus temperature, lever rule equilibrium and Scheil solidification has been developed.

- We are also working in collaboration with IPC Standards Committees (most closely with members from Celestica, Lucent, Raytheon, Rockwell, and Shipley-Ronel) to establish reproducible solderability test standards for board level assemblies. Activities include providing benchmark experiments for the wetting balance tests to predict on-line solderability for a wide range of surface finishes, lead materials, and solder alloys.

New NIST research to develop an understanding of whisker formation in Sn-based, Pb-free electroplated surface finishes complements the solderability studies. NIST is a co-chair in the NEMI Sn Whisker Modeling Group and an active participate in the NEMI Accelerated Sn Whisker Test Group.

A plating cell using a rotating cathode was used to control the hydrodynamic conditions during the electrodeposition of Sn and Sn alloys. We have characterized the grain size, and surface topography of Sn and SnCu coatings on a variety of substrates (amorphous carbon, vapor deposited Cu and electroplated Cu and Sn). Residual stress measurements are ongoing using the cantilever beam technique.

High purity bright Sn electrolytes were prepared using 18.3 Mohm-cm water. Controlled amounts of Cu were added to the Sn electrolyte. It was found that even trace levels Cu in Sn plating bathes have been identified as a contributory factor to

the propensity of tin whisker growth in electroplated deposits.

In collaboration with NEMI and TMS, NIST co-sponsored a full day workshop on Tin Whisker Formation in Microelectronics for industrial and academic participates at the TMS meeting held in San Diego, CA on March 2, 2003.

Collaborations

IPC; development of solderability test procedures

National Electronics Manufacturing Initiative; Lead-free solders and reliability.

TMS, The Minerals, Metals & Materials Society; workshop sponsor with NIST and NEMI

Recent Publications

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Interconnect Materials and Reliability Metrology

Goals

The objectives of this project are: (1) to develop experimental techniques to measure the reliability-related properties of thin interconnect conducting and insulating films, including basic tensile properties, elastic modulus by both static and dynamic means, residual stresses, fatigue, fracture resistance, and electromigration and stress-voiding resistance, in specimens fabricated and sized like materials used in actual commercial devices; and (2) to advance the ability to anticipate and meet thin interconnect reliability challenges by relating thin film reliability to microstructure and by developing understanding of the relationships between various modes of thin film failure, for example, electromigration and mechanical fatigue.

Customer Needs

Thin films are an essential component of all advanced electronic devices. Interconnect structures built up on ULSI microchips consist of 7 thin-film layers now, and will soon reach 10 layers (*International Technology Roadmap for Semiconductors, 2001*, *Interconnect, Table 62a*). These structures are fabricated using adjacent layers of materials with very different thermal expansion coefficients, exotic materials such as nanoporous low-k dielectric, and operate at ever higher temperatures. According to the *Roadmap (2001)*, *Interconnect, p. 23, "Computer-aided design (CAD) tools will need to incorporate contextual reliability considerations in the design of new products and technologies. It is essential that advances in failure mechanism understanding and modeling, which result from the use of improved test methodologies, be used to provide input data for these new CAD tools. With these data and smart reliability CAD tools, the impact on product reliability of design selections can be evaluated."* The National Electronics Manufacturing Initiative (NEMI) Roadmap of December 2000 reports a similar need. A section on pages 227-228 entitled *"Key Simulation Prerequisites"* states that *"Laboratory infrastructure/experimental expertise is essential for both model verification as well as property input evaluations, to have truly effective simulations."* A following subsection lists critical simulation areas. Listed first is *"Reliability-Mechanics-Physics of Failure (POF), and associated Mechanical Analysis and Design."* The message is clear: understanding and modeling of mechanical performance and potential failure modes in these devices require knowledge of the mechanical behavior of the films. This issue of mechanical modeling is likely to increase in significance with the growing integration of interconnect between the chip and the package, with their disparate material sets.

Because the films are formed by physical vapor deposition or spin-on deposition, their microstructures, and hence their mechanical properties, are quite different from those of bulk materials of the same chemical composition. While the general principles of conventional mechanical testing are applicable to thin films, conventional test equipment and techniques are not. Because vapor-deposited films are of the order of 1 μm thick, the failure loads are of the order of gram-forces or less, and the specimens cannot be handled directly. So, techniques specific to films on silicon substrates are needed. Developing test methods must eventually become applicable to test structures that can be included in production or development wafers, so that applicability to 'real' materials can be demonstrated. The intent of our goal of testing specimens similar in size to structures on actual production devices is to maximize the relevance of our results.

Radically different materials and material technologies are being considered for future ULSI devices, as the further development of leading-edge lithography increases in const and complexity. An example of a radically new material is the carbon nanotube. An example of a new material technology is self-assembly. Effective use of these new materials systems will require significant extension of the reliability metrology and analysis toolset, to understand and address new kinds of reliability issues. The NIST laboratory research programs, which back up the near-term metrology developments described here, are beginning to develop experimental and analytical techniques to address these challenges; NIST management is encouraging these developments through the new strategic focus area in nanotechnology.

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R. R. Keller
M. Gaitan

"A microtensile methodology, developed at the National Institute for Standards and Technology, has been adopted and applied in Motorola to evaluate material properties of thin films. This methodology is a significant part of the materials technology development at Motorola."

Betty Yeung, David Read, Yifan Guo, Bill Lytle, and Vijay Sarihan (Motorola AISL, Tempe, AZ), "Microtensile Methodology for Mechanical Characterization of Thin Films," Solid State Technology, June 2002, p. 125.

Technical Strategy

We are developing a variety of measurement techniques to provide material property data on interconnect materials. In testing and exercising these techniques, we develop data that are valuable in themselves, and we also develop our understanding of the relationship between the observed behavior and the microstructure, as influenced by processing conditions specific to the specimen material at hand.

We study individual thin films and multilayer interconnect structures on silicon substrates, both obtained from industry and fabricated by researchers within NIST and elsewhere. Specimens of CMOS structures have been obtained through the MOSIS service run by UCLA (Fig. 1). Occasionally, wafers or fabricated specimen geometries are received directly from our counterparts in industry. Some of our techniques require the removal of the silicon substrate beneath the test structure itself, to a depth of up to 50 µm. We have developed dry etching systems that use xenon difluoride to carry out these processes.

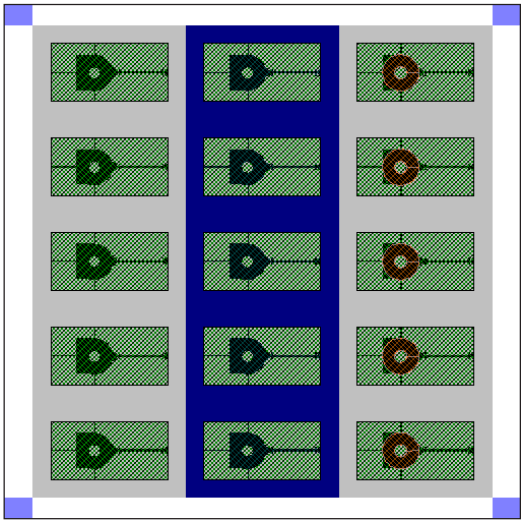

Figure 1. Test chip produced in the 1.2 µm AMI CMOS process available through the MOSIS service.

Measurement capabilities operating within this project include microtensile testing, d.c. and a.c. electromigration measurements, and resonant structure measurements. We have developed the silicon-frame tensile specimen and the piezo-actuated tensile tester, which operate successfully for specimens 100 µm wide and larger. Because problems were encountered with specimens narrower than 100 µm, a new technique, called the force-probe tensile test technique, has been developed. The apparatus includes a tensile loading system operable within the scanning electron microscope (SEM). This system has now been used on specimens as small as 2 µm wide. It is anticipated that the magnification of the SEM will allow testing even narrower specimens.

We have begun an effort on electrodeposited copper, including specimens from industrial colleagues and produced in-house, to characterize the variability of the mechanical behavior of electrodeposited copper with deposition conditions, film thickness, annealing, and other relevant variables.

Our measurements involving alternating current stressing of chip-level interconnects are used to explore the relationships between electrical and mechanical reliability. High current density a.c. signals are run at low frequencies through Al- and Cu-based electromigration structures in either passivated or unpassivated states. Joule self-heating results in a cyclic strain due to thermal expansion mismatch between the metal lines and their substrates. The associated deformation then leads to severe topographic distortions in the lines, and can eventually cause open circuit failure. We investigate the effects of current density, frequency, crystallographic orientation, and encapsulant material.

We have begun an effort this year, with the NIST Metallurgy Division, to address reliability of advanced interconnect materials with linewidth less than 100 nm. In addition to the challenges associated with electrodeposition into extremely narrow trenches, we expect significant influences of the interconnect sidewalls on electrical resistivity and possibly on electromigration resistance.

We are also developing non-contact optical methods to measure mechanical properties of thin films and interconnects using MEMS test structures that are compatible with the CMOS process. Such non-contact methods may be useful in monitoring the variations of mechanical properties in the production environment. A method has already been developed to measure the residual strain in the passivation and interconnect films using fixed-fixed beams. We are currently developing resonant measurements for cantilever beams to characterize the elastic modulus of each layer (Fig. 2).

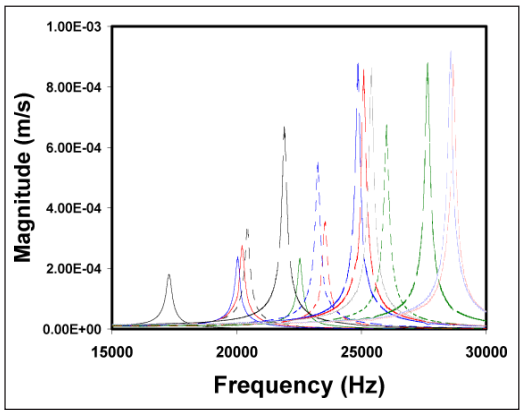

Figure 2. Resonant frequency response of micromachined CMOS cantilever test structures.

The method is based on the fact that the resonant frequency of the cantilevers is related to their elastic modulus, density, and the geometry. They can be fabricated with different combinations of layers and then comparisons of the resonant frequency can be used to extract the modulus of the individual layer. The cantilever test structures can be fabricated simultaneously with the fixed-fixed beams used to measure residual strain and strain gradient. With the residual strains, from the fixed-fixed beam method, and the elastic constant, from the resonant method, the residual stress and its gradient can be calculated.

DELIVERABLES: Our results are being disseminated in conference presentations and peer-reviewed articles in archival journals, as well as in presentations and written reports to the organizations that have supplied specimens.

Design and fabricate a test chip with improved cantilever test structures; develop method to determine elastic modulus from resonant frequency measurements.

Conduct electrical tests on electrodeposited copper lines of width 100 nm or less. 4Q 2003.

Accomplishments

Progress in recent years on measurements of the mechanical behavior of thin films has put us in the position of starting to be able to make various kinds of critical comparisons among our results: results for the same materials in different laboratories; results for similar materials from different sources; and results for the same property by different measurement methods. These comparisons are necessary to reach our goals of providing accurate and believable measurement techniques and an understanding

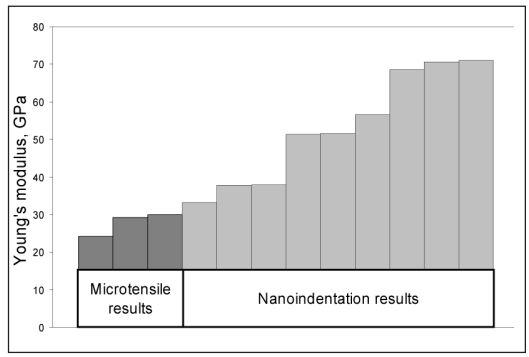

Figure 3. Comparison of Young's modulus obtained from nanoindentation and microtensile tests.

of the results. This year we obtained nanoindentation results on a previously tested aluminum film and on thick copper films from an outside collaborator. From the nanoindentation load-displacement data, we deduce Young's modulus and yield strength of the material in a very small volume deformed by the nanoindenter tip. The results obtained from nanoindentation scatter widely in both Young's modulus and yield strength for electron beam-evaporated aluminum; both values are consistently higher than those obtained from microtensile tests (see Fig. 3). This problem of scatter between nanoindentation and microtensile results is typical in such comparisons. Nano-indentation results for polyimide were also higher than microtensile results, but with less scatter. Work is continuing with other materials and understanding the causes of the scattering. The measurements on the thick copper films, analyzed using plastic-zone-sized deduced from AFM images, gave a good correlation with the micro-tensile results shown below.

DELIVERABLE: The collaborative study on copper has been presented at a technical conference and submitted for publication in a technical conference proceeding.

A key experimental tool for understanding the sources of mechanical weakness is fractography of broken specimens. A new scanning electron microscope, with a field-emission source and an in-lens detector, is allowing us to obtain very clear images of the fractures surfaces of microtensile specimens. An example is shown in Fig. 4. This aluminum CMOS contact metal had low elongation, and variable tensile strength with some very low values.

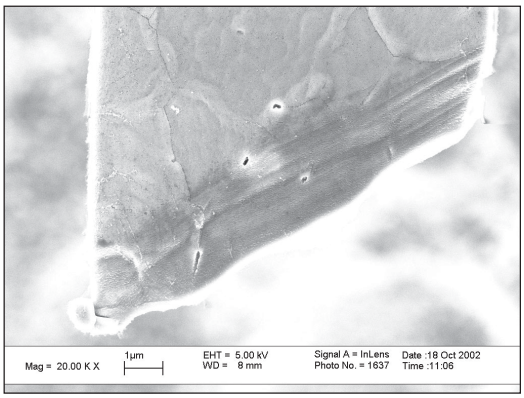

Figure 4. Fracture surface of tensile specimen of CMOS contact metal obtained through the MOSIS service.

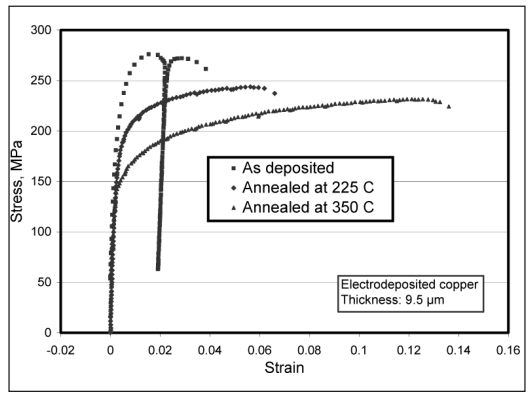

Figure 6. Typical stress-strain curves for annealed and as-deposited films, obtained by tensile testing.

Recently, we have been working to demonstrate the applicability of these techniques to materials recently introduced in the microelectronics industry, specifically copper, in the form of both sputtered thin films and thick electrodeposits. A microtensile specimen of electro deposited copper is shown in Fig. 5. We typically find that the strength values are far above the handbook values for pure annealed bulk copper, and the elongations are much lower than the handbook values. Increasing the film thickness from, for example, 1 to 10 µm, increases the ductility from around 1 % or less to 5 % or more. Annealing also changes the tensile properties markedly, as shown in the stress strain curves (Fig. 6). The changes with annealing are qualitatively as expected. The differences between the thin sputtered film and the thick electrodeposited film are generally consistent with trends seen for other thin film materials.

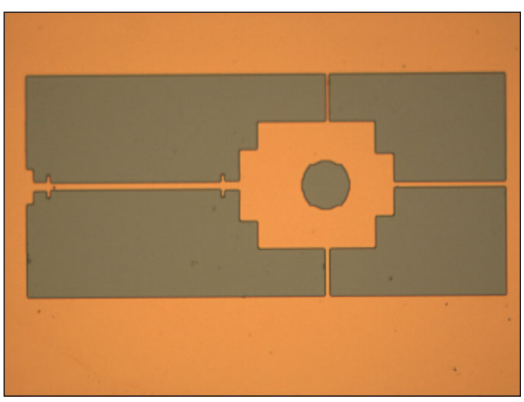

Figure 5. Microtensile specimen of electrodeposited copper produced at NIST. The slender strip on the left is the test section; the tab with the hold is used for loading. The grip section is 10 µm wide by about 200 µm long.

The demonstrated applicability of the force-probe technique to a variety of specimen materials and temperatures leads us to think that this technique and its complementary specimen geometry may become a standard method for microtensile testing.

Our a.c. tests continue to reveal damage phenomena drastically different from that observed in conventional d.c. electromigration tests. Last year, we reported observations of slip-induced surface offsets likely due to classical dislocation activity. TEM experiments will confirm the role of dislocations, and we expect to begin such experiments later this year. We have pursued crystallographic mapping experiments within a field emission SEM this year instead, due to the generous amount of information that can be obtained with such an approach. What has become apparent is the tremendous variation in behavior from grain to grain. We have observed significant growth of selected grains in a polycrystalline interconnect, which subsequently become more susceptible to surface offset formation with further cycling (Fig. 7). Accompanying such grain growth is a re-orienting of some grains, into a more accommodating orientation for slip activity. In other words, grain re-orienting seems to provide a larger resolved shear stress on a particular grain. Many factors interact to control the processes leading to catastrophic failure by open circuit, at a site where the interconnect cross section has decreased very significantly due to deformation. We are attempting to construct a model describing the roles of these factors, including strength of individual grains (grain size), ease of slip within individual grains (grain orientation), and prevalence of dislocation sources (grain boundary structures, surrounding grain constraints). The

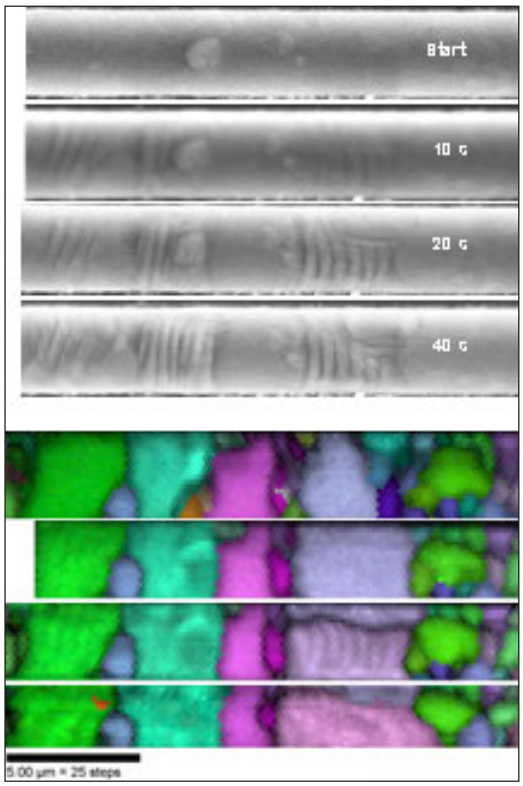

Figure 7. Quasi in-situ a.c. testing sequence in Al-1Si, showing development of surface offsets and accompanying grain growth after 0, 10, 20, and 40 seconds of a.c. cycling at approximately 12 MA/cm^2. Top four images obtained by secondary electron imaging. Bottom four images from same locations, obtained by automated electron backscatter diffraction.

end goal is to offer a scheme for predicting where an open circuit should be expected, given the initial grain structure of the interconnect.

Because it is sometimes impossible to get films of individual materials with the interconnect stack in a chip that goes through a normal manufacturing process, we are studying measurement methods that use composite laminate specimens that include several materials, such as metal and dielectric. The elastic modulus of the individual films in the laminate is to be determined by differences between the resonant frequencies of beams with different combinations of metal, dielectric, and polysilicon. A model has been developed for a composite cantilever beam. Preliminary measurements indicate that this technique can provide accurate values of the different layers in the interconnect structure, as well as insight into the behavior of the structure as a whole (see Fig. 8).

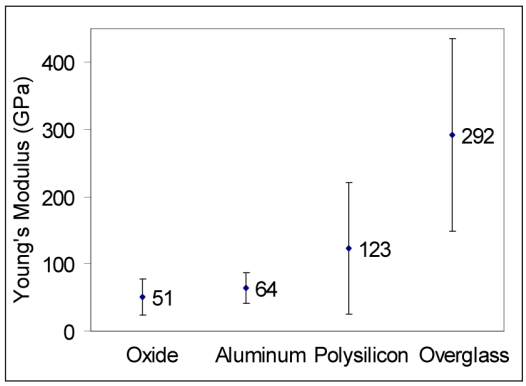

Figure 8. Elastic modulus of CMOS thin films extracted from the cantilever resonant frequency measurements.

Collaborations

Max-Planck-Institut für Metallforschung, Stuttgart, Germany, Prof. Eduard Arzt, Dr. Cynthia Volkert

Intel Corp., Chandler, AZ, Dr. Richard Emery

Motorola, Inc., AISL, Tempe, AZ, Betty Yeung, and MATC, Schaumburg, IL, Dr. Andrew Skipor

MOSIS Integrated Circuit Fabrication Service, 4676 Admiralty Way, Marina del Rey, CA, Dr. Tom Veriner.

Recent Publications

Keller, R. R., Mönig, R., Volkert, C. A., Arzt, E., Schwaiger, R., and Kraft, O., "Interconnect Failure due to Cyclic Loading," *Proceedings of the Sixth International Workshop on Stress-Induced Phenomena in Metallizations*, S. P. Baker, M. A. Korhonen, E. Arzt, and P. S. Ho, Eds., American Institute of Physics Conference Proceedings Vol. 612, pp. 119-132, Melville, NY (2002).

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Shuman, Shivesh, Gaitan, Michael, Joshi, Yogendra, and Harman, George, "Wire Bond Temperature Sensor," IMAPS 2001 Symposium, Baltimore, MD, October 7-11, 2001.

Yeung, B., Read, D. T., Guo, Y., Lytle, W., Sarihan, , V., "Microscale test technique and results for aluminum thin films," accepted for International Mechanical Engineering Conference and Exhibition, November 2001.

Recent Presentations

Geiss, R. H., Roshko, A., Bertness, K. A., and Keller, R. R., "Electron Backscatter Diffraction for Studies of Localized Deformation," Mike Meshii Symposium, TMS, forthcoming (2003).

Read, D. T., Geiss, R., Ramsey, J., Scherban, T., Xu, G., Blaine, J., Miner, B., Emery, R. D., "Nanoindentation and tensile behavior of copper films," 2003 Materials Research Society Spring Meeting, San Francisco, CA, April 21-25, 2003.

Read, D. T., McColskey, J. D., and Cheng, Y.-W., "Microtensile Testing of Thin Films in the Optical and Scanning Electron Microscopes," International Conference on Characterization and Metrology for ULSI Technology, Austin, TX, March 24-28, 2003 (poster presentation).

Read, D. T., "Interconnect Materials And Reliability Metrology," Government Microcircuit Applications & Critical Technology Conference 2003, Tampa, FL, March 31-April 3, 2003.

Mönig, R., Orso, S., Volkert, C. A., Keller, R. R., and Arzt, E., "AC-Induced Damage in Cu Interconnects," Materials Research Society Spring Meeting, San Francisco, CA, April 1-5, 2002.

Keller, R. R., Mönig, R., Volkert, C. A., Arzt, E., Schwaiger, R., and Kraft, O., "Interconnect Failure due to Cyclic Loading," Sixth International Workshop on Stress-Induced Phenomena in Metallizations, Ithaca, NY, July 25-27, 2001. (INVITED)

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Thermal Measurements and Packaging Reliability

Goals

The goals of this project are to:

a) Provide the micro-electronics packaging industry with information, guidance, and tools through technology transfer to characterize the behavior of features and interfaces in packaging that are thermally stressed. Information and guidance are provided directly to individual companies and to consortia through collaborations whereby we are provided with specimens, which present a reliability concern to the manufacturer or end-user. The results of the tests are reported to the provider, and are typically reported in the general literature or at technical meetings. This system contributes toward achieving our third and primary goal—providing the industry with the tools to characterize these thermomechanical behaviors. Review and evaluation of the techniques by our industrial collaborators allows us to refine the techniques to make them optimally beneficial to industry and to demonstrate to the industry at large the capabilities of the techniques on actual packages in development, essential for technology transfer.

b) Develop and evaluate methods for measuring temperatures at and within the chip-level for the purposes of determining *in situ* material thermal properties (e.g., thermal properties of interlayer dielectrics), device performance (e.g., SOI devices), and for evaluating the thermal performance of new architectures and technologies (e.g., 3D integration and innovative cooling methods for high performance logic).

Customer Needs

The trend in electronics is toward components of higher density and smaller size using less expensive materials. Materials used in packaging are many and display a variety of thermal responses that are not always compatible. This makes interfaces particularly vulnerable to thermomechanical fatigue failures. The program seeks to offer support and verification of models conducted or sponsored by the microelectronics industry. Development of measurement techniques allowing observation of the package throughout the thermal cycling is done so that one can identify the locations and materials in which deformations are occurring.

The physical size of nearly all electronic devices is decreasing rapidly and, at the same time, their capabilities are increasing dramatically. One move in this direction is the advent of integral passive components and another is the increasingly prevalent use of organic (polymeric) conductors and fillers. These organic materials have a large coefficient of thermal expansion, which can reduce the reliability of electronic packaging systems. We are investigating interfaces between organic materials and between organics and metals to determine the initiation of damage and failure mechanisms in these material systems.

Temperature measurements for microelectronic devices are more important today than they ever have been. It has always been true that extreme temperature places limits on the operating range of nearly all devices, but today, increasing power dissipation and power densities threaten to create temperatures that block continued progress according to 'Moore's Law.' Clearly, new and innovative methods for cooling chips and packages must be found along with new materials and circuit designs, and architectures for decreasing the power dissipation and operating temperature. Equally as clear, we must have accurate and well-understood methods for measuring the temperature of devices to aid in the development of these new techniques and materials.

"Packaging cost is a second area that could be an obstacle to realizing the potential of advances in silicon technology. …the average packaging share of total product cost will double over the next 15 years and, more significantly, the ultimate result will be greatly reduced gross profit margins, limiting investments in R&D and factory capacity." 2000 NEMI Roadmap

The maximum junction temperatures for chip operation are shown in tables 75 a and b of the ITRS Assembly and Packaging section. The criticality of knowing thermal properties of materials and devices is discussed on page 8 of the Assembly and Packaging section, page 25 of the Metrology section, and page 19 of the Interconnect (Reliability) section. Validated thermal models are discussed on page 25 of the Metrology section.

Technical Contacts:
A. J. Slifka
E. S. Drexler
D. L. Blackburn
A. R. Hefner

"The task of dissipating the heat from integrated circuits while maintaining acceptable junction temperatures has been a significant challenge for semiconductor and system manufacturers."

". . . .We continue to push the cooling and mechanical limits of electronic products. Complete thermal and mechanical modeling, validated with measurements, is needed."

2001 International Technology Roadmap for Semiconductors

Technical Strategy

1. Our established programs in infrared (IR) (thermal) microscopy and electron-beam moiré, and our developing techniques in scanning thermal microscopy, utilizing the AFM (atomic force microscope), have much to offer the microelectronics industry. We have been approached by industry with requests for aid as simple as "How high are the temperatures in this MCM (multichip module) during service" to as challenging as "What are the strains in the on-chip tungsten vias under thermal loading." The first was answered using the IR microscope; the second has yet to be answered.

We have just completed our third year of applying thermal conductivity measurements using the IR microscope to the problem of packaging reliability and have engendered great interest from the Advanced Embedded Passives Technology (AEPT) Consortium. As thermal conductivity measurements are one of the most sensitive indicators of metal purity, likewise they are one of the most sensitive indicators of interfacial integrity. A minute decline in interfacial thermal conductivity is the first indication of the microcracks and fissures that may ultimately result in failure.

DELIVERABLES: Quantitative measurements of industrial specimens from AEPT using thermal SPM, laser-heated IR microscopy, and Joule-heated IR microscopy. 4Q 2003

2. The electron-beam moiré technique offers a unique capability. Unlike moiré interferometry, it can quantify strain in the different materials at both low temperatures and at high temperatures. It measures thermally induced strains representative of those experienced by the package in service, rather than residual strains due to processing. In addition, it can quantify the accumulation of plastic strain during thermal cycling, and it is clear from the images in which materials the strains are occurring. The technique is designed to look at strains on a local scale, but is flexible enough to allow comparison of those local strains at multiple locations across the cross section.

DELIVERABLES: The results of a collaboration with the Jet Propulsion Laboratory were presented at the Fifth Annual Microelectronics Reliability and Qualification Workshop. 1Q 2003

3. Work continues with the AEPT on the embedded resistors. A second test vehicle has been sent to NIST for strain measurements for embedded resistors that have different sizes and layouts. Two resistor sizes for each of two layouts will be compared.

DELIVERABLES: Electron beam moiré measurements of next-generation embedded resistor specimens from the AEPT consortium. 3Q 2003

4. Thermal microscopy and electron-beam moiré are complementary techniques, each supplying pieces to the puzzle of how failure occurs. Combining the data from both techniques will yield a complete picture of thermomechanical fatigue.

DELIVERABLES: Analyze and report IR microscopy, SPM thermal microscopy and electron beam moiré data from next generation embedded resistor specimens. 4Q 2003

5. As the size of packages gets smaller, heat removal becomes a more significant problem. The SPM is being used to develop a technique to measure thermal conductivity of thin films for application first to metal interconnect lines. The technique will also be able to measure interfacial thermal resistance between materials. The theoretical work on this development is being done in collaboration with Dr. Kevin Cole of the University of Nebraska.

DELIVERABLES: Report via the literature, on measurements of a model film, such as gold or diamond-like-carbon. 4Q 2003

6. The reasons for desiring to know the operating temperature of a semiconductor device can be divided into the following four broad categories:

- Predict reliability or operating life of device
- Measure material/device thermal properties in-situ
- Confirm or determine the operating limits or thermal performance of a device
- Validate thermal models for chip and device performance.

A broad range of temperature measurement techniques will be investigated. These will include:

- Electrical techniques that use temperature sensitive device and material parameters (such as junction voltages, threshold voltages, and resistivity) as thermometers, optical techniques such as infrared thermal emission, micro-Raman spectroscopy, and reflectance, and micro-probes based upon AFM systems.

DELIVERABLES: Complete modeling of buried interconnect system thermal performance. 3Q 2003

Develop and fabricate test structures for interconnect thermal metrology. 2Q 2004

Demonstrate temperature measurements of buried interconnect lines. 3Q 2004

Develop procedure for coating chips with thin high emissivity paint and characterize the performance for high speed IR thermal metrology. 4Q 2003

Develop transient thermal IR metrology calibration test chip using micro hotplates. Demonstrate temporal and spatial calibration procedure. 3Q 2003

Apply transient IR test system to develop gas sensor temperature BIST. 4Q 2003

Accomplishments

■ Thermal measurements have continued on three similar embedded resistor specimens. One specimen each is being measured using laser-heated IR microscopy, Joule-heated IR microscopy, and thermal SPM. Upon completion of thermal cycling and testing, results will be analyzed and the techniques compared. A single crack appeared in one of the three similar specimens after 11 thermal cycles, but failure has not occurred yet. All three specimens have been thermally cycled 18 times and data analysis has begun. Figure 1 shows a thermal image from the SPM and accompanying temperature profile data used in the analysis. The y-axis scale of the temperature profile corresponds to 8 ºC.

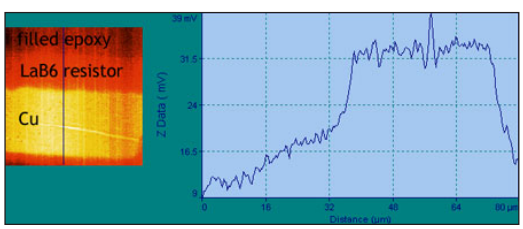

Figure 1. Thermal SPM image and temperature profile of an industrial integral resistor specimen.

■ Electron-beam moiré tests have been completed on three of four specimens from DuPont comparing the strain fields in a printed circuit board containing ceramic resistors of various sizes and layouts during thermal cycling. Figure 2 shows electron-beam moiré images from two specimens with the same layout, but with different sized resistors taken at 177 °C.

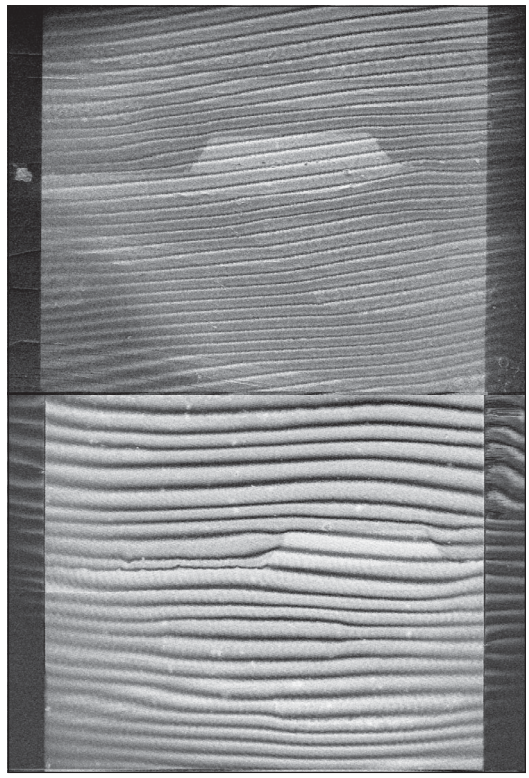

Figure 2. Moiré images at 177 °C from small and large sized resistors with the same layout.

■ In a collaboration with the Jet Propulsion Laboratory (JPL), the effect of a microwave process on solder bump reliability was studied. The program looked at the differences in strain in solder bumps that have been processed before thermal cycling, and a control set that were not be processed.

■ Development of a technique for measuring the thermal conductivity of thin films using the SPM has begun. Most films used in electronics and electronic packaging are so thin that a measurement using even the thermal SPM would be primarily a measurement of the substrate material. With collaboration from Dr. Kevin Cole of the University of Nebraska, work has begun on a theoretical treatment of the data to allow measurement of thin films and the interfacial thermal resistance between the film and substrate. One application for this technique is measurement of thermal properties of interconnect lines. Measurements have begun using a model system, gold films of various thickness evaporated onto glass substrates. Figure 3 shows the imaging contrast available with the technique.

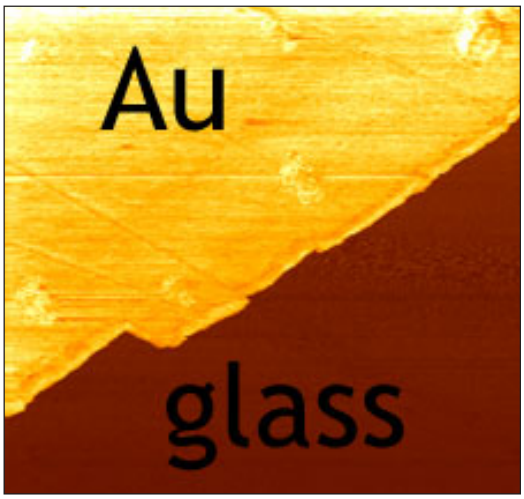

Figure 3. Thermal SPM image of a 200 nm thick gold film on glass.

■ We have been approached by Cenymer Corporation to make thermal and other measurements on a diamond-like-carbon coating that they manufacture. Since the coating is typically around a micron thick, the thermal SPM is a good tool for this measurement. Cenymer is also interested in interface materials to allow adhesion of diamond-like-carbon coatings to various substrates. This work fits well with our thin-film research, providing specimens with different, controlled interfaces to help solve the problem of analyzing thermal data on thin films and even thinner adhesion layers.

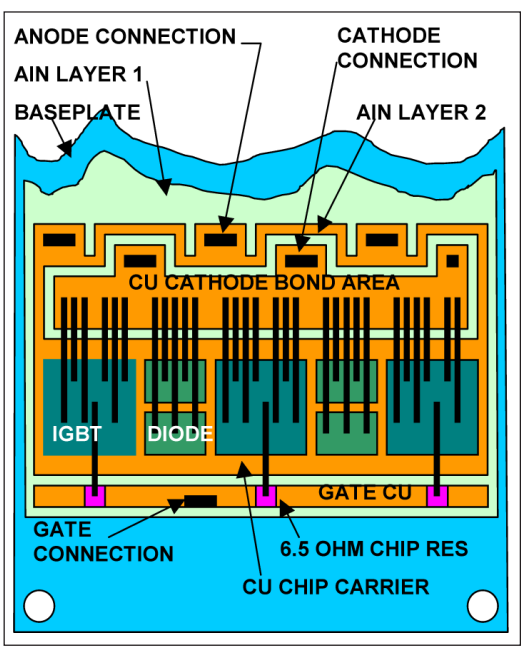

Figure 5a. Drawing of the layout of the IGBT chips within the module. and b) the vertical structure from one of the chips to the baseplate of the module.

■ We have developed a method to measure the high speed heating response of Insulated Gate Bipolar Transistors (IGBTs) packaged in high power modules. The method uses the gate-source voltage, V_{GS}, at a constant, relatively low current and at a high anode-cathode voltage as the temperature sensitive parameter. Under these circumstances, variations in V_{GS} result from equal changes in the threshold voltage. The method is used to validate and extract short time constant thermal parameters for an electro-thermal simulation model of the IGBT (including the details of the package module). Under the measurement conditions used, there are concerns about the sharing of current between the chips in the package, but by taking these into account, excellent agreement is obtained between the measured and simulated temperatures (see Fig. 4). The module is shown in Fig. 5.

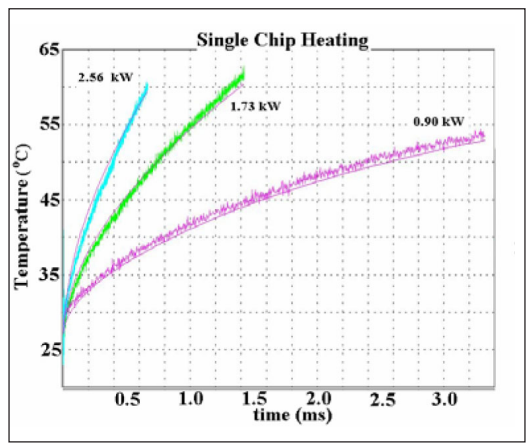

Figure 4. Electrically measured and computer simulated measurement of the temperature of IGBT chip in a power module.

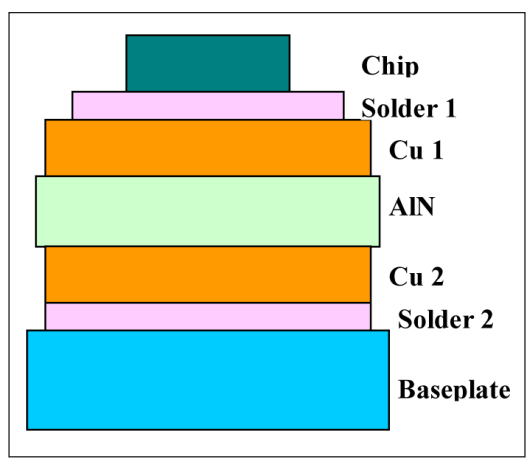

Figure 5b. Drawing of the vertical structure in the power module from one of the chips at the top to the baseplate at the bottom.

■ We have been invited to organize a technical session on *Temperature Measurements of Semiconductor Devices* at the 2004 IEEE Semiconductor Thermal Measurements and Management Symposium (SEMITHERM) to be held in March of 2004. The intent is to have presentations from experts in electrical, optical, and scanning probe temperature measurements for semiconductor devices and circuits.

Collaborations

IBM, Rochester, MN

Arv Sinha, Joe Kuczynski

AEPT Consortium

Dupont, John Felten

MacDermid, Dennis Fritz

Merix, Bob Greenlee

MicroFab, Plano, TX

Virang Shah

SAS Circuits, Littleton, CO

Richard Snogren, Matt Snogren

University of Colorado

Ken Douglass, T. Andrew Winningham

Colorado School of Mines

Ivar Reimanis, Saki Krishnamurthy,

John Berger

University of Nebraska

Kevin Cole

Cenymer Corporation

Charles Partee

Georgia Institute of Technology

George Washington University

University of Maryland

Motorola

Cree, Inc.

Army Research Laboratory

Recent Publications

Slifka, A. J., Drexler, E. S., "Thermomechanical Effects in Embedded Passive Materials," *Journal of Electronic Materials* , **31**, 4, pp.286-291 (2002).

Drexler, E. S., Snogren, R. C., Snogren, M. C., Felten, J. J., and Green, P. A., "Strain Measurements In Thermally Loaded Circuit Boards Containing Embedded Resistors," *Proceedings of the 52nd Electronic Components Technology Conference, pp.526–531 (2002).*

Slifka, A. J., Drexler, J. W., "Apparent Mobility of Interfaces in Integral Resistor Material," *Microscopy and Analysis,* pp.19-21, January 2003.

Hefner, A., Berning, D., Blackburn, D., Chapuy, C., and Bouche, S. A."High-Speed Thermal Imaging System for Semiconductor Device Analysis," *Proceedings of the 17th Annual IEEE Semiconductor Thermal Measurement and Management Symposium,* pp. 43-49 (2001).

Afridi, M. Y., et. al, "Transient Thermal Study of Microhotplates by Using High-Speed Thermal Imaging System," *Proceedings of the 18th Annual IEEE Semiconductor Measurement and Management Symposium*, March 2002.

Blackburn, D. L., "Temperature Measurement of Semiconductor Devices," Ther*mes 2002-Thermal Challenges in Next Generation Electronic Systems,* Millpress, Rotterdam Netherlands (2002), pg. 23.

J. Rodriguez, Z. Parrilla, M. Veléz-Reyes, A. Hefner, D. Berning, J. Reichl, and J. Lai "Thermal Component Models for Electro Thermal Analysis of Multichip Power Modules," in *conf. record IEEE Industry Applications Society Meeting, pp. 234-241,* October 2002.

D. Berning, J. Reichl, A. Hefner, M. Hernandez, C. Ellenwood, and J-S. Lai, "High Speed IGBT Module Transient Thermal Response Measurements for Model Validation," to be published in IEEE IAS meeting, October 2003.

Ortiz-Rodríguez, J. M., Hefner, A. R., Vélez-Reyes, M., and Gonzalez, J., "Electro-Thermal Modeling of the IPEM Generation II in SABER," *CPES Annual Industry Seminar, April 28-29, 2002.*

Atomic Layer Deposition – Process Models and Metrologies

Technical Contacts:
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W. S. Hurst

Goals

Develop validated process models and *in situ* metrologies for atomic layer deposition processes.

Customer Needs

As device critical dimensions continue to shrink, atomic layer deposition (ALD) is receiving increased attention as a method of depositing thin (nanometer-scale), conformal layers, required for many microelectronics applications. Applications include high-κ gate dielectric layers, diffusion barrier layers, copper seed layers, and DRAM dielectric layers. For some thin layer deposition applications, the 2001 ITRS identifies ALD as the dominant solution.

According to the 2001 ITRS, "modeling of thin film deposition and etch variation and feature variations across a wafer can provide tremendous savings in development time and cost" [2001 ITRS, Modeling and Simulation, page 2]. In addition, according to the 2001 ITRS, "An important future application of equipment modeling is the control of manufacturing equipment based on real time simulators including sensor design and simulation" [2001 ITRS, Modeling and Simulation, page 7]. Hence, wafer-scale modeling of ALD processes should facilitate efficient integration of ALD into the fab and aid in development of ALD diagnostics. However, *validated* ALD process models are not generally available. In fact, the 2002 ITRS Update identifies ALD modeling as a difficult challenge with important issues being the availability of accurate fundamental physical data as well as reaction mechanisms and reduced models for complex chemistry. In addition, the 2001 ITRS identifies experimental validation as a "key difficult challenge across all modeling areas" [2001 ITRS, Modeling and Simulation, page 1].

Technical Strategy

This project is in the initial stages. As such, this project involves only two primary directions: development of *in situ* metrologies sensitive to ALD chemistry and development of ALD chemical reaction mechanisms. These two directions are seen as mutually-supporting. It is expected that experimental results that elucidate ALD chemistry will aid in chemical mechanism development and ultimately in process model validation. Further, it is expected that the most important reaction species will be identified as understanding of a particular ALD reaction improves, thus facilitating the design of improved process metrologies.

Ultimately, aspects of both of metrology development and reaction mechanism development will be required to create validated ALD process models. ALD process models would be created by incorporating the chemical reaction mechanisms developed here into commercially available computational fluid dynamics code and then validating the process model under a range of parameters using experimental data collected in the course of this project. Initial reaction mechanism development will focus on Al_2O_3 ALD deposition.

While these two directions will be closely coupled for development of a specific ALD chemical reaction mechanism, this will not preclude exploration of non-mutually-supporting aspects of the metrology development and model development directions. For example, fundamental thermochemical and chemical kinetic properties of numerous organometallic compounds potentially suitable for ALD are under investigation. However, it would not be feasible to simultaneously provide experimentally validated ALD process models for all compounds. Also, metrologies are being investigated that will potentially be useful for ALD layer characterization but that would not necessarily provide data to validate ALD models currently under development, e.g., metrologies sensitive to impurity distributions in transition metal oxide films.

1. The first step in providing validated ALD process models is evaluating the suitability of diagnostics that are sensitive to ALD chemistry. Mass spectrometry and optical spectroscopic techniques are of particular interest because of their potential for in-situ monitoring. Mass spectrometry is relatively straight-forwardly integrated with an ALD reactor and, when in situ diagnostics are applied to ALD reactors, mass spectrometry is frequently employed. However, mass spectrometry is only sensitive to volatile

species and, hence, it is sometimes difficult to relate the species detected to mechanisms of interest on the growth surface. Because of the desire to directly probe ALD surface chemistry, Raman spectroscopy and infrared spectroscopy are also being investigated as potential ALD diagnostics. However, it is technically challenging to apply Raman and infrared spectroscopy to detect species present at monolayer quantities. For this reason, the suitability of these techniques is being evaluated using research-grade ALD reactors with optimized optical accessibility. After various diagnostics are evaluated in test ALD reactors, a more industrially-relevant ALD reactor will be designed and built. Suitable diagnostics will be integrated into this reactor to provide data that will aid in chemical mechanism development and overall process model validation.

DELIVERABLES: Construction of research-grade, optically-accessible ALD reactors. 3Q 2003
Evaluation of selected optical spectroscopic techniques for characterization of ALD films. 4Q 2003

2. The calculation, estimation, and dissemination of fundamental thermochemical and chemical kinetic properties of organometallic compounds with potential application to ALD, as well as chemical vapor deposition (CVD), processes is on-going. The thermochemical properties and reaction kinetics of most useful organometallic compounds and related molecular precursors are poorly characterized. This project obtains these properties through three activities involving theoretical estimations and modeling studies. The first data activity, which is in coordination with the Standard Reference Data Program, compiles and evaluates currently available thermochemical data of organometallic compounds and related precursors. These data are available through a NIST website: http://srdata.nist.gov/ckmechx/. The second activity supplements available data by using *ab initio* and semi-empirical calculations to develop reaction mechanisms from computed molecular structures, thermodynamic properties and spectroscopic properties of Group III and Group V compounds. The third activity utilizes the experimental and computed thermochemical and chemical kinetic data to develop mechanisms for the decomposition of organometallic precursors.

DELIVERABLES: Bibliographic and thermochemical data for aluminum and aluminum oxide deposition and relevant gas phase precursors. 3Q 2003
Calculated bond dissociation energies and barriers to reaction for organoaluminum precursors relevant to aluminum and aluminum oxide deposition. 4Q 3003

Accomplishments

■ ALD Reactor Construction — Research-grade, optically-accessible ALD reactors and precursor delivery systems have been designed and built. Each reactor is optimized for a particular optical diagnostic and will be used to test the suitability of that diagnostic to probe ALD processes. Investigations of various optical diagnostics have begun.

■ Chemical Properties Calculations — Molecular structure and vibrational frequency data for Group III (Al, Ga, In) and Group V (N,P,As) Hydrides have been compiled. These include the stable molecules (*e.g.*, AlH_3) and radicals (*e.g.*, AlH_2). *Ab initio* calculations have been utilized over a wide range of theories utilizing different quality basis sets. The *ab initio* results have been compared to available experimental data in order to determine the minimum level of calculation necessary to give good molecular structures and vibrational frequencies. Although some of this work has already been reported in the literature, no comprehensive set of benchmark calculations for the whole series has been performed. Molecular structure and vibrational frequency data and bond dissociation energies (BDE's) for the Indium Methyl Hydrides $InH_x(CH3)_y$ have been computed at the B3LYP/cc-pVTZ level of theory. The Indium Methyl Hydrides include the stable molecules InH_3, $InH_2(CH_3)$, $InH(CH_3)_2$, $In(CH_3)_3$, the radicals InH_2, $InH(CH_3)$, $In(CH_3)_2$, and the closed shell intermediates (with lone pairs) InH, $In(CH_3)$. Transition state calculations for abstraction of H atoms from the Indium Methyl Hydrides (In-H, CH_2-H bonds) by H atoms and CH_3 have been computed, as well as a number of other transition state calculations. These transition state structures were then used to determine temperature-dependent rate expressions for the reactions. A simple decomposition mechanism has been constructed based on these data, compared to available experimental data, and is currently being refined. Calculated molecular structure, vibrational frequencies, and BDE's for the Gallium Methyl Hydrides have also been carried out.

■ Database Website — A website http://srdata.nist.gov/ckmechx/ has been made available through the NIST Standard Reference Data website. This site currently contains bibliographic and thermochemical information of silicon hydrides, halocarbons, and organometallic compounds important to semiconductor processes. This site currently contains thermochemical and bibliographic information of silicon hydrides and halocarbons important to semiconductor processes. The plan for this site is to have it provide all data necessary to support chemical mechanisms of significance to the industry. The current version of CKMechX has a number of capabilities. Over 4,000 enthalpies of formation are available for more than 1,000 species with over 4,000 bibliographic citations. These data were taken from NIST compilations and evaluations of silicon hydrides, silicon oxyhydrides, hydrocarbons, fluorinated hydrocarbons, and chlorinated hydrocarbons.

■ This ALD project relies heavily on experience obtained in the course of a previous project investigating silicon thermal CVD via silane pyrolysis. That CVD project also involved development of chemical reaction mechanisms and experimental measurements to support mechanism development and process model validation. Multiple CVD process models were constructed employing the silane pyrolysis mechanisms, including gas phase nucleation of silicon particles, developed during this project and validated using the experimental results obtained in the course of this project. The different models employed reaction mechanisms of varying complexity and reactor geometries of varying dimensionality. Experimental measurements were performed in a vertical flow, rotating disk reactor under various process conditions. Gas temperature profiles were determined using rotational Raman spectroscopy. Gas phase silicon particle spatial distributions were determined with elastic light scattering. The extent of precursor decomposition and the chemical composition of the gas-phase-nucleated particles were investigated with vibrational Raman spectroscopy. A website (http://www.cstl.nist.gov/div836/836.02/cvd/toppage.html) has been established in order to disseminate the numerical and experimental results obtained from this investigation.

Collaborations

Professor G. W. Rubloff, University of Maryland; ALD processes and metrology.

Recent Publications

D. M. Kremer, R. W. Davis, E. F. Moore, J. E. Maslar, D. R. Burgess, and S. H. Ehrman, *An Investigation of Particle Dynamics in a Rotating Disk Chemical Vapor Deposition Reactor*, J. Electrochem. Soc. **150,** G127-G139 (2003).

D. M. Kremer, R. W. Davis, E. F. Moore, and S. H. Ehrman, *A Numerical Investigation of the Effects of Gas-Phase Particle Formation on Silicon Film Deposition From Silane*, J. Cryst. Growth **247,** 333-356 (2003).

Dielectric Metrology Supporting Integrated Passive Device Technology

Goals

To develop testing procedures specific to the needs of the electronics industry needed for the development of novel materials for Embedded Passive Devices Technology. The current focus is on the measurement of broad-band permittivity at microwave frequencies, dielectric withstanding voltage, and key structural attributes that control the properties of organic resins filled with electronic modifiers. The development of Integrated Passive Device technology depends on the availability of suitable measurement techniques to evaluate materials' properties and the functional characteristics of the manufactured passive devices.

Customer Needs

The continuous reduction in the electrical charge required to drive logic gates and storage cells has resulted in tremendous progress in miniaturization and density of integrated circuits. However, in modern highspeed electronics, the functional performance increasingly depends on passive components, where the dielectric permittivity and impedance characteristic are the main factors that control spatial dimensions, time scale, speed, shape, and amplitude of electronic signals. Passive devices have not shrunk in size as rapidly as active devices and tend to occupy an increasingly larger area and mass fraction of electronic subassemblies. In order to increase component density and reduce the parasitic effects of the associated interconnections, passive components may be integrated within substrates. Since integrated passive components are formed during substrate fabrication, they require new processing steps in addition to those that provide only interconnections and new thin-film integrated passive materials.

Novel dielectric hybrid materials based on polymers filled with modifiers of their electromagnetic properties have been identified by the industry as essential for advancing miniaturization and functional performance of high-speed electronics. There are significant challenges in developing new thin film materials that exhibit enhanced electrical performance characteristics, such as impedance and high dielectric constant, which are needed to operate at higher microwave frequencies and at increased voltage strengths. Consequently, new metrology methods are needed to address the specific behavior of thin film specimens and for better fundamental understanding of the relation between functional performance and the structural attributes of the materials.

The materials and testing requirements for capacitors, resistors and are outlined in the 2001 International Technology Roadmap for Semiconductors. A need for new standard test methods for embedded materials was identified by the IPC Embedded Passive Device Standard Sub-committee D-39.

Technical Strategy

1. The strategy pursued for high frequency characterization is to incorporate a thin passive film material into a device that comprises a capacitive or resistive termination in a transmission line. Samples that represent recent development and technological trends in embedded passive materials are obtained from our industrial partners. We also use model polymer composite materials to validate the measurement methods. Multifunctional acrylate polymers filled with electronic modifiers such as ferroelectric ceramics, metal particles, and carbon nanotubes are used to address fundamental dielectric properties of the composites. We employ a broad-band measurement technique to develop a systematic methodology for measuring impedance and the dielectric permittivity of embedded passive device materials at frequencies of 100 MHz to 10 GHz.

2. We are exploring non-linear dielectric measurement methodology for testing passive materials at high electric fields and voltages. Due to the thin film configuration, nonlinear effects may be activated at moderate bias levels and contribute to dielectric breakdown. Nonlinear dielectric effects may cause rectifying, an increased repolarization loss, or act as frequency multipliers, thus altering the nominal impedance characteristics of the material.

DELIVERABLES: Complete feasibility study of measurement on high-k films that are currently being developed by the electronic materials suppliers.
1Q 2004

Technical Contact:
J. Obrzut

"We truly need NIST expertise to take on this metrology work and help guide the participating people in the proper direction."

Tom Newton
Director of PWB
Standards & Technology
IPC Association
Connecting Electronics Industries

"Your effort to characterize the dielectric performance of the materials at high frequencies helped us to understand these materials and successfully realize our program objectives."

Richard A. Charbonneau,
Project Leader of the
EDC Consortium,
Storage Technologies

DELIVERABLES: Develop an AC dielectric withstanding voltage measurement system for embedded passive materials. Measure impedance of high-k films as a function of applied high voltage. Determine both the magnitude and phase of impedance from the corresponding voltage and current waves. 4Q 2003

3. In addition, NIST staff is chairing the Test Methods Task Group, D-37d, for the IPC – 4902 Embedded Passive Devices Standard Specification. This Test Methods Subcommittee is responsible for developing test methods which are specific to the needs of the D-37 Embedded Passive Devices Committee and its 3 Task Groups for materials, performance and design. As these Embedded Passive Devices-specific test methods are developed, they will be sent to the 7-11 Test Methods Subcommittee for inclusion in the TM-650 manual.

DELIVERABLES: Draft a standard test method document for IPC. 3Q 2003

4. The relationships between the dielectric properties and structure in polymer resins filled with ferroelectric ceramics are explored using these new measurement methods. Our effort is focused on local fast relaxation mechanism that we discovered in dielectric composites.

DELIVERABLES: Identify key materials attributes that control dielectric properties in polymers filled with ferroelectric inclusions. 3Q 2003

Accomplishments

■ We have implemented a broadband technique as a standard test method that enables dielectric measurements at microwave frequencies of up to several GHz. The technique is based on the observation and theoretical analysis of the fundamental mode propagating at high frequencies in thin film dielectrics that terminate a coaxial air-filled transmission line.

■ In partnership with IPC, we initiated a standard test method development and chair the IPC-D37-d test method sub-committee for Embedded Passive Devices. We guided the design of the test protocol and made arrangements with co-sponsoring member companies for round robin evaluation.

■ Our capability to measure the dielectric relaxation times in the sub-nanosecond regime and the relaxation strength for a wide range of dielectric permittivity values is used to quantify dispersion, alignment, and structure in hybrid materials. Using the broadband study, we demonstrated that the composites of organic polymer resins filled with ferroelectric ceramics exhibit a dominant intrinsic high frequency relaxation behavior. Such dielectric properties were found beneficial in eliminating the electromagnetic noise in processors and logic devices. We have confirmed that the fastest dielectric relaxation process is controlled by the di-polar dynamics of the polymer matrix while the dielectric loss arises from the difference in coupling between the relaxed and unrelaxed dipoles. Our numerical models are capable of quantitatively correlating the dependence of the real and imaginary parts of the complex permittivity on the volume fraction of the ceramic filler.

■ Suitable experimental set-up and testing procedures have been demonstrated for unambiguous determination of the dielectric withstanding voltage of embedded passive materials. In contrast to conventional procedures, the specimen voltage and current are determined as complex quantities from the corresponding time resolved voltage waves (Fig. 1). The new testing procedure represents a compatible extension of the existing standard test method, but is better suited for capacitive and resistive thin film materials.

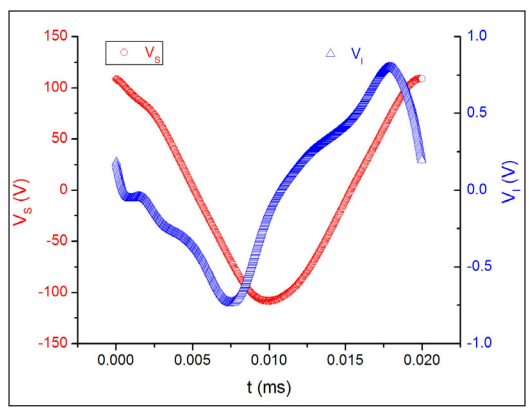

Figure 1. The specimen voltage wave (circles) and the wave corresponding to the specimen current (triangles). Distortions seen in the specimen current results from re-polarization dynamics, which has a considerable effect on impedance and contributes to the overall loss.

The specimen impedance and the loss tangent of the material can be determined by performing complex algebra calculations. It was found that embedded passive materials do not exhibit a constant impedence characteristic, as is the case for conventional dielectrics, but that their impedence characteristic sharply decreases with

increasing voltage. Conventional dielectrics such as FR-4 exhibit a flat impedance characteristic, nearly independent of voltage, up to the material break-down conditions. The break-down symptoms are associated with HV flashing and sparking that require further failure analysis. We concluded that the existing test methods seem to be adequate for typical dielectrics for which substantial laboratory and field data have been accumulated. In contrast, the impedance of embedded passive materials decreases continuously with increasing voltage and is associated with a large increase in the dielectric loss. This change in impedence cannot be detected by conventional methods.

With our method, the value of the dielectric break down can be accurately determined as an applied voltage at which the specimen impedance characteristic changes irreversibly. The value of the dielectric withstanding voltage can be determined when the specimen impedance drops below a certain functionally acceptable level or the phase angle increases above the functional limit.

Collaborations

Polymers Division, NIST – A. Anopchenko, K. Kano, N. Noda

Hokkaido University – R. Nozaki

DuPont — McGregor, G. S. Cox, J. Felten

Shipley — D. Senk

Nortel — R. Sheffield

Gould Electronics — T. Bergstresser

Electro Scientific Industries — K. Fjeldsted

Merix — R. Greenlee

Motorola — R. Crosswell

Recent Publications

Noda N., and Obrzut J., "High frequency dielectric relaxation in polymers filled with ferroelectric ceramics," Mat. Res. Soc. Symp. Proc., **628**, pp. EE.3.8.1-6 (2002).

Obrzut, J., Noda N., and Nozaki, R., "Broadband Characterization of High Dielectric Constant Films for Power - Ground Decoupling," IEEE Trans. on Instrumentation and Measurement, **51**, pp. 829 (2002).

Obrzut J., Anopchenko A., "High Frequency Input Impedance Characterization of Dielectric Films for Power-Ground Planes," IEEE Trans. on Instrumentation and Measurement, in press (2003).

Wafer Characterization and Process Metrology Program

Device scaling has been the primary means by which the semiconductor industry has achieved unprecedented gains in productivity and performance quantified by Moore's Law. Until recently only modest changes in the materials used have been made. The industry was able to rely almost exclusively on the three most abundant elements on Earth – silicon, oxygen, and aluminum.

Recently, however, copper has been introduced for interconnect conductivity, replacing aluminum alloys. A variety of low-dielectric constant materials are being introduced to reduce parasitic capacitance, replacing silicon dioxide. As dimensions continue to shrink, the traditional silicon dioxide gate dielectric thickness has been reduced to the point where tunneling current has become significant and is compromising the performance of the transistors. This is requiring the introduction of higher dielectric constant materials. Initially the addition of nitrogen to the gate material is sufficient, but in the near future more exotic materials such as transition metal oxides, silicates, and aluminates will be required. As dimensions are reduced, gate depletion effects and dopant diffusion through the gate dielectric are limiting transistor performance. With the replacement of the traditional silicon dioxide/ polysilicon gate stack processes with materials capable of supporting ever shrinking geometries, the task of the industry becomes more difficult. The overall task represented by the projects below reflects the need for analytical techniques with unparalleled spatial resolution, accuracy, robustness and ease of use.

Shrinking dimensions of transistors while simultaneously increasing the wafer diameter from 200 mm to 300 mm is placing more stringent requirements on wafer flatness, thickness and warp, ion and particle contamination.

Accurate metrology of process gases is essential for reproducible manufacture of semiconductor products. Critical physical parameters need to be measured on a wide variety of reactive and non-reactive process gases, allowing the accurate calibration of flow meters and residual gas analyzers. Water contamination at extremely low levels in process gases presents serious manufacturing difficulties. Accurate calibration of water vapor at extremely low vapor pressures is required.

Accurate metrology of process gases is essential for reproducible manufacture of semiconductor products and a wide variety of metrology issues emerge in plasma, chemical vapor, and rapid thermal processing steps used in semiconductor manufacture.

Detection and accurate sizing of particle contamination continues to challenge semiconductor manufacturing.

Wafer and Chuck Flatness Metrology

Goals

Develop measurement support for 300 mm diameter silicon wafers used in lithography applications. This project will provide measurement and infrastructural technology to support the interferometric measurement of thickness variation and surface flatness in the free form or chucked condition.

Customer Needs

Decreasing linewidths, and the resulting reduced depth of focus, combined with larger wafer diameters for current stepper lithography applications place ever increasing restrictions on flatness measurement and the required measurement uncertainty for thin parallel windows. For example, the International Technology Roadmap for Semiconductors (ITRS) suggests a flatness of less than 90 nm will be required per die site for the 90 nm node (expected by 2004). We are focused on meeting customer requirements for calibrated thickness variation maps of free form wafers and flatness measurements of chucked wafers. We are addressing the need for thickness variation maps of 300 mm diameter wafers using the NIST Improved Infrared Interferometer (IR^3). There are two reasons for concentrating on wafer thickness variation. First, an independent traceable measurement is required by instrument manufacturers to certify the performance of their instruments. Second, thickness variation measurements of silicon wafers can be combined with models of wafer/chuck interactions to determine the flatness of low surface area wafer vacuum chucks, which is difficult to measure directly. The surface flatness of chucked wafers can be measured using NIST's "eXtremely accurate CALIBration InterferometeR" (XCALIBIR). XCALIBIR has a 300 mm aperture for flat measurements and provides a way of verifying industry models of wafer/chuck interactions.

Technical Strategy

IR^2 is a prototype infrared interferometer built for NIST by Tropel, Inc., based on a NIST patent U.S. (5,739,906). The instrument can be used in several configurations. The collimated wavefront mode is the current focus of the project. In this method, the planar infrared wavefront is normally incident on the wafer. A portion of the beam is reflected from the front wafer surface, while the rest passes through the wafer and reflects from the rear surface. The interference of these two wavefronts produces fringes and, by wavelength phase shifting, allows calculation of the wafer thickness variation. See Fig. 1 below. This measurement configuration is limited to double side polished wafers.

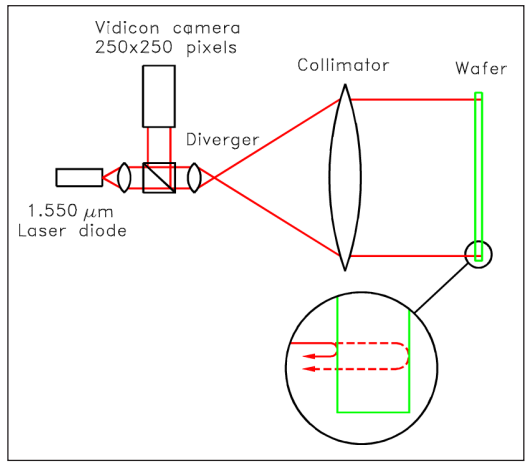

Figure 1. Schematic for collimated wavefront wafer thickness variation measurement.

1. There are two primary limitations to reaching the desired measurement performance using the current configuration of IR^2. These are the available measurement aperture and the optical imaging system. Using the collimated wavefront measurement technique, the existing measurement aperture is 150 mm. Although this aperture allows measurements to be performed and uncertainty evaluation to proceed, it is not sufficient to reach the end goal of thickness variation measurements of 300 mm diameter wafers. Additionally, it has been experimentally observed that due to large-scale geometric distortions in the free form wafers (e.g., bow or a drum shaped deflection), it is not possible to obtain data over the full measurement aperture. Instead, data dropout occurs because light does not reach the detector from certain portions of the wafer. This is due to: 1) a long path length from the objective lens to zoom lens in the imaging system; 2) non-uniform illumination over the measurement aperture, which subtracts from the available dynamic range of the detector; and 3) an asymmetric design for the objective lens. To address these needs, a collimator with 300 mm clear aperture has been designed and built by

Technical Contacts:
U. Griesmann
R. Polvani

"NIST continues to support the effort to bring quantitative standards and measurement practices to the semiconductor wafer metrology area. Their support in the area of wafer-chuck interaction studies are enabling advances in the state-of-the-art of wafer chucking that are essential to fully realize the potential of short wavelength lithography. WFSI's ability to collaborate with NIST in this area is critical to us."

T. D. Raymond
Wavefront Sciences, Inc., Albuquerque, NM

Nu-Tek Corp. The infrared interferometer is currently being upgraded and will be available for the testing of 300 mm diameter wafers in the 2nd half of 2003.

DELIVERABLES: Complete upgrade to IR^2 interferometer. 3Q 2003

2. A component in the evaluation of chucked wafer non-flatness is the characterization of interactions between the vacuum chuck and wafer. We will be continuing collaboration with Wavefront Sciences, Inc. (WFSI), Albuquerque, NM and potentially one or more lithographic stepper manufacturers to help understand these interactions. WFSI is carrying out numerical analyses of the chuck/wafer interface for various chuck geometries. XCALIBIR, a general purpose 300 mm aperture phase measuring interferometer developed at NIST, can now be used to measure the flatness of chucked wafers. We will compare our measurements with measurements made on the WFSI optical measurement tool. The data can then be used to evaluate the influence of wafer/chuck interactions on the chucked wafer flatness.

DELIVERABLES: Make flatness measurements with XCALIBIR of 300 mm diameter wafers to help characterize interactions between vacuum chucks and wafers. 3Q 2003

Accomplishments

■ A drift test was carried out using a 150 mm aperture collimator that captured data from the central portion of a 200 mm diameter, 750 µm thick, double side polished wafer. The measured optical path difference (*OPD*) was converted to thickness variation in nm using an assumed, homogeneous silicon index of 3.5. Total thickness variation (*TTV or GBIR*), which includes both the constant wafer thickness as well as local and/or linear variations in thickness, was not measured here because the piston, or constant, term was considered a setup error and removed during data analysis. Piston was removed because the *OPD* between the front surface and back surface reflections varies with changes in the angular orientation between the wafer and collimated source.

■ Average of repeatability testing measurements. The average of 192 phase measurements recorded at 15 minute intervals over a two day period is shown in Fig. 2. A peak-to-valley (PV) thickness variation of 1663.0 nm and root-mean-square (RMS) value of 414.4 nm were recorded over the measured aperture. Clearly, this wafer geometry is dominated by wedge, or a linear variation in thickness across the wafer face (the wafer is thinner at the top).

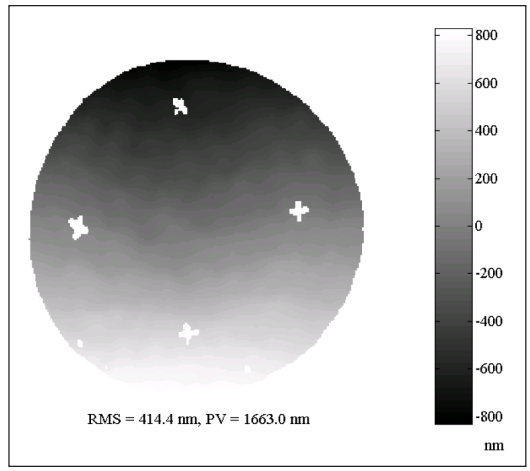

Figure 2. Average of repeatability testing measurements.

The (one sigma) pixel by pixel standard deviation in the 192 measurements is also shown in Fig. 3. This result, which was dominated by stray light in the interferometer, suggests repeatability at the 6 nm level for this set of tests. Temperature sensitivity was also measured; however, no strong correlation between variation in the results and temperature existed due to the high stability of the measurement cavity (i.e., the wafer).

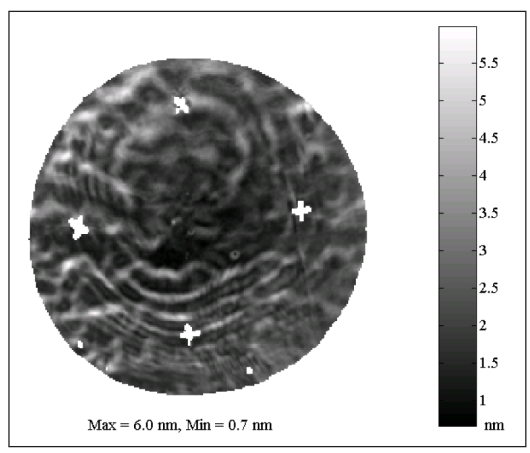

Figure 3. One sigma pixel by pixel standard deviation of repeatability measurements.

■ The result for a thickness variation measurement of a 100 mm diameter, 750 µm thick double side polished wafer follows and shows a PV thickness variation of 204 nm, Fig. 4, where the thickness variation is manifested as 'power', or the Zernike a_2^0 term, in the phase map. This large power suggests a gradual thinning radially from the outside edge to the center of the wafer.

Surface reflection measurements of this wafer were performed using a commercial phase measuring interferometer in a Fizeau configuration. A front surface measurement showed a slightly concave shape with an a_2^0 Zernike coefficient of 4.437 waves (at a wavelength of 632.8 nm). A back surface measurement demonstrated a slightly convex shape with an a_2^0 value of 4.372 waves. The sag, *s*, for each surface can be calculated as $s = 2 \cdot a_2^0 \cdot 632.8\,(\text{nm})$. The larger sag for the front (concave) surface suggests the wafer is thinner in the center, as shown by the IR[2] result. The sag for the front surface measurement was 5615 nm and 5533 nm for the back surface. The difference of these two gives an estimate of the gross thickness variation over the approximate measurement aperture of 30 mm (the smaller aperture was required to obtain reasonable fringe density for the bowed wafer and allow successful phase unwrapping). This difference is 82 nm.

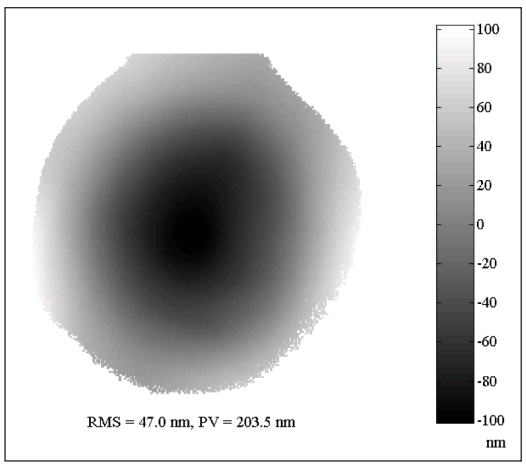

Figure 4. Thickness variation measurement for 100 mm diameter, 750 μm thick double side polished wafer (piston and tilt removed). Map shows that wafer is thinner in center by approximately 204 nm.

■ A diamond-turned vacuum chuck for 300 mm diameter wafers was designed and machined at NIST for chucked wafer flatness measurements with the XCALIBIR interferometer.

Collaborations

Wavefront Sciences, Inc, T. D. Raymond; flatness measurements of free form and chucked wafers on XCALIBIR.

Virginia Semiconductor, Inc., Stephen Jones; thickness variation measurements of ultra-flat wafers.

Komatsu Silicon America, Paul Langer; 300 mm diameter wafer measurements.

Recent Publications

Griesmann, U., Schmitz, T. L., Soons, J., Polvani, R., "New Optical Metrology at NIST for Semiconductor Lithography," ASPE Spring Topical Meeting "Progress in Precision," April 17-18, 2002, Raleigh, NC (in press).

Parks, R. E., Shao, L.-Z., Davies, A., Evans, C. J., "Haidinger Interferometer for Silicon Wafer TTV Measurement," Proceedings of SPIE, Vol. 4344, Metrology, Inspection and Process Control for Microlithography XV (2001), pp. 496-505.

Evans, C. J., Davies, A., Schmitz, T. L., Parks, R. E., Shao, L.-Z., "Interferometric metrology of substrates for VLSI," 2nd International Conference of the European Society for Precision Engineering and Nanotechnology – **eu**spen, "Torino Incontra" Congress Centre, Torino, Italy (2001).

Evans, C. J., Parks, R. E., Shao, L.-Z., Davies, A., "Interferometric Metrology of Photomask Blanks: Approaches Using 633 nm Wavelength Illumination," NISTIR 6701, December 2000.

Modeling, Measurements, and Standards for Wafer Surface Inspection

Technical Contacts:
T. A. Germer
G. W. Mulholland

"I would like to thank you and NIST for the support that you have provided to VLSI Standards in the sizing of polystyrene latex spheres through the work of Dr. George Mulholland. We are very pleased with the measurements that Dr. Mulholland has performed, and with the level of technical support that the NIST staff has provided to us. This work is of technical and economic importance to the semiconductor industry and to VLSI Standards, because the ability to correctly size ever smaller particulate contaminants on silicon substrates is key to the manufacturing yield of silicon chips. We look forward to a continuing technical relationship between VLSI Standards and NIST."

Marco Tortonese, Ph.D.
VLSI Standards, Inc.

Goals

Provide industry with models, measurements, and standards for particles and other defects in order to improve the inspection of wafer surfaces. Develop facilities to accurately measure particle size and to deposit monosize particles on calibration artifacts to reduce the uncertainty in the sizes of particles used by the semiconductor industry to calibrate scanning surface inspection systems (SSIS). Investigate theoretically and experimentally the behavior of light scattering from particles, defects, and roughness on wafer surfaces.

Customer Needs

The Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors (ITRS) identifies the detection and characterization of defects and particles on wafers to be a potentially show-stopping barrier to device miniaturization. The roadmap specifies that by 2005, 40 nm particles must be detectable on bare silicon, nonmetallic films, and metallic films, while 100 nm particles must be detectable on wafer backsides. Currently, no solutions to this inspection problem exist. While the detection sensitivity for defects must be increased, the ability to characterize defects in terms of size, shape, composition, etc., is critical for yield-learning. Defects must be characterized independent of defect location and topology.

With the need to detect smaller defects, the costs of inspecting wafers are skyrocketing. For new advances to be implemented in production environments, improvements in sensitivity must be achieved without suffering a tradeoff in throughput and must be cost-effective. The drive towards *in situ* sensors for production tools requires techniques which can be effectively miniaturized.

In order that wafer manufacturers and device manufacturers have a common basis for comparing specifications of particle contamination, improved standards for particles are needed. A recent comparison of the measurements of calibration wafers by thirteen different SSISs indicated unacceptably large deviation between the SSIS results and the actual particle sizes. This study involved six particle sizes ranging from 88 nm to 290 nm and included the NIST SRM 1963 and two other sizes measured by NIST. For the two smallest particle sizes, 88 nm and 100.7 nm, the scanners systematically underestimated the size by about 8 %. By 2005, it is anticipated that accurate calibration particles as small as 30 nm will be needed.

By 2005, at the 80 nm node, particle having diameters 40 nm must be detectable on bare silicon, nonmetallic films, and metallic films, while 100 nm must be detectable on the backsides of wafers. No known solutions exist at this time. [2002 ITRS, Yield Enhancement, Table 93a]

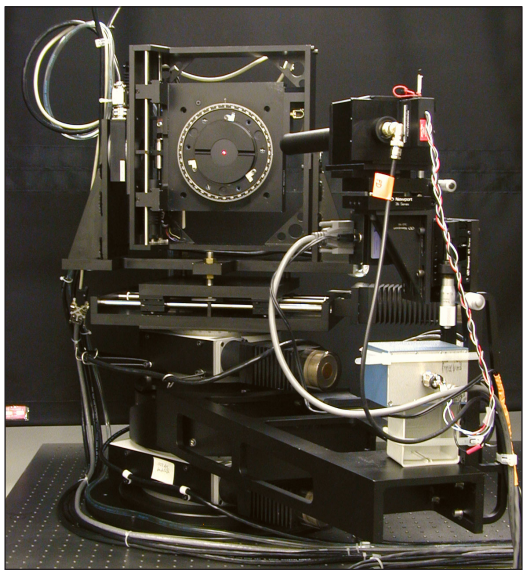

Figure 1. The Goniometric Optical Scatter Instrument is a state-of-the-art laser scattering facility.

Technical Strategy

There are two major strategies to improving the performance of scanning surface inspection systems. One strategy is to develop a fundamental understanding of optical scattering at surfaces so that tool manufacturers can optimize the performance of their instrumentation, in terms of defect detection limits and discrimination capabilities, to characterize the response of instrumentation to different types of defects, and to develop and calibrate particles of well-defined size and material. Recent work by this group has demonstrated that the polarization of light scattered by particle contaminants, subsurface defects, and microroughness has a unique

signature that can be used to identify the source of scatter. In particular, it was found that small amounts of roughness do not depolarize scattered light. This finding has enabled the development of instrumentation which can collect light over most of the scattering hemisphere, while being blind to microroughness. That instrumentation, for which a patent has been awarded, should result in a factor of two improvement in minimum detectable defect size.

A second strategy is to provide leadership in the development of low uncertainty calibration particles for use in calibrating surface scanners. A major focus has been development of the differential mobility analysis (DMA) method for accurately sizing monosize polystyrene spheres. This work together with a SSIS round robin has provided evidence that current SSIS measurements have an unacceptably large uncertainty for particle sizes in the 90 nm to 100 nm size range. The technical focus of our future work will be applying the DMA for accurately sizing calibration particle sizes as small as 30 nm and developing methods for generating other types of monosize particles.

Specific project elements are defined below:

1. Polarized Light Scattering Measurements – The Goniometric Optical Scatter Instrument (GOSI), shown in Fig. 1, enables accurate measurements of the intensity and polarization of scattered light with a wide dynamic range, high angular accuracy, and multiple incident wavelengths (visible and UV). We measure the light scattering properties of well-characterized samples exhibiting interfacial roughness, deposited particles, subsurface defects, dielectric layers, or patterns. The emphasis is on providing accurate data, which can be used to guide the development of light scattering instruments, and to test theoretical models.

DELIVERABLES: Light scattering measurement of diameter of a 60 nm sphere standard and an associated uncertainty analysis. 3Q 2003

Demonstrate proof of principle light scattering-based overlay measurement and assess uncertainty of the measurement. 3Q 2003

2. Theoretical Light Scattering Calculations – The focus of our theoretical work is on: (a) developing models that accurately predict the polarization and intensity of scattered light, and (b) determining what information can be efficiently and accurately extracted from light scattering measurements. Approximate theories are used in conjunction with more complex techniques to gain an understanding of which parameters affect the light scattering process. Particular cases that are being analyzed include: (a) scattering by defects and roughness associated with dielectric layers, (b) scattering by particulate contamination on bare and oxidized wafers, and (c) scattering by periodic structures.

DELIVERABLES: Publish, via the world-wide-web, a version of the SCATMECH library of scattering codes which contains a theory for scattering by axially-symmetric particles on surfaces. 1Q 2004

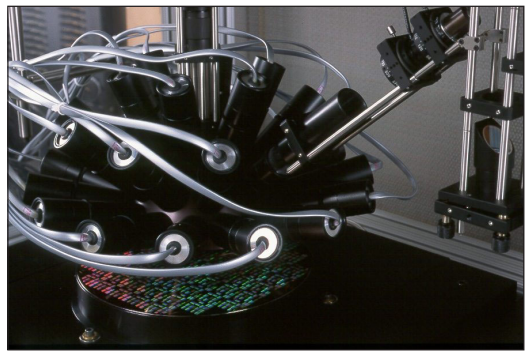

Figure 2. The MHPOSI enables the scattering from individual particles to be analyzed.

3. Instrument Development – A second instrument, the Multidetector Hemispherical Polarized Optical Scatter Instrument (MHPOSI) (see Fig. 2), complements the capabilities of GOSI as a prototype for a production-line light scattering inspection tool. An instrument with twenty-eight fixed detection elements covering the scattering hemisphere, MHPOSI enables a determination of the differential scattering cross section, for individual particles or defects on a wafer surface. This instrument can be configured so that it is blind to interfacial roughness. Together with an understanding of the light scattering functions for different imperfections, MHPOSI has a substantially improved capability for rapidly detecting and identifying defects, particles, and microroughness on wafers.

DELIVERABLES: Perform size distribution measurements of the 100 nm sphere standard (NIST SRM 1963) using the MHPOSI system. 3Q 2003

4. Size Distribution Measurements – Differential mobility analysis (DMA) has been shown to be capable of making accurate size measurements for mean particle size for 100 nm monosize polystyrene latex spheres (PSL). There are

promising results for the measurement of the size distribution for broader size distributions; however, the results are not quantitative. Work is in progress to quantify the uncertainty in the size distribution measurement and to extend the method to smaller particle sizes.

DELIVERABLES: Development of particle sizing calibration facility and documentation of measurement protocol and data analysis. 2Q 2003

Provide uncertainty estimates for moments of the size distribution for PSL spheres based on DMA measurements. 4Q 2003

5. Aerosol Generation – An aerosol must be formed typically from a liquid spray of a particle suspension before the particles can be sized by the DMA or deposited on a wafer. Work is in progress to use a variety of innovative methods for generating, shaping the size distribution of the aerosol, and depositing the particles. These include the electrospray for generating particle sizes smaller than 60 nm, impactor to remove the large size fraction of the aerosol and to deposit the particles, and an electrostatic chamber for depositing small particle sizes. Work is also in progress to generate metallic particles from chemical precursors in a tube furnace.

DELIVERABLES: Recertify SRM 1963 for the size of the primary sphere. 1Q 2003

Deposit of monosize 65 nm PSL spheres on silicon wafers for use in light scattering measurements. 3Q 2003

Publication of manuscript on the generation and sizing of PSL spheres as small as 30 nm using electrospray. 4Q 2003

6. Resource on Particle Science – Over the past five years, the particle related work has included projects with SEMATECH and particle suppliers to the semiconductor industry. A number of needs by particle related companies were expressed at a NIST particle workshop including redoing the uncertainty assessments of existing particle SRMs and offering a particle sizing calibration service. Providing support for particle needs critical to the semiconductor industry will continue to be a priority.

DELIVERABLES: Coordinate round robin to assess the performance of particle deposition systems in collaboration with the semiconductor industry. 3Q 2003

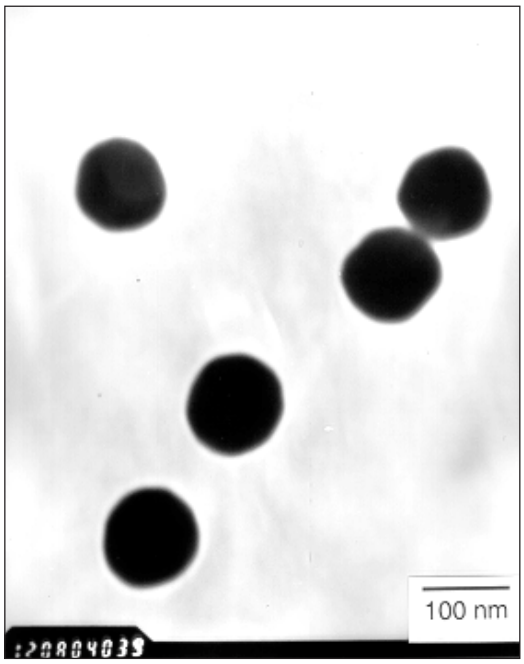

Figure 3. Transmission electron microscope images of 100 nm copper spheres generated by a novel spray pyrolosis method. These particles are being developed to test light scattering theories for scattering by particles on surfaces.

Accomplishments

- In January 2001, A NIST-sponsored workshop entitled "Issues Related to SSIS Calibration with Polystyrene Spheres" brought together suppliers of wafers, reference particles, particle sizing and deposition equipment, and wafer inspection instruments. This sets the stage for developing a more responsive particle program.

- Determined that the electrospray technique can produce an aerosol having characteristics optimal for transferring particles in a liquid suspension onto wafers for particle diameters as small as 25 nm. This significant finding enables improved wafer depositions by reducing the number of contaminant residue particles, the number of doublets, and the amount of residue on the particles.

- Developed a NIST Calibration Facility for sizing monodisperse spheres suspended in water in the size range of 50 nm to 400 nm with an expanded uncertainty of 1.5 % of the peak size. This facility has been used for two customers providing calibration particles to the semiconductor community.

■ In collaboration with the University of Maryland, developed a method for generating pure copper spheres (see Fig. 3), with diameters ranging from 100 nm to 200 nm. These spheres, which mimic real-world particles better than polystyrene, were used to validate particle scattering theories in conditions for which models have a higher degree of uncertainty. Measured polarization and intensity of light scattered from the copper spheres and found good agreement with the Bobbert-Vlieger theory for light scattering from a sphere above a surface.

■ Developed a method, based upon scattering ellipsometry, for quantifying scatter from two sources and demonstrated its use by characterizing the roughness of both interfaces of an SiO_2/silicon system. This finding establishes the validity of the light scattering models for roughness in a dielectric film, which in turn limits the detection sensitivity of SSIS instruments. The method was also used to characterize scattering from steel surfaces, demonstrating capability to distinguish between scattering from surface roughness and material inhomogeneity. The method was further used to study the scatter from an anti-conformal polymer film, helping to establish the limits of validity of the scattering theory.

■ Developed the SCATMECH (see http://physics.nist.gov/Divisions/Div844/facilities/scatmech/html/) library of C++ routines for light scattering. Published the SCATMECH library, providing a means for distributing scattering models and polarized light calculations to others. From the time of its public availability in March 2000 to the end of January 2002, 647 copies of the library have been downloaded from the web. In July 2003, Version 4 will be released, which contains an accurate theory for the scattering of light by a spherical particle on a surface and theories for scattering from roughness and small defects in dielectric layers.

■ Extended the theory of scattering of a sphere on a surface to axially-symmetric non-spherical particles. Demonstrated that the scattering by a metal particle on a surface is extremely sensitive to the shape of the particle in the region where the particle contacts the surface. This unusual sensitivity to shape must be considered when light scattering tools classify particles for material and size.

■ Performed a light-scattering-based diameter measurement of the NIST 100 nm PSL sphere standard (SRM 1963) deposited onto a silicon wafer. The measurement results included a thorough assessment of the uncertainties that arise in such measurements. It was found that the uncertainty was dominated by sample-to-sample variations, which probably result from the presence of doublet particles. Uncertainties in the substrate optical properties, the thickness and optical properties of the substrate oxide, and the shape of the particle dominate the systematic uncertainty.

Collaborations

Department of Chemical Engineering, University of Maryland, Professor Sheryl H. Ehrman, Validation of Scattering Theory Using Novel Monodisperse Particles.

Department of Mechanical Engineering, University of Minnesota, Professor David Pui, Generation and Measurement of Nanosize Particles.

National Metrology Institute of Japan, Dr. Kensei Ehara, Nanoparticle Metrology.

Recent Publications

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George W. Mulholland, Thomas A. Germer, and John C. Stover, "Modelling, Measurement, and Standards for Wafer Inspection," GOMACTech 03 "Countering Asymetric Threats," Tampa, FL, March 2003.

High Resolution Microcalorimeter X-ray Spectrometer for Chemical Analysis

Goals

We will develop new generations of x-ray spectroscopy tools to meet the materials analysis needs of the semiconductor manufacturing industry. Energy-Dispersive Spectrometers (EDS) based on microcalorimeters have the ability to detect photons with high energy resolution and near-unity quantum efficiency. Using these tools, a wide range of materials analysis problems can be solved. In semiconductor manufacturing, improved x-ray materials analysis is needed to identify nanoscale contaminant particles on wafers and to analyze very thin layers of materials and minor constituents. Microcalorimeter EDS improves the spectral resolution by one to two orders of magnitude compared to the semiconductor Si-EDS, the existing industry standard. Such improved resolution combined with energy dispersive operation makes possible direct spectral separation of most overlapping peaks often encountered with Si-EDS in complex multi-element systems. The improved resolution of the microcalorimeter EDS also increases the peak-to-background ratio. Peak shape and shift can be studied to reveal chemical state information.

Developing arrays of x-ray microcalorimeters will enable the acquisition of high statistics spectra in reduced time, improving the efficiency and statistical quality of existing materials analysis applications. Further, large-format arrays (up to 1,000 pixels) will make it possible to chemically analyze smaller features and trace constituents, and to track rapidly evolving x-ray spectra for in-process and process-stream monitoring.

The microcalorimeter EDS detector invented at NIST consists of a superconducting thermometer (a superconducting transition-edge sensor (TES)) and an x-ray absorber fabricated on a micromachined Si_3N_4 membrane, and cooled to cryogenic temperatures (0.1 K). When x-rays are absorbed in the detector, the resulting heat pulse in the microcalorimeter is measured by the TES thermometer. The change in the temperature of the thermometer is measured by a superconducting quantum interference device (SQUID) amplifier. The temperature pulse height gives a measurement of the energy of the x-ray photon one to two orders of magnitude more sensitively than Si-EDS. The detector is cooled to 0.1 K by a compact adiabatic demagnetization refrigerator.

Customer Needs

Improved x-ray detector technology has been cited by SEMATECH's Analytical Laboratory Managers Working Group (ALMWG, now Analytical Laboratory Managers Council, ALMC) as one of the most important metrology needs for the semiconductor industry. In the International Technology Roadmap for Semiconductors, improved x-ray detector technology is listed as a key capability that addresses analysis requirements for small particles and defects. The transition-edge sensor (TES) microcalorimeter x-ray detector developed at NIST has been identified as a primary means of realizing these detector advances, which will greatly improve in-line and off-line metrology tools that currently use semiconductor energy-dispersive spectrometers (EDS). At present, these metrology tools fail to provide fast and unambiguous analysis for particles less than approximately 0.1 mm to 0.3 mm in diameter. Improved EDS detectors such as the TES microcalorimeter are necessary to extend the capabilities of existing SEM-based instruments to meet the analytical requirements for future technology generations. With continued development, microcalorimeter EDS should be able to meet both the near-term and the longer-term requirements of the semiconductor industry for improved particle analysis.

Promising new technology such as high energy resolution x-ray detectors must be rapidly commercialized. Prototype microcalorimeter energy dispersive spectrometers (EDS) and superconducting tunnel junction techniques have x-ray energy resolution capable of separating overlapping peaks and providing chemical information. These advances over traditional EDS and some wavelength dispersive spectrometers can enable particle and defect analysis on SEMs located in the clean room. **2001 International Technology Roadmap for Semiconductors**

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C. D. Reintsema
J. N. Ullom
L. R. Vale

"[T]his type of resolution, very simply, was something that I thought was truly, truly a dramatic advance. And I really would like to encourage the people working on this at NIST and the equipment industry to get this into commercialization as soon as they possibly can."

Mark Melliar-Smith, Former President and Chief Executive Officer of SEMATECH

Technical Strategy

1. The usefulness of single-pixel x-ray microcalorimeter EDS in materials analysis has now been well established in a variety of demonstrations. Small arrays of x-ray microcalorimeters are being tested, and the development of technologies for large-format arrays is in process. To meet the needs of the semiconductor industry, it is necessary to make both single-pixel and array microcalorimeter systems more widely available. In addition to microcalorimeters, the system requires novel superconducting electronics to instrument the detectors, compact adiabatic demagnetization refrigerators to simplify cooling to milliKelvin operating temperatures, and custom room-temperature electronics and software to process the output signals. Our goal is to develop new generations of detector systems, to transfer them to the Chemical Science and Technology Laboratory (CSTL), see Fig. 1 in NIST Gaithersburg, Maryland for collaborative use in studying problems of interest to the industry, and to work with other partners in disseminating the technology.

Figure 1. Single-pixel NIST x-ray microcalorimeter system on a scanning-electron microscope. The system was developed in the Electronics and Electrical Engineering Laboratory (EEEL) at NIST, Boulder, and transferred to the Chemical Science and Technology Laboratory (CSTL) at NIST Gaithersburg, Maryland to be used to study problems of interest to the semiconductor industry.

DELIVERABLES: Provide continued support and upgrades for the single-pixel microcalorimeter system transferred to CSTL. Prepare for the eventual transfer of an array microcalorimeter system. Collaborate with CSTL on using the microcalorimeter to study problems of interest to the semiconductor industry. 4Q 2003

2. For many semiconductor materials analysis problems, further improvements in energy resolution (beyond that already demonstrated with these detectors) are not as important as an increase in the maximum count rate and collection area. Both the collection area and count rate can be improved by the implementation of multipixel arrays of detectors. Small arrays of x-ray microcalorimeters are now being tested. This work must be continued with a demonstration of the addition of x-ray spectra from multiple pixels.

DELIVERABLES: Demonstrate the addition of x-ray spectra from multiple pixels in a close-packed x-ray microcalorimeter array to demonstrate the increase in collection area and count rate achievable with arrays. 4Q 2003

3. One of the barriers to widespread dissemination of x-ray microcalorimeter instruments is the complexity and cost of the adiabatic demagnetization refrigerator used to cool to 100 mK. The development of an on-chip solid-state micro-refrigerator based on superconducting tunnel junctions to cool from 300 mK to 100 mK would greatly simplify the cryogenic system needed for microcalorimeter EDS. Adiabatic demagnetization refrigerators could be replaced by small, simple, and inexpensive ^{3}He systems, which cool to 300 mK, coupled to the solid-state tunnel-junction refrigerator cooling to 100 mK.

DELIVERABLES: Fabricate an integrated solid-state tunnel-junction refrigerator and microcalorimeter x-ray detector that could be coupled to a simple ^{3}He refrigerator. 4Q 2003

4. The multiplexed operation of 8 x-ray microcalorimeters has now been demonstrated using SQUID multiplexers operated at cryogenic temperatures. A higher bandwidth system must now be demonstrated to increase the number of pixels that can be multiplexed and the maximum count rate.

DELIVERABLES: Design and fabricated a high-bandwidth SQUID multiplexer optimized for high-count-rate microcalorimeter EDS. 3Q 2003

5. Extensive custom room-temperature digital electronics and firmware has been developed to drive and provide feedback signals to SQUID multiplexers, and to acquire data from multiplexed x-ray microcalorimeters. Improvements are still necessary to make a useful multiplexed array system. Dedicated, multi-row address-line driver boards to switch on multiplexed amplifiers must be developed, and software must be developed to analyze the data that is streamed to disk.

DELIVERABLES: Develop dedicated custom address-line driver electronics and software to analyze multiplexed array data and create pulse-height spectra. 3Q 2003

Accomplishments

■ This year, we fabricated 8×8 arrays of microcalorimeters on surface-micromachined structures (see Fig. 2). These structures consist of a silicon-nitride membrane freely suspended 2 microns above a solid silicon substrate, and connected to it by silicon-nitride supports. This is in contrast to the usual bulk micromachining technique, in which a silicon nitride membrane is deposited on a silicon wafer, and all silicon below it is removed through the entire thickness of the wafer. Single pixels from the array have been shown to work. These arrays are now being tested in a multiplexed SQUID readout system.

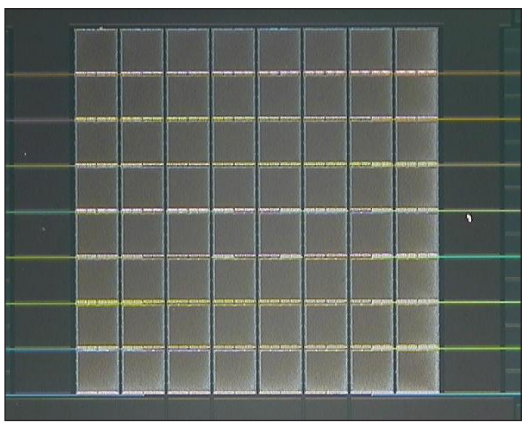

Figure 2. A 8x8 array of x-ray microcalorimeters on suspended silicon nitride platforms created using surface micromachining at NIST. Each microcalorimeter consists of a microcalorimeter and a 2-μm-thick Bi absorber.

■ We transferred a complete prototype microcalorimeter EDS system from EEEL in NIST, Boulder to CSTL in NIST, Gaithersburg. The microcalorimeter system has been successfully implemented on a CSTL analytical scanning electron microscope in Gaithersburg. We are now collaborating with CSTL researchers on upgrading the system. It will eventually be upgraded to a microcalorimeter array system (see Fig. 3).

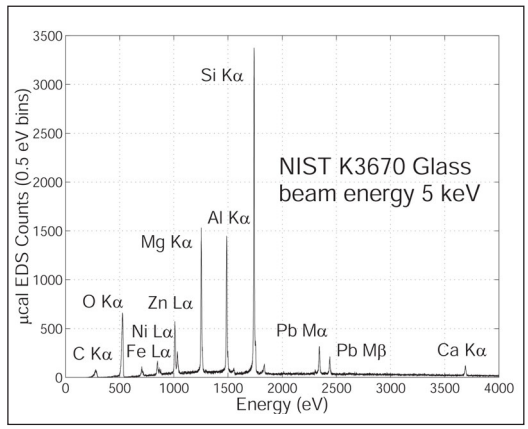

Figure 3. Microcalorimeter EDS spectrum of NIST calibration glass K3670 taken by the microcalorimeter system transferred to CSTL in Gaithersburg, Maryland.

■ We have demonstrated the multiplexed readout of 8 microcalorimeter pixels from an 8×8 microcalorimeter array (see Fig. 4). All eight channels were multiplexed and read out in one output channel, and demultiplexed in software. The energy resolution was measured for pulses of energy injected in the microcalorimeters due to Joule heating. No energy resolution degradation was observed due to multiplexing. We are now testing the multiplexed array with x-rays. We are also designing faster SQUID multiplexers to allow more pixels to be multiplexed in one channel.

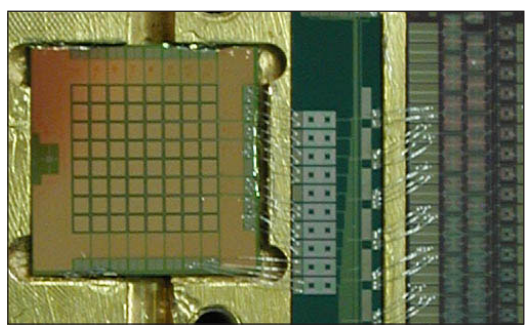

Figure 4. Photograph of an 8x8 array of microcalorimeters. 8 channels of the array are read out in one output channel with a SQUID multiplexer. The chip on the left is the microcalorimeter array. The middle chip is a filter chip. The chip on the right is the SQUID multiplexer.

■ We have begun work on an on-chip solid-state refrigerator to cool x-ray microcalorimeters from 300 mK to 100 mK (see Fig. 5). If successful, this refrigerator could greatly simplify the cryogenic system needed for microcalorimeter EDS. Adiabatic demagnetization refrigerators could be replaced by small and inexpensive ^{3}He

systems coupled to the solid-state refrigerator. This device is a superconducting analog of a Peltier cooler. Cooling is produced in the devices by the tunneling of electrons through normal-insulator-superconductor junctions. We have recently demonstrated cooling from 300 to 175 mK in devices whose cooling power is well matched to microcalorimeter x-ray sensors. The solid-state refrigerator is fabricated on a silicon wafer using conventional thin-film and photolithographic techniques, has no moving parts, and operates continuously. A micro-refrigerator will be integrated with an x-ray microcalorimeter this year.

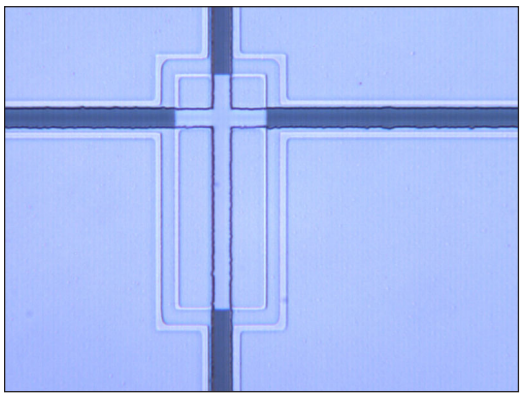

Figure 5. Micrograph of solid-state refrigerator. Four normal-insulator-superconductor tunnel junctions cool the central metal island. The island has dimensions of 15 µm x 40 µm. NIS microrefrigerators will be integrated with microcalorimeters this year.

■ The NIST microcalorimeter EDS holds the world record for energy resolution for an EDS x-ray detector of 2.0 eV at 1500 eV, which is over 30 times better than the best high resolution semiconductor-based detectors currently available. This energy resolution was measured using a glass prepared by Dale Newbury of NIST to use as a test standard for EDS.

■ We created a chemical shift map showing the chemical bonding state of Al in a sample containing both Al and Al_2O_3 (see Fig. 6). An aluminum film was deposited on part of a sapphire substrate. A microcalorimeter EDS was used to measure the x-ray spectrum as the electron beam was rastered to form the SEM image. The Al x-ray line position was shifted by a small amount (about 0.2 eV) in the regions containing Al_2O_3 as compared to the regions containing elemental Al (see Fig. 6). The high energy resolution of the microcalorimeter allowed the shift to be measured, resulting in the false-color image in Fig. 7. The map clearly demonstrates that microcalorimeter

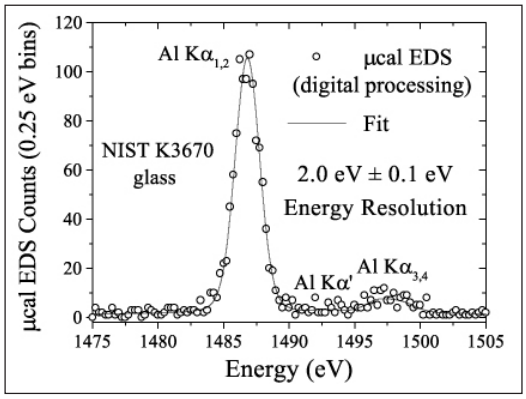

Figure 6. The Al-Kα region of a microcalorimeter EDS spectrum of the multielement NIST K3670 glass. The acquired spectrum is shown as well as a weighted least-squares fit of the Al Kα and satellite lines convolved with a Gaussian instrument response, yielding an energy resolution of 2.0 eV ± 0.1 eV FWHM.

EDS can be used to discriminate the chemical bonding state using shifts in the positions of x-ray lines. The result also highlights the need for large-format arrays to increase the data-collection rate. The image shown here was acquired over several hours. Images such as this could be acquired much more quickly and with much sharper position resolution using an array microcalorimeter.

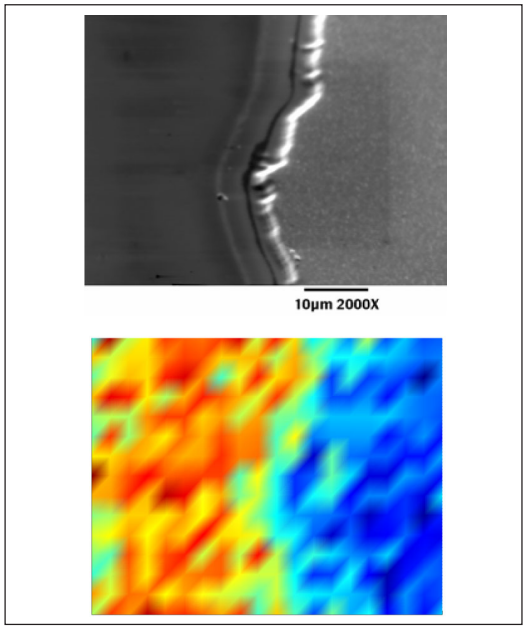

Figure 7. SEM photo (top) of an aluminum film partially covering a sapphire substrate and a false-color map (bottom) of the shift in the mean x-ray energy of the Al Kα peak taken using a microcalorimeter EDS system. The shift in energy is due to the chemical bonding of the aluminum with the oxygen. The average energy shift is ~0.2 eV.

Collaborations

Chemical Science and Technology Laboratory, NIST, Gaithersburg, Terry Jach, Lance King, Dale Newbury, John Small, and Eric Steel, the development of microcalorimeter EDS systems.

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Wollman, D. A., Newbury, D. E., Nam. S. W., Hilton, G. C., Irwin, K. D., Rudman, D. A., Deiker, S., Bergren, N. F., Martinis, J. M., "Microcalorimeter EDS: Benefits and Drawbacks," Proc. Microscopy and Microanal. 2000, 738-739 (2000).

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Thermophysical Property Data for Modeling CVD Processes and for the Calibration of Mass Flow Controllers

Technical Contacts:
John Hurly
Michael R. Moldover

"I was pleasantly surprised when I came across your database of thermophysical properties of gases used in the semiconductor industry.

It was virtually, exactly what I was searching for."

Bob Rathfelder
Project Engineer,
Parker Hannifin,
Central Engineering.

Goals

NIST will measure the thermophysical properties of the gases used in semiconductor processing. The property data will improve the modeling of chemical vapor deposition (CVD) and the calibration of mass flow controllers (MFCs). As data are acquired, they are promptly being posted as part of an online database at http://properties.nist.gov/semiprop (Fig. 1). The gases and the properties to be studied were identified by industry representatives. The gases include process gases, "surrogate" gases used for calibration, and binary mixtures of process and carrier gases. The required properties include: speed-of-sound, heat capacity, density (equation of state), viscosity, and thermal conductivity. Industry representatives have also recommended targets for the accuracy of the data.

Customer Needs

The Modeling and Simulations section of the 2001 *International Technology Roadmap for Semiconductors* lists "Materials Modeling" as first in a list of "Technology Requirements." The *Roadmap* states that "*Modeling and simulation tools in equipment, process, device, package, patterning, and interconnect are only as good as the input materials parameters. In many cases these parameters are not known. Databases that contain both experimental and, calculated . . . are needed*." The *Roadmap* states that continuing research is needed to obtain experimental data for "transport and thermal constants." This project will generate transport and thermodynamic property data for the gases

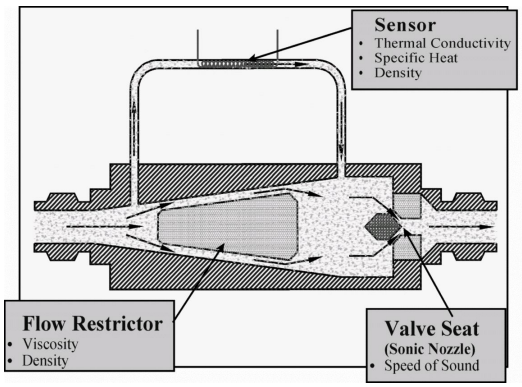

Figure 2. Components of a generic mass flow controller (MFC) and the thermophysical properties required to model them.

Tungsten Hexafluoride — WF_6

M.W. [1]	N.B.P. [2]	T.P. [2]
297.84	290.25 K	275.0 K
P_c [3]	T_c [3]	V_c [3]
4.57 MPa	452.7 K	0.1 m^3/kmol

Return to [Gas Index | Fluid Science Group | Process Measurements Division | NIST Home | SEMI | NSMP]

T K	$\frac{C_P^0(T)}{R}$	Vapor Pressure MPa	$B(T)$ $cm^3 \cdot mol^{-1}$	dB/dT $cm^3 \cdot mol^{-1} \cdot T^{-1}$	$C(T)$ $cm^6 \cdot mol^{-2}$	dC/dT $cm^6 \cdot mol^{-2} \cdot T^{-1}$	λ mW/(m·K)	η μPa·s
Estimated Uncertainty	1%/0.1%	1%	Gas densities are calculated to better than 0.1% over the temperature and pressure ranges of the reference.				10%	10%
Reference	[4]/[5]	[6]	[5]	[5]	[5]	[5]	[5]	[5]
205	11.84	0.19	-2001.6	5951.2	-4658932	47121716	-	-
210	12.00	0.34	-1864.5	5441.0	-3653771	36754361	-	-
215	12.16	0.58	-1741.8	4994.1	-2884907	28924191	5.2	14.17
220	12.66	0.95	-1631.6	4600.8	-2291407	22949084	5.4	14.41
225	12.78	1.53	-1532.2	4252.9	-1829413	18345717	5.6	14.64
230	12.90	2.39	-1442.1	3943.9	-1466994	14767456	5.7	14.88
235	13.03	3.62	-1360.3	3668.3	-1180656	11962851	5.9	15.11

Figure 1. Sample Web Page from database located at the URL http://properties.nist.gov/semiprop/

used in semiconductor processing. The data will be useful for equipment modeling in CVD processes and the data will also provide a rational basis for the calibration of MFCs used to meter process gases.

Figure 2 shows the components of a generic MFC and the thermophysical properties required to model their performance. During May 2000, a workshop entitled "Mass Flow Measurement and Control for the Semiconductor Industry" was organized at NIST by Dr. Robert Berg. At the workshop, representatives of industry identified the gas properties and their allowable uncertainties which are required for accurately modeling MFCs and related equipment. The workshop's list of properties is: heat capacity at constant pressure $C_p(T)$ (±0.1 %), equation of state $\rho(T,p)$ for predicting gas densities (±0.1 %), viscosity $\eta(T)$ (±0.5 %), and thermal conductivity $\kappa(T)$ (±0.5 %). The workshop urged that values of these properties be made available from a 'standard' source that is accessible to all of the industries associated with semiconductor processing.

Technical Strategy

In the first phase of the work, NIST is measuring the speed of sound $u(T, p)$ in process gases and in the surrogate gases that are often used for calibration. The speed-of-sound data have standard uncertainties of $0.0001 \times u$. The initial results range up to 200 °C and from 25 kPa to 1500 kPa (or to 80 % of the vapor pressure for condensable gases). As an example, Figure 3 shows the phase diagram of trimethyl gallium. Each triangle on Figure 3 indicates values of $u(T, p)$ where a speed-of-sound measurement was made. The speed-of-sound data were used to determine the idealgas heat-capacities $C_p^0(T)$ with the targeted uncertainty of $0.001\times C_p^0$. The pressure and temperature-dependence of $u(T, p)$ were correlated with model two-body and three-body intermolecular potentials. These potentials are used to calculate the virial equation of state $\rho(T, p)$ and to get first estimates of the viscosity $\eta(T)$ and the thermal conductivity $\kappa(T)$. For gases where reliable data exist, we verified that results calculated in this way have uncertainties that are less than $0.001\times\rho$, $0.1\times\eta$, and $0.1\times\kappa$ from 200 K to 1000.

In parallel with measuring the speed of sound, NIST is developing novel acoustic techniques to measure the viscosity and thermal conductivity with uncertainties of less than 0.5 % as specified

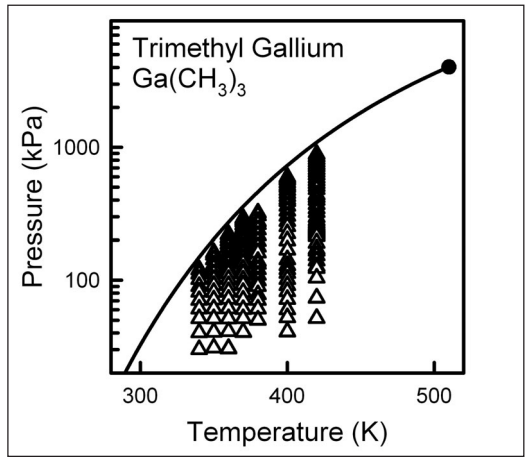

Figure 3. Phase diagram of trimethyl gallium. The vapor pressure is represented by the curved line which ends at the critical point: $T_c \approx 510$ *K and* $p_c \approx 4.4$ *MPa. At each triangle, the speed of sound was measured.*

by the Mass Flow Controller Workshop. Throughout the project, the results will be made available to the customers through publications in professional journals, presentations at professional meetings, and via an on-line data base accessible through the internet at http://properties.nist.gov/semiprop.

DELIVERABLES: Design and fabricate a facility capable of measuring the speed of sound in the hazardous gases utilized in semiconductor processing. Completed 2Q 2000.

1. NIST has already developed techniques to accurately measure the speed of sound in gases and to determine the ideal-gas heat-capacity and the equation of state from the $u(T, p)$ data. NIST used these techniques to determine the thermodynamic properties of alternative refrigerants. Because the alternative refrigerants are inert and non-hazardous by design, modifications are needed to study the reactive, corrosive, and/or toxic gases used in semiconductor processing. These modifications address the issues of safety, sample purity, sample disposal, and materials compatibility.

DELIVERABLES: Develop and optimize novel acoustic techniques for measuring the transport properties of semiconductor process gases. Viscometer designed, fabricated and optimized by 1Q 2002, thermal conductivity device designed by 2Q 2002, fabricated by 4Q 2002, and optimized by 2Q 2003.

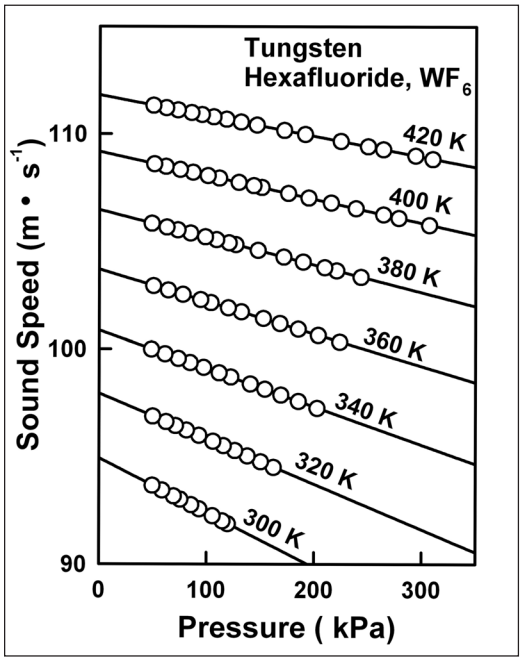

Figure 4. Speed of sound in tungsten hexafluoride as a function of pressure along isotherms.

2. Because conventional measurements of the transport properties of dilute, corrosive gases are difficult, we are developing acoustical methods of measurement. As suggested by M. Greenspan, the acoustical viscometer is a double Helmholtz resonator. The viscosity is deduced from the viscous damping of gas oscillating at acoustic frequencies through a tube joining two chambers. A second resonator will be developed to obtain the thermal conductivity from measurements of the thermal losses of similar oscillations.

DELIVERABLES: Design and fabricate a facility capable of safely measuring the transport properties in the hazardous gases utilized in semiconductor processing. Facility installed by 1Q FY2002, viscometer installed in facility by 2Q FY2002, automation software written and tested by 3Q FY2002, design and fabricate hazardous gas viscometer by 3Q FY2002, install hazardous gas viscometer by 4Q FY2002, design and fabricate hazardous gas thermal conductivity device by 2Q FY2003.

3. A second facility to measure the transport properties will have to be fabricated taking into account the same issues of safety, sample purity, sample disposal, and materials compatibility as for the speed-of-sound facility.

DELIVERABLES: Measure the speed of sound in the semiconductor process gases identified by the customers. From the speed-of-sound measurements determine the ideal-gas heat-capacity and equation of state for each species. Nitrous oxide by 1Q 2002, Nitric Oxide by 2Q 2002, Octafluoro-cyclobutane by 4Q 2002.

DELIVERABLES: Measure the transport properties in the semiconductor process gases identified by the customers. C_2F_4 by Q3 2002, CF_4 by 4Q 2002, SF_6 by 1Q 2003, NO by Q2 2003, NO_2 by 3Q 2003.

4. Once the two facilities have been fabricated, calibrated and safety assessments performed the actual measurements in the semiconductor process gases identified by the customers will be performed.

Table 1. Ranges of speed-of-sound data for process gases.

	Temperature Range (K)	Maximum Pressure (kPa)
Cl_2	260 – 440	1,500
HBr	230 – 475	1,500
BCl_3	300 – 460	1,500
WF_6	290 – 420	300
C_2H_4O	285 – 440	1,000
NF_3	200 – 425	1,600
$Ga(CH_3)_3$	340 – 420	900
N_2O	220 – 460	1,600
NO	200 – 450	1,600

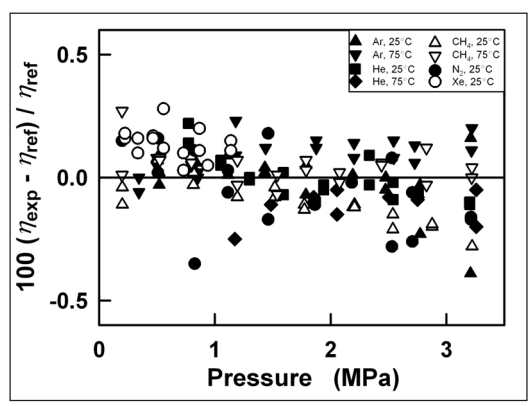

Figure 5. Percent deviation of viscosity measurements made in the Greenspan viscometer from the reference values in several gases.

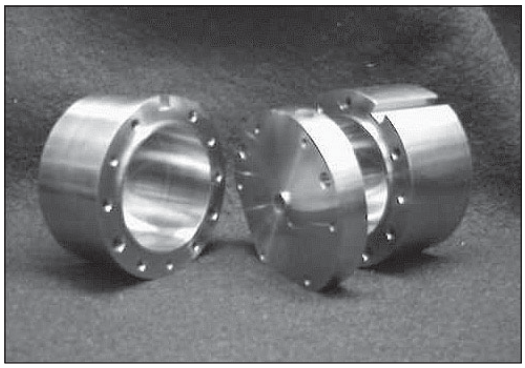

Figure 6. Monel Greenspan acoustic viscometer for use with corrosive process gases.

DELIVERABLES: Disseminate the resulting measurements to the customer. Update on-line database by 4Q 2002, publish measurements in Cl_2 by 1Q 2002, publish measurements in $Ga(CH_3)_3$, C_2H_4O, and NF_3 by 3Q 2002, publish measurements in NO and NO_2 by 1Q 2003.

5. The measurements will be disseminated to the customer through papers in professional journals, talks given at professional meetings, and on an on-line database available via the internet.

Accomplishments

■ A facility was built to safely measure the speed of sound in semiconductor process gases. The apparatus was calibrated with argon. The speed of sound was measured in the surrogate gases CF_4, C_2F_6 and SF_6.

■ Computer programs were developed for correlating speed-of-sound data with model, hard-core Lennard-Jones intermolecular potentials. Programs were developed to calculate second and third virial coefficients and transport properties from the model intermolecular potentials.

■ The speed of sound was measured in the process gases Cl_2, HBr, BCl_3, WF_6, $Ga(CH_3)_3$, NF_3, C_2H_4O, NO, and N_2O throughout the temperature and pressure ranges listed in Table 1. Figure 4 shows a fraction of the results for WF_6. Typically, the standard uncertainty of the speed of sound was less than 0.01 %. The ideal-gas heat-capacity was determined to within 0.1 % from the zero-pressure intercept of each isotherm. The slope and curvature of each isotherm provided information about each gas's non-ideality from which we developed an equation of state to predict the gas's densities to within 0.1 %. This year we will complete measurements in C_4H_6 and octafluoro-cyclobutane.

■ The Greenspan acoustic viscometer was developed to measure the viscosity of process gases. Several viscometer geometries and acoustic models were tested to optimize the viscometer's performance. The performance of the acoustic viscometer was tested by comparing the acoustic results for several gases with reference data from the literature. Figure 5 shows that the data from the acoustic viscometer are within 0.5 % of the from reference values. We have measured the viscosity in the three surrogate gases CF_4, C_2F_6 and SF_6 as well as the hazardous semiconductor gases N_2O and NF_3.

■ A second generation Greenspan viscometer has been designed and will be assembled this year. The new version is being constructed out of Monel which will allow the study of the corrosive process gases. Figure 6 shows the parts of the new resonator before their final assembly.

■ A data base available on the internet at the URL http://properties.nist.gov/semiprop/ has been developed (Figure 1). This data base is updated regularly to give our customers immediate access to our results.

Recent Publications

Hurly, J. J., "Thermophysical Properties of Gaseous CF_4 and C_2F_6 from Speed-of-Sound Measurements," *International Journal of Thermophysics*, Vol **20**, No 2, 455-484, September 1999.

Hurly, J. J., and Moldover, M. R., "Thermophysical Properties of Process Gases," Proceedings of SEMICON West 1999.

Hurly, J. J., "Thermophysical Properties of Gaseous HBr and BCl_3 from Speed-of-Sound Measurements," *International Journal of Thermophysics,* Vol.21, No. 4, 805-829, July 2000.

Hurly, J. J., "Thermophysical Properties of Gaseous Tungsten Hexafluoride From Speed-of-Sound Measurements," *International Journal of Thermophysics*, Vol. 21, No. 1, 185-206, January 2000.

Hurly, J. J., "A Progress Report: Thermophysical Properties of Semiconductor Manufacturing Process Gases," Proceedings of SEMICON West 2000.

Hurly, J. J., "The Thermodynamic Properties of Chlorine From Speed-of-Sound Measurements," Vol. 23, No. 3, 667-695, May 2002.

Hurly, J. J., "Thermophysical Properties of Nitrogen Trifluoride, Ethylene Oxide, and Trimethyl Gallium from Speed-of-Sound Measurements," Vol. 23, No. 2, 455-475, March 2002.

Moldover, M. R., Gillis, K. A., Hurly, J. J., Mehl, J. B., and Wilhelm, J., "*Chapter 10. Acoustic measurements in gases.*", in Modern Acoustical Techniques for the Measurement of Mechanical Properties, edited by Moises

Levy and Henry E. Bass, pp 377-427 (Academic Press, San Diego, USA, 2001); also "*Chapter 12: Acoustic measurements in gases: Applications to thermodynamic properties, transport properties, and the temperature scale"*, Vol IV, in Handbook of Elastic Properties of Solids, Fluids, and Gases, edited by M. Levy, H. Bass, and R. Stern, pp 329-370 (Academic Press, San Diego, USA, 2000).

Wilhelm, J., Gillis, K. A., Mehl, J. B. and Moldover, M. R., "An improved Greenspan viscometer," Int. J. Thermophysics, Int. J. Thermophysics, Vol 21, pp. 983-997 (2000).

List of Talks/Presentations

Hurly, J. J., "Progress Report: Thermophysical Properties of Semiconductor Manufacturing Process Gases," delivered to the Gas Distribution Systems Working Group, Sunday July 15, at the SEMICON west 2000 conference in San Francisco, CA.

Hurly, J. J., "Thermophysical Properties of Semiconductor Process Gases," delivered to the European SEMI Technical Gas Committee, September 21, 2000, at Oostende Belgium.

Hurly, J. J., "Thermophysical Properties of Semiconductor Process Gases Determined with Acoustic Techniques," delivered at the Fourteenth International Symposium on Thermophysical Properties, June 28, 2000.

Temperature Measurements and Standards for Rapid Thermal Processing

Technical Contact:
K. G. Kreider
D. P. DeWitt
B. K. Tsai

Goals

The goal is to develop the technologies required to enable the measurement of Rapid Thermal Processing (RTP) wafer absolute temperatures with uncertainties of 2 °C at 1000 °C as prescribed in the International Technology Roadmap for Semiconductor (ITRS).

Our project, initiated in FY97, has approached this goal with four objectives: (1) To improve calibration wafer technology to a 1 °C standard uncertainty by demonstrating the use of thin-film thermocouples (TFTCs) in conjunction with wire thermocouples (TCs) on test wafers, in Fig. 1, RTP tools; (2) To develop methods for in-tool radiation thermometer (RT) calibration, which relate TFTC wafer temperatures to indicated radiance temperatures; (3) To develop and validate models to account for wafer emissivity and the effects of chamber reflected-irradiation on temperatures determined from model-corrected RTs that are calibrated against blackbodies; and (4) To collaborate with the semiconductor industry in implementing new methods for reliable and traceable temperature measurements.

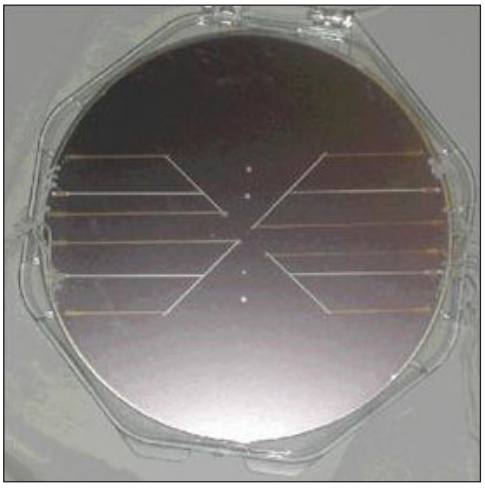

Figure 1. NIST thin-film thermocouple calibration wafer used in lightpipe proximity evaluations after 41 thermal cycles above 800 °C.

Customer Needs

The measurement needs of the semiconductor manufacturing industry have been stated in the ITRS. The requirement is for measurement and control of RTP tools to ± 2 °C at 1000 °C during processing with calibrations traceable to the International Temperature Scale of 1990 (ITS-90). *In the 2001 edition of the ITRS in the section on "Metrology Difficult Challenges" the roadmap states "Better sensors must be developed for . . . wafer temperature measurement during RTA."*

Our customers are the device manufacturers and the suppliers of thermal processing equipment and temperature measurement instrumentation. This community forms our project's Common Interest Group (20 companies meeting annually at NIST since 1997). They serve as a bridge between research and practice, provide advice on shaping objectives, and generate opportunities for technology transfer. ISMT has established a joint effort at UT-Austin, with NIST and several instrument suppliers, to develop a facility to evaluate and validate accuracy claims of commercial thermometry systems. In addition Applied Materials and Atmel are evaluating the NIST test wafer.

Technical Strategy

Our strategy is to address three core elements of our research that will enable the semiconductor industry to meet the road map requirement: (a) fabrication of test wafers with improved thin-film technology for use by our industrial collaborators to demonstrate in-tool calibration of RTs traceable to the ITS-90; (b) experimentation on the NIST test bed and thermal modeling to determine the effects of wafer emissivity and lightpipe proximity on in-tool calibration of lightpipe radiation thermometers (LPRTs); and, (c) calibration and characterization of LPRTs.

The present scope of the TFTC technology work includes designing, fabricating, and testing thin-film thermocouple calibration wafers for use in industrial RTP tools, defining the effects of various wafer and film emissivities as well as sensor arrangement on the temperature measurement, and establishing the uncertainty of the temperature measurements using the NIST calibration wafer.

We are using the NIST Test Bed to perform inter-comparisons between the TFTCs and LPRTs. The aims are: (a) to demonstrate calibration procedures for and establish uncertainties of the LPRTs against the TFTCs, and (b) to establish uncer-

tainties for model-corrected LPRTs calibrated against blackbodies. Experimental studies are being designed for these conditions: a range of wafer and film emissivities, variable separation distance between wafer and cold shield, different distances between the LPRT and wafer, and variable chamber wall reflectance. These studies require concurrent efforts to develop and validate radiation heat transfer models to estimate wafer effective emissivities that are essential for establishing uncertainty limits for LPRTs in our test bed, and in production tools.

DELIVERABLES: Evaluation of wafer emissivity and paper on LPRT proximity effects on wafer temperatures. 2Q 2003

We are using industrial RTP test beds to establish the usefulness of the NIST calibration wafer in the semiconductor processing industry and to define the benefits of using the NIST calibration wafer under various industrial conditions.

A cooperative project with ISMT and the University of Texas at Austin (UT-Austin) uses their RTP test bed, which has very high uniformity in wafer temperatures and can be used to confirm the uncertainties and repeatability of the NIST calibration wafer. Their test bed also is used to compare the NIST wafer with commercial thermocouple test wafers and industrial lightpipe radiation thermometers.

DELIVERABLES: NIST TFTC calibration wafers for ISMT test bed and joint report with UT-Austin on LPRT calibrations. 2Q 2003

Cooperative projects with Applied Materials and Atmel industries are permitting investigations of the use of the NIST calibration wafers in industrial RTP tools. These evaluations are critical for transferring the NIST developments to the semiconductor processing industry. The NIST thin-film thermocouple calibration wafer has demonstrated unique capabilities in temperature measurements and in establishing traceability to the international temperature scale (ITS-90).

DELIVERABLES: NIST TFTC calibration wafers for RTP temperature measurements and joint report with Applied Materials and Atmel on LPRT calibrations. 3Q 2003

Common Interest Group (CIG) meetings have been held annually since 1997 for the purposes of assessing and planning project research directions, and for fostering collaborative work with equipment suppliers, chip makers, and instrumentation suppliers. At the 10th International Conference on Advanced Thermal Processing of Semiconductors (RTP'02, Sept. 25-27, 2002, Vancouver, Canada) the meeting addressed two major themes: reports by our industrial collaborators on test wafer demonstrations and discussions on proposals for establishing emissivity-standard wafers. At RTP'03 (Sept. 24-26, 2003, Charleston, South Carolina), our team will organize two regular conference sessions under the theme of traceability of RTP temperature measurements. Papers will be presented on TC and RT calibrations methods and thermal modeling. A panel will discuss plans for an industry-wide emissivity standards initiative. An important contribution by NIST to the initiative is the use of the high temperature properties measurement facilities to generate a reliable, traceable data base and to validate optical properties models.

DELIVERABLES: Organize and conduct Common-Interest Group meeting on traceable temperature measurements at key industry RTP conference. 4Q 2003.

Accomplishments

Emissivity Effects

We investigated the effect of different silicon wafer emissivities and the effect of low emissivity films on RTP wafer temperature measurements using LPRTs. These tests were performed in the NIST RTP Test Bed. We used a NIST TFTC calibration wafer to calibrate the LPRTs *in situ.* The measurements of LPRTs viewing Au and Pt thin-film spots in the center of the wafer were compared to LPRT radiance temperature readings that viewed silicon surface with thermal oxide film. We found differences of up to 36 °C at 900 °C in the LPRT measurements due to the low emissivity films. A model of the wafer temperature measurement was presented to provide insight into the effects of wafer emissivity on LPRT measurements in RTP tools.

Thermal Modeling: Emissivity Effects

A thermal model of the wafer and cold shield enclosure has been developed and employed to predict the effects of NIST Test Bed-chamber features on LPRT measurements. The thermal response of the wafer was predicted for different thin-film spot, wafer emissivity, and shield reflectivity. The thin-film spot resulted in a temperature rise at the center of the wafer and its magnitude was strongly dependent on the shield reflectivity and less dependent on the wafer

emissivity. The effects of the lightpipe sensor on the temperature distribution of the wafer were also investigated. Due to its low reflectivity compared with the cold shield, the lightpipe sensor caused a temperature decrease at its viewing area, which is a strong function of the shield reflectivity.

Lightpipe Proximity

Our Common Interest Group indicated the need for a better understanding of the lightpipe radiation thermometer (LPRT) location on wafer temperature measurement. The lightpipe is a sapphire rod of 2 mm diameter surrounded by a 4 mm diameter sapphire sheath and has a very low reflectivity (0.1) compared to the surrounding reflecting plates of the cavity facing the wafer. Shown in the accompanying schematic, Fig. 2, is the wafer-cold shield enclosure with the light pipe at a proximity distance *p*. The effect of the light pipe is to cause a temperature depression over the wafer, which can significantly influence the temperature indicated by the radiation thermometer.

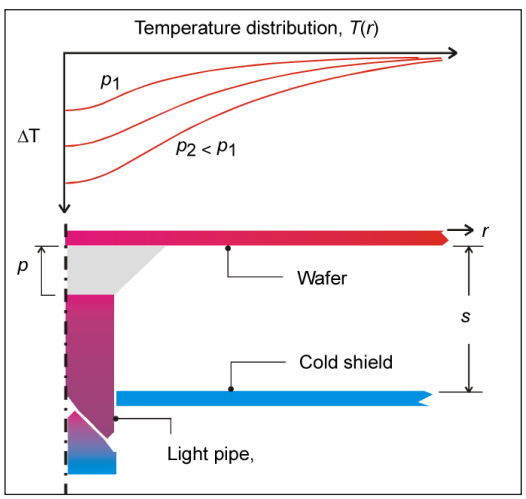

Figure 2. Schematic of wafer-cold shield enclosure with lightpipe at proximity distance p and temperature depression due to lightpipe proximity from model above.

We designed an experimental and analytical study to quantify the lightpipe proximity effect and provide a model for industrial users of LPRTs to correct their LPRT readings. The experiments employed thin-film thermocouple wafers, our RTP test bed, and LPRT readings to characterize the effects of lightpipe proximity on wafer temperatures. We used various distances between the wafer and the reflecting plate and various distances between the wafer and the tip of the lightpipe to quantify the wafer temperature depression.

Figure 3 shows the comparison of the temperature depression caused by various wafer to lightpipe distances, p, with the reflecting plate to wafer distance of s = 10 mm. Dashed and solid lines in the figure represent the model's predictions at 6 mm and 3 mm. This temperature depression is compared to the measurement made with the lightpipe flush with the reflecting plate. It can be seen that the wafer temperature can be depressed more than 20 °C by positioning the lightpipe tip too close to the wafer. These results were presented in a paper for the 2003 International Conference on Characterization and Metrology for ULSI Technology on March 27. An expanded paper on the same subject will be presented at the RTP conference in September.

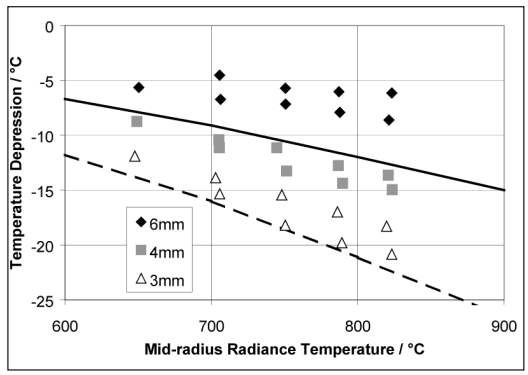

Figure 3. Change in central radiance temperature due to the proximity of center lightpipe to the wafer.

Lightpipe Characterization

Our objective was to investigate improved procedures for characterization and calibration of sapphire lightpipes using uniform blackbody sources. We evaluated spectral, spatial, and temporal characterizations of LPRTs to obtain critical information on effective wavelength and field of view, as well as stability information required for making accurate temperature measurements and uncertainty assessments. We reported guidelines for making qualitative and quantitative inspections of the sapphire lightpipes. Proper inspections of the lightpipes can assist the user in identifying lightpipes that will have poor performance before using them in RTP tools. We also compared "cold" calibrations done in less than 5 s and "hot" calibrations taking about 30 min and discovered that the difference between "cold" and "hot" calibrations can be as much as 2.5 °C in some situations. We offered caution for utilizing information received in factory

calibration reports. A comparison of three vendors showed that the differences between the factory calibration and the NIST calibration were as much as 7.6 °C. We disseminated a list of recommendations for the lightpipe user to assist them in performing more useful characterizations and accurate calibrations.

Recent Publications

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Low Concentration Humidity Standards

Goals

The primary objective is to establish quantitative standards enabling the accurate measurement of trace quantities of water vapor (< 10^{13} molecules cm^{-3}). This effort supports the development and application of commercial humidity sensors used for gas purity measurements and inline monitoring and process control – functions that are relevant to minimizing wafer misprocessing.

Customer Needs

As discussed in the 2001 International Technology Roadmap for Semiconductors (ITRS) in the chapter entitled Metrology, the evolution of sensor-based metrology for integrated manufacturing requires the development of in-situ sensors enabling in-time measurements. In Table 96 entitled Metrology Difficult Challenges, the need for robust and accurate sensor technology and impurity detection in starting materials is highlighted. Of the known impurities in processing gases, water vapor is one of the most ubiquitous and difficult to eliminate. Thus its measurement and control is often critical to various semiconductor-related processes.

Although a variety of high sensitivity sensors of water vapor are available, most do not directly measure water in the gas phase. Rather they typically respond to moisture-induced changes in bulk or surface properties associated with the adsorption of water vapor. Consequently, a rigorous first-principles determination of sensor response is often precluded, thus compromising accuracy. Moreover, since many such devices exhibit drift and poor reproducibility, frequent recalibration is required. Interpretation of these measurements is also complicated by complex physical interactions of water vapor with technical surfaces in transfer lines, in reaction chambers and in sensor housings.

Technical Strategy

The development of accurate and robust water vapor sensors requires well-characterized reference standards against which such devices can be evaluated. This should include a primary method of measurement for water vapor concentration and a complementary method yielding high-precision and stable sources of water vapor. By providing access and traceability to the unique capabilities at NIST discussed below, instrument manufacturers and sensor users can assess the overall performance and accuracy of their measurements.

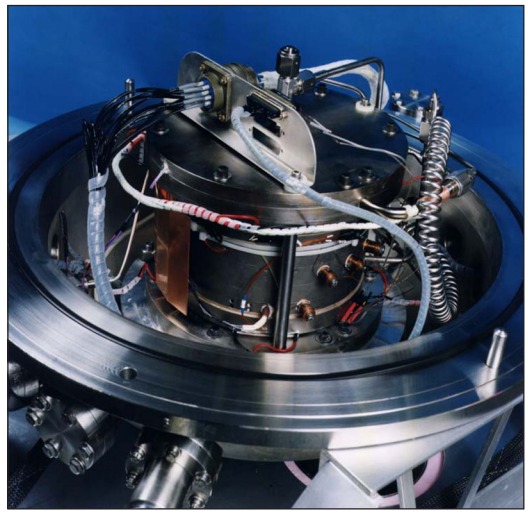

Figure 1. NIST Low Frost-Point Humidity Generator.

Our strategy is to establish complementary capabilities in high-precision generation and measurement of water vapor. To address these respective needs, we have developed a thermodynamically based humidity source and high-sensitivity optical absorption measurement methods discussed below. The thermodynamic humidity source, known as the Low Frost-Point Generator (LFPG), see Fig. 1 and Fig. 2, serves as the project cornerstone and is capable of delivering 3 mmol to 3 nmol of water vapor per mole of dry gas. Here the water vapor concentration in a gas stream is precisely controlled by active regulation of the saturator temperature and pressure. As such, the LFPG is

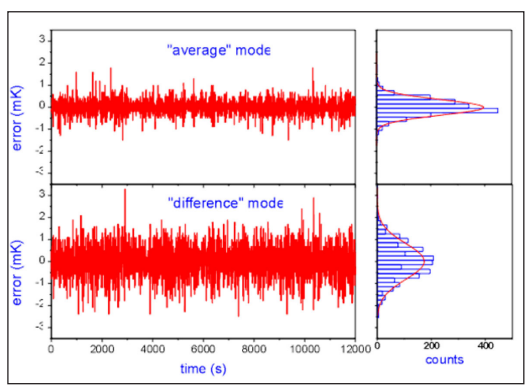

Figure 2. Steady state response of saturator control thermometers in NIST Low Frost-Point Humidity Generator.

Technical Contacts:
J. T. Hodges
G. E. Scace

"The LFPG is the 'Gold' standard for moisture generation and after the round robin experiments it is possible for the industry to talk about moisture measurements that can be compared to the standard."

Suhas Ketkar,
Air Products and Chemicals

ideally suited for testing the performance of various sensing and humidity generation technologies. To date, it is has been used to characterize water vapor measurement and generation systems at the research and development stage as well as commercial devices.

1. A common technology used by the semiconductor industry for delivering controlled quantities of water vapor is based upon the controlled permeation of water vapor (called permeation tube generator (PTG)) through a material, followed by mixing and dilution with a dry gas of known flow rate. We recently constructed a calibration system for water permeation tubes, comparing permeation tubes to the LFPG using a commercial water vapor sensor as a nulling device. This approach constitutes an efficient and low-cost mechanism for the dissemination of NIST trace humidity standards. To meaningfully characterize the long-term stability of this system and its combined uncertainty, measurements of the system performance must be taken over an extended time frame.

DELIVERABLES: Complete system testing and uncertainty analysis of permeation-tube calibration system. 3Q 2003

2. The basis for the LFPG as a humidity standard is knowledge of the temperature-dependent ice vapor pressure. The most commonly used correlation is that developed by Wexler of NBS. This correlation is generally considered valid to a minimum temperature of -100 °C. Recent comparisons in our laboratory with independent humidity generation techniques suggest that the actual ice vapor pressure may differ from that predicted by the Wexler correlation by an amount exceeding the expected uncertainty. Further, to use the LFPG at temperatures below -100 °C requires extrapolation of this correlation, with the risk of large uncertainties. We expect to quantify important deviations from the Wexler ice-vapor pressure correlation, and extend its useful range to -110 °C.

DELIVERABLES: Refine and extend the temperature-dependent ice vapor pressure correlation. 1Q 2004

3. The LFPG is currently limited to generating greater than 3 nmol mol^{-1} of water vapor in N_2 based on the minimum achievable temperature of the saturator, and knowledge of the ice vapor pressure discussed above. A new strategy for pmol mol^{-1} -level humidity generation has been identified. The approach involves the controlled dilution of water vapor/gas mixtures produced by the LFPG, using a flow dilution system similar to that incorporated within the PTG calibration system described above.

DELIVERABLES: Extend the LFPG to pmol mol^{-1} levels of humidity generation. 2Q 2004

4. To complement our established capability in precision generation of trace humidity levels, we are developing absolute techniques based upon the absorption of visible and near-infrared laser radiation. Water vapor has an absorption spectrum comprising thousands of distinct rovibronic absorption transitions in this spectral region. Thus, the concentration of water vapor can be readily determined in terms of measurements of sample absorbance and independently determined absorption line strengths. Recent advances in source and detector technology, and new spectroscopic techniques that extend the sensitivity of laser absorption measurements now enable the precise sensing of water vapor at concentrations below 10^{10} molecules cm^{-3}. To account for line broadening effects, and mitigate interference effects associated with absorption by other species the most precise absorption measurements require that individual transitions be spectrally resolved. This demands a technique having a frequency resolution much smaller than the characteristic widths of the absorption transitions, and requires that the frequency intervals in the measured spectrum be accurately determined. By combining high spectral resolution with high precision absorbance measurements, the water vapor concentration can be found independently of the composition of the carrier gas. Of the optical absorption methods, cavity ring-down spectroscopy (CRDS) is expected to be the most suitable for a primary method. CRDS is a cavity-enhanced optical absorption technique that has high sensitivity, fast response, and probes a compact well-defined volume. It is important to emphasize that under certain conditions, CRDS can exhibit exceptional spectral resolution, enabling detailed measurements of absorption line shape. To this end, we have developed a refined version of CRDS called frequency-stabilized single-mode cavity ring-down spectroscopy (FSSM-CRDS). Here, the ring-down cavity is actively length stabilized, the probe laser is frequency locked to the ring-down cavity, and the frequency axis of the spectra is based upon the longitudinal mode spacing of the ring-down cavity. See Figure 3 below.

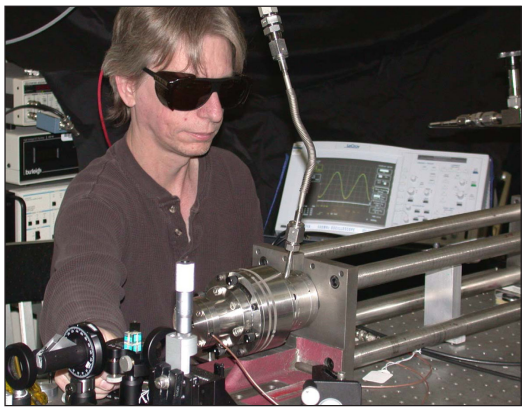

Figure 3. Frequency-stabilized CRDS system.

Figure 4. New PTG calibration apparatus.

Using the existing FSSM-CRDS apparatus, appropriate transfer standard generators and hygrometers, we will link H_2O transition line strengths to thermodynamic-based LFPG. Taking advantage of the high spectral resolution afforded by FSSM-CRDS, pressure-broadening of these transition line shapes by various media will also be quantified.

DELIVERABLES: Link H_2O transition line strengths to LFPG for water vapor concentration measurements in the range 10 nmol mo1^{-1} to 100 µmol mo1^{-1} and measure N_2 pressure broadening coefficients.
4Q 2003

Accomplishments

■ In FY 2003 we constructed a permeation tube calibration facility (see Fig. 4 above). The purpose of this system is to provide measurement traceability for industrial users of permeation tube humidity generators. The calibration system comprises a custom PTG, the LFPG and high-sensitivity quartz crystal microbalance (QCM). The water-containing permeation tubes to be calibrated are placed inside the temperature-stabilized PTG oven. Water vapor diffuses from the tube surface into a precisely controlled stream of purified N_2. The diluent gas flow rate is adjusted so that the water vapor concentration produced by the PTG is equivalent to that produced by the LFPG, as measured by the QCM. From these measurements the water permeation rate of the tube under test can be determined in terms of the known LFPG output. The calibration facility is now operational and being tested to assess its combined uncertainty.

■ A new strategy for pmol mol^{-1} (ppt) -level humidity generation was recently identified. The approach, shown in Fig. 5, involves the controlled dilution of water vapor/gas mixtures produced by the LFPG, using a flow dilution system similar to that incorporated within the PTG calibration system described above.

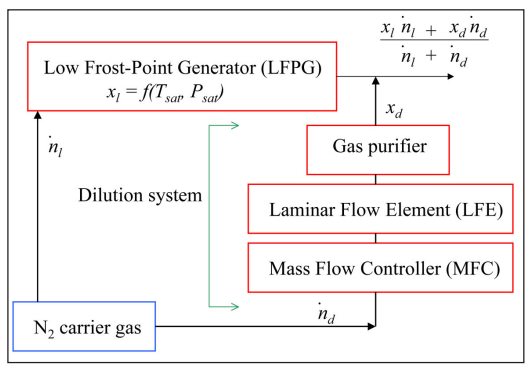

Figure 5. Proposed dilution system for extending the LFPG operating range to pmol mol^{-1} levels.

■ The LFPG uncertainty analysis is based on the uncertainties in temperature and pressure within the LFPG saturator, ice vapor pressure and the enhancement factor for mixtures of water vapor and air. However, this analysis neglects background effects associated with the transient adsorption and desorption of water vapor from internal surfaces in the flow manifold located downstream of the LFPG. For the lowest range considered, such processes may affect significantly the water vapor concentration in the sample gas delivered by the LFPG to test instrumentation. In collaboration with Air Products Inc., we quantified the magnitude of this water vapor background using atmospheric pressure ionization mass spectrometry (APIMS). Results, shown in Fig. 6, indicate that background contribution to H_2O from system components

downstream of the LFPG was less than 0.2 nmol/mol. These measurements also demonstrated that linearity deviations of the LFPG output H_2O mole fraction are less than 0.1 nmol/mol.

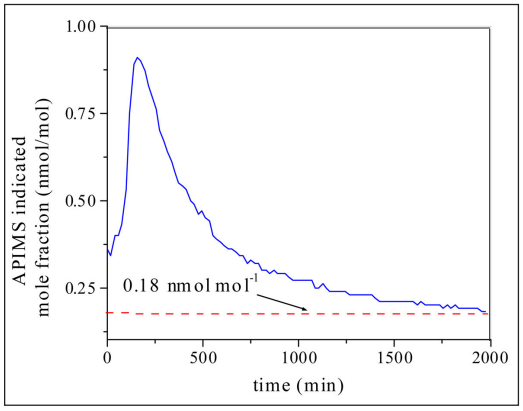

Figure 6. APIMS measurement of LFPG background H_2O concentration showing decay to steady state level.

■ We developed a quantitative method for comparing the outputs of commercial and custom permeation tube moisture generators (PTGs) to that of the LFPG. This technique is capable of resolving fractional differences of approximately 1 %, for PTGs covering the mole fraction range 10 to 100 nmol/mol. An intercomparison of PTG devices from several customers was completed, and results comparing two representative PTGs to the LFPG are summarized in Fig. 7. Uncertainties in flow metering and background water vapor present in the carrier gas were identified as limiting effects. This technique was the basis for newly developed permeation-tube calibration service discussed above.

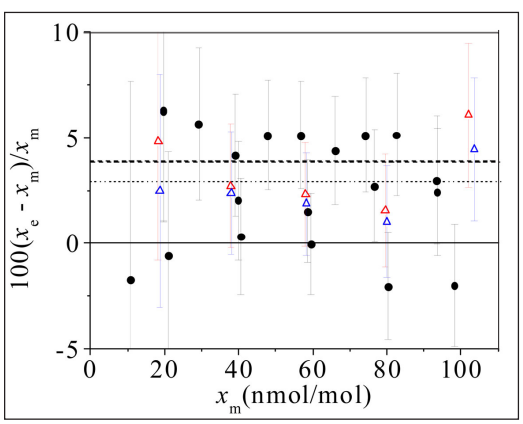

Figure 7. Comparison of results for PTG A *(circles) and PTG* B *(triangles). The dashed curves represent the respective average percent differences between the PTG and the LFPG. Error bars represent 1 standard deviation.*

■ We measured trace levels of water vapor generated by the LFPG using a prototype diode laser hygrometer (DLH). This hygrometer, which was based upon wavelength modulation spectroscopy, had a linearity better than 1 % over the water vapor mole fraction range 3 nmol/mol to 2 µmol/mol and yielded a sensitivity of better than 0.5 nmol/mol when tested against the LFPG. These experiments and subsequent tests on a beta system were critical to the development of a similar DLH that is now commercially available.

■ We recently completed the development of a FSSM-CRDS system, based on a near-infrared continuous wave diode laser emitting near 936 nm. The gas sampling system is optimized for high-precision measurements of trace water vapor concentration. The flow system has all-metal seals, low dead volume, and active mass flow rate and pressure regulation. Background levels < than 0.5 nmol mol^{-1} (background equivalent) have been demonstrated. A FSSM-CRDS spectrum of atmospheric H_2O is shown in Fig. 8, corresponding to a mole fraction of approximately 8 µmol mol^{-1} and concentration of 2.7×10^{13} molecules cm^{-3}. The spectral resolution of the FSSM-CRDS spectrum is approximately 1 MHz, and permits high precision line shape determinations that are not instrument-limited. To illustrate, systematic deviations from commonly used Voigt line shapes are observable with this system, suggesting its utility for fundamental studies of collision-induced line shape phenomena. Other results indicate that the integrated CRDS spectra scale linearly with H_2O concentration, and transition line strengths can be reproducibly determined to within 0.5 %. Also, detection limits less than 10 nmol mol^{-1} of H_2O in N_2 have been demonstrated, using the relatively weak absorption lines near 935 nm accessible with the near-ir diode laser used in this system. Finally, a replica of the FSSM-CRDS system is now used to characterize the purity of semiconductor source gases in a molecular beam epitaxy (MBE) facility at NIST-Boulder.

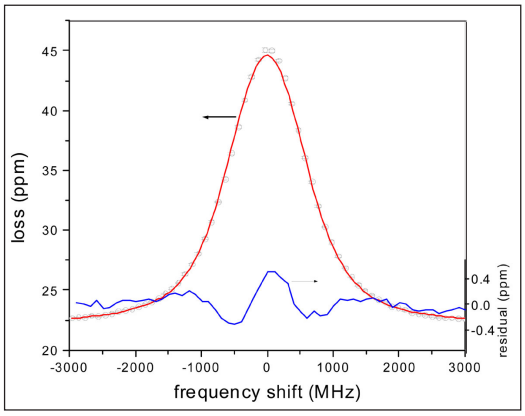

Figure 8. High-resolution FSSM-CRDS spectrum of pressure-broadened H_2O rovibronic transition at 10687.36 cm^{-1}. The open circles are the measured losses, and the red solid line is a Voigt fit to the measured profile. The blue line represents the fit residuals.

Collaborations

Air Products and Chemicals Inc., Seksan Dheandhanoo; APIMS measurements of trace moisture and characterization of semiconductor gas purity.

NIST Optoelectronics Division, Kris A. Bertness; CRDS measurements of H_2O in III-V compound process gases.

Dow Chemical, Linh Le and J. D. Tate; CRDS measurements for process gas control RH Systems, Robert Hardy; Characterization of low range chilled-mirror hygrometers.

Southwest Sciences Inc, Chris Hovde.; Development of wavelength modulation laser hygrometer for trace H_2O sensing.

Recent Publications

J. T. Hodges, J. P. Looney and R. D. van Zee, "Response of a ring-down cavity to an arbitrary excitation," J. Chem. Phys., **105**, 10278-10288 (1996).

G. E. Scace, P. H. Huang, J. T. Hodges, D. A. Olson and J. R. Whetstone, "The new NIST low frost-point humidity generator," National Conference of Standards Laboratories, Proceedings of the 1997 Workshop and Symposium, 2, 657-673, July 27-31, 1997, Atlanta, GA.

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G. E. Scace, D. C. Hovde, J. T. Hodges, P. H. Huang, J. A. Silver and J.R. Whetstone, "The NIST Low Frost-Point Humidity Generator: A New Standard for Trace Humidity Measurement," Workshop on Gas Distribution Systems, Semicon West 98, San Francisco, CA, July 12, 1998.

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J. P. Looney, J. T. Hodges and R. D. van Zee, "Quantitative absorption measurements using cavity-ringdown spectroscopy with pulsed lasers," Chapter 7, in *Cavity-Ringdown Spectroscopy-A New Technique for Trace Absorption Measurements*, ed. K. W. Busch, American Chemical Society Symposium Series No. 720 (1999).

R. D. van Zee, J. T. Hodges and J. P. Looney, " Pulsed, single-mode cavity ring-down spectroscopy," Appl. Opt., **38**, 3951-3960, 1999.

D. C. Hovde, J. T. Hodges, G. E. Scace, J. A. Silver, "Wavelength-modulation laser hygrometer for ultrasensitive detection of water vapor in semiconductor gases," Appl. Opt., **40**, 829-839 (2001).

G. E. Scace, and J. T. Hodges, "Uncertainty of the NIST low frost-point humidity generator," Proceedings of the 8th International Symposium on Temperature and Thermal Measurements in Industry and Science, June 19-21, 2001, Berlin, Germany.

P. H. Huang, G. E. Scace, and J. T. Hodges, "Measuring technique for quantifying performance of dilution-based trace moisture generators," Proceedings of the 8th International Symposium on Temperature and Thermal Measurements in Industry and Science, June 19-21, 2001, Berlin, Germany.

J. G. Cormier, J. T. Hodges and J.R. Drummond, "On the Application of Cavity Ringdown Spectroscopy to Measurements of Line Shapes and Continuum Absorption," in SPECTRAL LINE SHAPES: 16th International Conference on Spectral Line Shapes (Volume 12), AIP Conference Proceedings 645, ed. Christina A. Back, pp.401-412 (2002).

S. Y. Lehman, K. A. Bertness and J. T. Hodges, "Detection of trace water in phosphine with cavity ring-down spectroscopy," Jour. of Crys. Growth, **250,** 262-268 (2003).

Plasma Process Metrology

Technical Contacts:
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K. Steffens
E. Benck

"NIST is one of the leaders in plasma processing related research in the US. They have capability to thoroughly understand plasma behavior using a variety of diagnostics tools."

Peter Ventzek
Motorola

"The NIST plasma process metrology group has helped us to understand the fundamental physical and chemical processes that are important to electronics materials and semiconductor processing industries."

Bing Ji,
Air Products and Chemicals, Inc.

Goals

To provide advanced measurement techniques, data, and models needed to characterize plasma etching and deposition processes important to the semiconductor industry, enabling continued progress in model-based reactor design, process development, and process control.

Customer Needs

To fabricate future generations of devices, the semiconductor industry requires improvements in plasma etching and deposition processes. Plasma processes and equipment face increasingly stringent requirements due to the need to maintain high device yields at decreasing feature sizes, the introduction of new dielectric materials, and the constant pressure to keep production efficiency high. To meet these challenges, the International Technology Roadmap for Semiconductors (ITRS) identifies a need for better predictive system modeling. To obtain more reliable predictions of the chemical, physical, and electrical properties of processing plasmas, further progress in model development and validation is required. ITRS also identifies a need for improvements in intelligent process monitoring and control, which require the development of robust and reliable sensors that are compatible with manufacturing equipment.

Technical Strategy

Our multifaceted program provides numerous outputs to assist our customers, including advanced measurement methods, high-quality experimental and fundamental data, and reliable, well-tested models of plasma behavior.

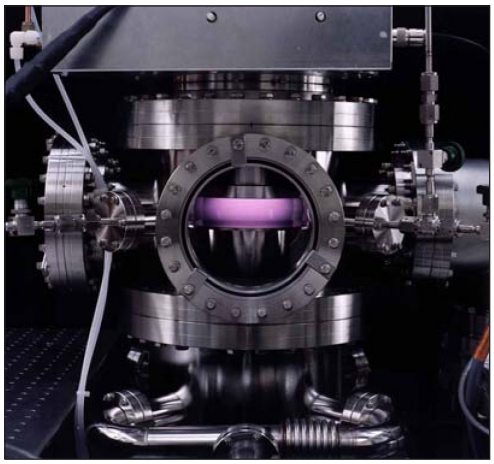


Figure 1. One of the inductive, high-density plasma reactors used in our experimental studies.

First, we develop and evaluate a variety of *measurement techniques* that provide industry and academia with methods to characterize the chemical, physical, and electrical properties of plasmas. The techniques we develop include improved laboratory diagnostic measurements for use in research and development, as well as more robust, non-perturbing measurements for use in process monitoring and control in manufacturing applications. See Fig. 1 for a photograph of one of our plasma reactors.

In addition to measurement techniques, we also provide *data* necessary for gaining an understanding of complex plasma properties and for testing and validating plasma models. The data help semiconductor manufacturers and plasma equipment manufacturers to better understand and control existing processes and tools and help them to develop new ones. The experimental data we provide are measured under well-defined conditions in highly-characterized standard plasma reactors.

Finally, we are engaged in the development and validation of plasma *models*. Such efforts concentrate on modeling of plasma sheaths, the thin regions at the boundary of the plasma. Sheaths play a dominant role in determining discharge electrical properties and the properties of the highly energetic ions that are necessary for plasma etching. More accurate sheath models are needed to better predict and optimize discharge electrical characteristics and ion kinetic energies. Sheath models are also used to develop new types of process monitoring techniques based on radio-frequency electrical measurements.

Our ongoing and planned efforts focus on measurement, data, and modeling challenges in the following specific areas:

1. We are currently developing a new optical diagnostic technique, sub-millimeter wave spectroscopy, to measure the density and temperature of important chemical species in plasmas. Work is progressing on validating the sensitivity limits of important plasma species and feed gas contaminants. In addition, spatially resolved absorption measurements will be made to map out the species and temperature distributions within the plasma and surrounding gas.

DELIVERABLES: Validate new applications of the sub-millimeter wave absorption spectroscopy as a plasma diagnostic. Validate sensitivity estimates of water vapor contamination in plasma feed gases. Develop method to separate absorption signal contributions from the plasma and the surrounding gas. 4Q 2003

2. Gas phase fluorocarbon radicals have been identified as species critical in the deposition of the fluorocarbon polymer layer that forms on wafer surfaces and provides selective etching of SiO_2 over Si during dielectric etch processes. The direct correlation between gas phase chemistry and surface composition of the polymer layer under a wide variety of plasma conditions has not been adequately measured. To gain a better understanding of the relationship between gas phase precursors and surface composition, we plan to couple our existing capabilities in gas phase measurements with surface measurements. We will utilize planar laser-induced fluorescence (PLIF) to determine 2-D density maps of fluorocarbon radicals in the gas phase. Wafer surfaces will be probed using IR absorption at several radial positions to determine how variations in gas phase chemistry affect the composition of the fluorocarbon polymer films.

DELIVERABLES: Develop diagnostic technique for surface measurements and correlate gas phase PLIF species density maps with spatial variations on surfaces. 4Q 2004

3. In order to continue the progress in shrinking semiconductor device dimensions, the ITRS Roadmap requires that lithographic techniques switch to shorter wavelength sources. Photoresist materials which are now commonly used do not work at these shorter wavelengths, so that entirely new materials based on very different chemistry are required. How the new photoresist materials will interact with etching plasmas is poorly understood at best. We will be applying a broad range of diagnostic capabilities (optical emission spectroscopy, sub-mm absorption spectroscopy, electrical diagnostics, ion mass spectrometry, ion energy analysis, microwave interferometry, and Langmuir probe techniques) to study plasma-surface interactions with new 157-nm photoresists. Initial work will focus on how etching of photoresist alters the etching plasma. Later work will examine polymer deposition and other means by which the plasma affects the photoresist surface.

DELIVERABLES: Characterize plasma – surface interactions of 157 nm photoresists with fluorocarbon etching plasmas. 4Q 2004

4. Electrical measurement techniques for use in process monitoring and control applications are also under development. These techniques rely on measurement of the radio-frequency current and voltage applied to plasma reactors. The rf measurements are compatible with commercial reactors and they contain valuable information about the flux and energy of the ions that bombard wafers during processing. Values for the total ion flux and ion energies are obtained by analyzing the current and voltage signals using electrical models of plasma sheaths. Tests to validate the models have largely been completed. Values for the total ion flux, sheath voltages, and ion energy distributions obtained from the rf measurements have been compared against independent measurements and shown to be in good agreement. Future development of these techniques is focused on improving the speed of the analysis algorithms to allow them to be used in real-time process monitoring and control applications, and subsequent demonstration of the ability of the technique to monitor and diagnose drift in ion flux and ion energies during plasma etching processes.

DELIVERABLES: Methods for monitoring total ion flux and ion energies using rf current and voltage measurements, with improved analysis speed to allow real-time process monitoring and control. 4Q 2003

DELIVERABLES: Demonstration and evaluation of rf-based ion flux and ion energy monitoring during plasma etch processes. 3Q 2004

Accomplishments

■ We have recently developed and tested a model-based technique for monitoring ion energy distributions that relies on rf current and voltage measurements made outside of a plasma reactor. The technique is designed for process monitoring applications in manufacturing where the use of invasive probes to measure ion energies is not practical. The method was validated by tests performed in argon and CF_4 discharges at 10-25 mTorr in an inductively-coupled, high-density plasma reactor, with rf bias applied to the substrate electrode at frequencies of 0.1-20 MHz. Plasma potential waveforms and sheath voltage waveforms obtained from the noninvasive rf technique agreed well with independent measurements made using a capacitive probe. Ion energy distributions from the rf technique were in good agreement with distributions measured by a mass spectrometer equipped with an ion

energy analyzer, at grounded as well as rf-biased electrode surfaces (see Fig. 2).

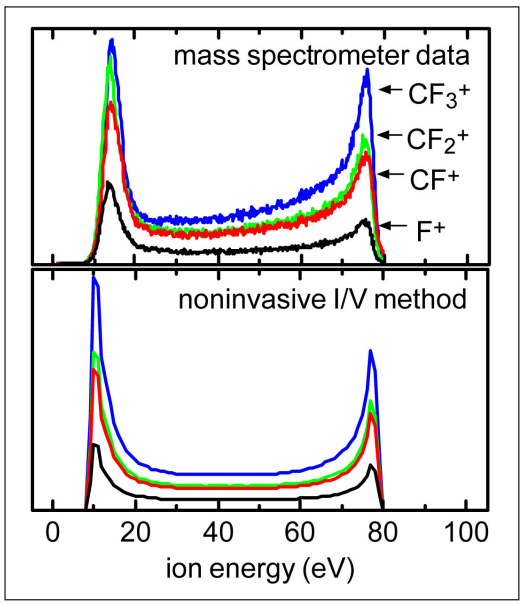


Figure 2. Ion energy distributions in a high-density CF_4 plasma: measured by a mass spectrometer/ion energy analyzer system (top) and obtained from non-invasive rf current and voltage measurements (bottom).

■ Sub-millimeter wave absorption spectroscopy is being developed as a plasma diagnostic to identify and monitor species in etching plasmas. Sub-mm wave spectroscopy can monitor the crucial chemical species in a plasma and provide the necessary feedback for understanding plasma processing (see Fig. 3). The density of radicals in capacitively coupled fluorocarbon etching plasmas have been measured for several different fluorocarbon etching gases in the presence of several different blanket coated silicon wafers. These measurements were correlated with etching rates and FTIR measurements of the downstream effluents. In situ measurements of water vapor contamination of the vacuum chamber and feedgases indicated a sensitivity limit for water on the order of 7.7×10^7 cm^{-3}. A detection sensitivity of 2×10^7 cm^{-3} was demonstrated for SiO, an etching byproduct of SiO_2 surfaces. The spectral resolution of the sub-mm diagnostic is so high that it can also be used to determine the translation temperature of the plasma species through the Doppler broadening of absorption line shapes. Gas temperatures are important input parameters to many plasma models since they are necessary to relate the measured gas pressure to the actual particle density in the chamber. Initial gas temperature measurements made from two different types of sub-mm sources, a backward wave oscillator (BWO) and an IR laser photomixer, were different. We have recently shown that this difference was caused by frequency jitter in the IR lasers. With improved frequency stabilization, gas temperatures measured with both sources are now in agreement.

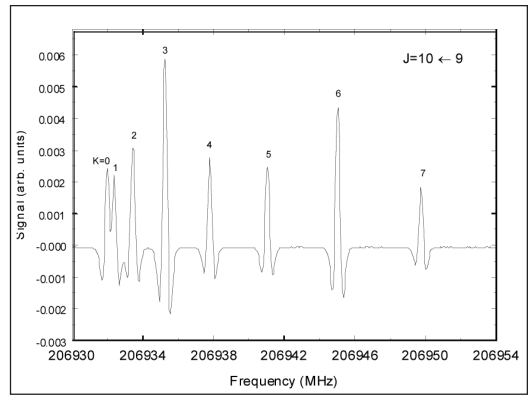


Figure 3. Sub-millimeter wave absorption spectrum of CHF_3 in a high-density, inductively coupled plasma.

■ Also this year, we have developed the capability to measure spatially-resolved 2-D temperature maps in fluorocarbon plasmas using planar laser-induced fluorescence (PLIF) of the CF radical. Several PLIF images are measured, each probing a different rotational level to give a 2-D map that is related to the CF population in the probed rotational state. With the relative population for several rotational levels known at each location, a rotational temperature map is calculated and assumed to be equivalent to the gas temperature under these conditions. We have measured temperature maps in CF_4 plasmas as a function of pressure and power, with and without silicon wafers present. Simultaneously, CF density images were obtained. Under our conditions, radial variations in temperature from 10 K to 90 K were observed. Axial temperature gradients were also observed to be quite large, especially under our highest pressure conditions (800 mTorr or 107 Pa) (see Fig. 4). The strongest temperature gradients were consistently found near the cooled electrode surfaces. These variations can have strong implications. Species density measurements that probe a specific rotational level can be misleading if the population of the chosen rotational level is not constant within the temperature range investigated. In addition, gas density in hotter regions will be lower, and this must not be interpreted as a chemical effect.

Especially near surfaces, where species density fluxes are often interpreted as indicating surface chemistry, one must be aware of the implications of these temperature effects. In addition, understanding temperature is important for modeling, since chemical reaction rates are often a function of temperature.

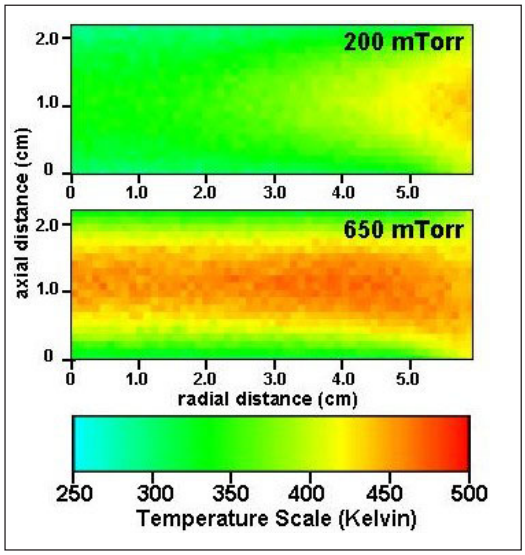


Figure 4. Temperature maps of a capacitively-coupled CF_4 plasma at 200 mTorr (26.7 Pa) and 650 mTorr (86.7 Pa).

■ Our capactively coupled plasma reactors have recently been modified to allow operation in dual-frequency mode. Dual-frequency reactors are becoming of increasing importance to the semiconductor industry, particularly in dielectric etching. New electrical measurement software has been developed to monitor the applied voltage and current waveforms, account for reactor stray impedance, and determine the true values of current, voltage and power drawn by these discharges. Unlike reactors that operate at a single frequency—where only the fundamental and a limited number of harmonic components are present—measurements of a dual frequency reactor need to monitor the fundamental and harmonics of both frequencies as well as the sum and difference frequencies. Time-resolved optical emission measurements of dual-frequency plasmas have also been performed. Together, the optical and electrical results provide a well-defined characterization of the dual-frequency plasmas, better understanding of their operation, and validation for models of their behavior.

■ Absolute, mass-resolved ion fluxes were measured in the presence of a silicon water in inductively coupled plasmas generated in a C_4F_6 processing gas. These measurements were made simultaneously with sub-mm absorption and optical emission measurements of the neutrals in the plasma. C_4F_6 is of interest as an alternative etching gas with low greenhouse gas emissions. The results provide insight into the complicated chemistry of C_4F_6 plasmas and are useful for validating and refining plasma simulation codes used by industry.

■ Fundamental data continue to be distributed to plasma modelers throughout industry and academia via the web-based NIST "Electron Interactions with Plasma Processing Gases" database (http://eeel.nist.gov/811/refdata/) (see Fig. 5). This web site has experienced tens of thousands of hits throughout its history.

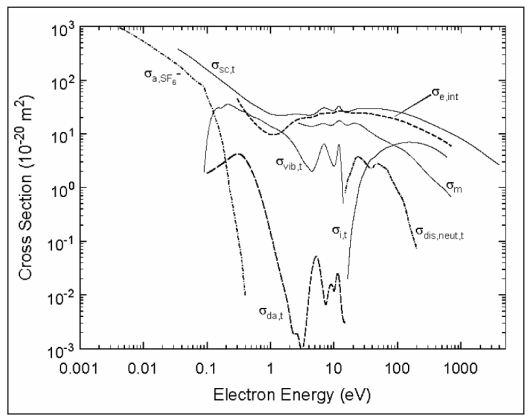


Figure 5. Recommended electron cross section data for SF_6 (shown here) and many other plasma processing gases are available at http://eeel.nist.gov/811/refdata/.

Recent Publications

K. L. Steffens and M. A. Sobolewski, "Effect of changing the electrode gap on the spatial and electrical properties of O_2/CF_4 plasmas," J. Vac. Sci. Technol. A **21**, 241 (2003).

M. Edamura and E. C. Benck, "Transition from E to H mode discharge in pulse-modulated inductively coupled plasmas," J. Vac. Sci. Technol. A **21**, 470 (2003).

M. A. Sobolewski, Y. Wang, and A. Goyette, "Measurements and modeling of ion energy distributions in high-density, radio-frequency biased CF_4 discharges," J. of Appl. Phys. **91**, 6303-6314 (2002).

M. A. Sobolewski, "Measuring the ion current in high-density plasmas using radio-frequency current and voltage measurements," J. Appl. Phys. **90**, 2660-2671 (2001).

K. L. Steffens and M. A. Sobolewski, "Investigation and control of spatial characteristics of chamber-cleaning plasmas," in AIP Conf. Proc. **550**, *Proceedings of the 2000 International Conference on Characterization and Metrology for ULSI Technology*, 233-237 (2001).

M. A. Sobolewski, "Monitoring ion current and ion energy during plasma processing using radio-frequency current and voltage measurements," in AIP Conf. Proc. **550**, *Proceedings of the 2000 International Conference on Characterization and Metrology for ULSI Technology*, 263-267 (2001).

E. C. Benck and K. Etamadi, "Fiber optic based optical tomography sensor for monitoring plasma uniformity," in AIP Conf. Proc. **550**, *Proceedings of the 2000 International Conference on Characterization and Metrology for ULSI Technology*, 268-272 (2001).

Measurements for Vacuum Process Control

Goals

Develop primary standards for gas flow in the range from 10^{-7} to 10^{-3} mol/s and transfer this flow measurement capability to the US semiconductor industry. (10^{-6} mol/s is 1.3 standard cubic centimeters per minute.)

Customer Needs

Many industrial processes require the accurate metering of mass flow rate over the range from 10^{-7} to 10^{-3} mol/s. Most prominent are the manufacturers of semiconductor devices, who use thermal mass flow controllers (MFCs) to control a wide variety of toxic, flammable, and corrosive gases. Participants at an industry workshop at NIST expected future requirements for flow measurement accuracies to be better than 1 %, and they identified the need for national flow transfer standards with uncertainties of 0.1 %. New primary flow standards and improved flow measurement techniques must be developed to meet these needs.

Measurement of gas flow is crucial for the control of the stoichiometry in plasma etching. The Critical Dimension reduction efforts discussed in the 2001 International Technology Roadmap for Semiconductors imply improvements in MFCs. "Improvements will be required in the etch chemistries…"; "…development of multi-step etch processes…may translate into the need to change gas chemistries in the same etch module…."

Technical Strategy

The flow measurements are based on a diverse series of primary standards. The first was a constant-volume (pressure rate-of-rise) primary standard that we developed to measure flows up to 10^{-3} mol/s with uncertainties of about 0.1 %. It has been replaced by a constant-pressure (variable volume) standard that can operate at pressures from 0.5 to 5 atmospheres with an uncertainty of about 0.05 %. The third primary standard is gravimetric; flow measurements made by a transfer standard are integrated and compared to the weight change of a gas bottle.

Transfer standards allow the primary flow standards at NIST to be compared to flow meters at other locations. Although a flow meter manufacturer typically constructs its own primary standard, comparisons with NIST allow the manufacturer to demonstrate proficiency and, if necessary, provide traceability to NIST. For this purpose, we have developed a series of very stable transfer standards based on laminar flow through a thermostatted duct. The first generation used a stainless steel, helical duct of rectangular cross-section. It was used to perform on-site proficiency tests of industrial flow standards at fabrication facilities and MFC manufacturers. The second generation transfer standard uses quartz capillaries with a circular cross-section, which are available commercially for gas chromatography (see Fig. 1). It has been used for comparisons with metrological institutes of other countries as well as manufacturers of flow meters. A third generation standard is under construction.

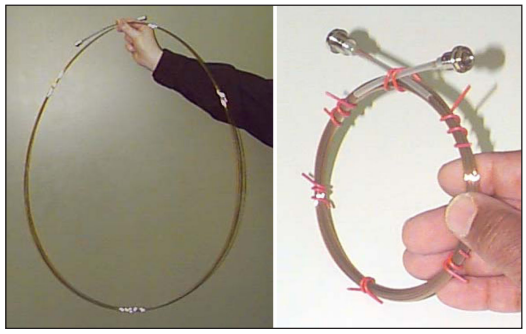


Figure 1. Left: A transfer standard flow impedance formed from 19 parallel quartz capillaries. Right: Tightly coiling the flow impedance tested the centrifugal corrections used in the transfer standard's hydrodynamic model.

DELIVERABLE: Develop and characterize primary standards for small gas flow. 2Q 2003

This flowmeter uses optical interferometry to measure and control the displacement of a piston of known cross-section. Controlling the piston's rate of displacement maintains a constant pressure in the gas accumulation volume.

DELIVERABLE: Develop and characterize an improved transfer standard for gas flow. 1Q 2003

The second-generation transfer standard is based on laminar flow through a quartz capillary impedance. It operates at higher flow rates with a smaller slip correction and much smaller centrifugal effects than the first-generation transfer.

Technical Contact:
Robert F. Berg
A. Lee

All in all we are very pleased and gratified NIST took the time to perform this comparison with us. We learned a great deal. Our technical personnel received some really good exposure to detailed analysis of flow comparisons and the amount of careful preparation required.

M. Bair,
DH Instruments

DELIVERABLE: Investigate new gas flow measurements systems. 4Q 2003

Accomplishments

- We directed flows of sulfur hexafluoride and propane through the second-generation transfer standard and into the constant-pressure primary flow standard. Both gases have a large density and a large deviation from ideal gas behavior. The results led to improvements in the hydrodynamic model of the transfer standard.

- We used the second-generation transfer standard to make comparisons of gas flow with two manufacturers of flow meters. Both companies used the comparison to evaluate new flow meter designs.

- We improved the characterization of the constant-pressure primary flow meter by modeling the effects of temperature lag and thermal expansion.

Recent Publications

R. F. Berg, "Two primary standards for low flows of gases", Proceedings of the Fifth International Symposium on Fluid Flow Measurement, Washington, DC (2002).

Test Metrology Program

Lead counts of several thousand per chip and test frequencies in the microwave regime challenge current test methodologies. The overall task is to develop test methodologies to address these new requirements.

Accurate at-speed test methodology of digital integrated circuits is a critical requirement. Traditional methods utilizing IC contact probing technology requires large contact pads incompatible with current IC designs. The development of alternative probing approaches through non-contact and intermittent probing techniques appear very promising. However, to implement these techniques, solving the at-speed test calibration issues is crucial. With the challenges facing designers and the rising costs of development, it is crucial to develop accurate testing strategies.

Metrology for System-on-a-Chip (SoC)

Technical Contacts:
A. R. Hefner, Jr.
M. Y. Afridi

"NIST Microhotplate may help search for extraterrestrial life."

Science Daily

"The NIST-developed microhotplate gas sensor technology is the future for homeland security and military applications of toxic gas and trace explosive detection."

Ernesto A. Corte,
Vice President,
Thermo Electron Corporation

Goals

Develop solutions to key metrology issues confronting the semiconductor System-on-a-Chip (SoC) industry. These include development of measurement methods and standards for characterizing non-digital Virtual Components (ND-VCs), a critical class of building blocks from which SoCs are developed. One focus is on delivering standards to facilitate the incorporation of multi-technology (MT) VCs including MEMS-based VCs into SoCs. The project activities include: multi-technology hardware description language (HDL) model development, VC interface standards, synthesis and scaling standards for ND-VCs compatible with digital methodologies, testing standards and verification standards. The NIST MEMS-based integrated gas-sensing VC will be used as a test bed to demonstrate the viability of these standards. In addition, the demonstration of general purpose gas-sensing VC methodologies will be used to facilitate the adoption these MT-VCs into new Homeland Security and Industrial applications.

Customer Needs

The driving force in today's semiconductor industry is the need to maintain a rate of improvement of 2x every two years in high-performance components. Historically, these improvements have relied exclusively on advances made in semiconductor miniaturization technology. The 1999 International Technology Roadmap for Semiconductors (ITRS) suggested that, "innovation in the techniques used in circuit and system design will be essential to maintain the historical trends in performance improvements." Achievement of this advancement in circuit and system design techniques is increasingly becoming dependent on integrating multiple technologies into a single chip referred to as System-on-a-Chip (SoC). The design challenges for SoC-MT devices will be overcome with the use of platform-based design approaches that emphasize design reuse, i.e. the development of ND-VCs that can be used as cost-effective building blocks for SoC-MT devices.

The challenges for SoC-MT devices are discussed in the 2001 International Technology Roadmap for Semiconductors in the Design, System Drivers and Test and Test Equipment sections.

Technical Strategy

1. The key to developing successful ND-VCs for SoC-MT devices it to make the ND-VCs, for all practical purposes, look like digital VCs. The first step in this multi-step process is to develop the ability to make the ND-VC devices via a CMOS compatible process. To demonstrate this capability we have chosen a MEMS microhotplate based VC, including operational amplifiers and decoders to process the data.

2. The second step in making the ND-VC look like a digital VC is to build a digital interface shell around the ND-VC. Since the ND-VC needs to interface to the digital circuitry of the system, this shell will add no additional cost to the system and having digital circuitry on as many of the interfaces as possible will greatly simplify the definition of the ND-VC's IO. To facilitate this approach we will develop methodologies and standards for adding digital shells to ND-VCs and demonstrate them on the gas sensor VC described above.

DELIVERABLES: Develop methodologies for designing digital interface shells for ND-VCs and demonstrate their viability via our micro hotplate gas sensor technology. 4Q 2003

3. The predominant design approach used by industry for SoC devices is top-down design. This requires that high-level HDL models exist for the VCs that are candidates for use in any particular system of interest. Compared to those for digital VCs, the methodology and standards for developing high-level models for ND-VCs is at best poorly developed. To address this need, high-level models are being developed for ND-VCs using Analog and Digital Hardware Description Languages, and methodologies are being developed to validate the models.

DELIVERABLES: Develop methodologies and standards for developing high-level models for ND-VCs and demonstrate their viability via our micro hotplate gas sensor technology. 4Q 2005

4. After the high-level simulation of the system in the top-down design process is successfully completed, the next step is to synthesize the individual VCs. Compared to those for digital VCs, the methodology and standards for ND-VC synthesis is at best poorly developed. To address the need for synthesizing ND-VCs, we are

developing standards and metrologies for a non-digital synthesis like process that is compatible with digital synthesis. This process is based upon libraries of existing designs and the device design equations.

DELIVERABLES: Develop methodologies for an equivalent MT-VC synthesis approach and demonstrate its viability via our microhotplate gas sensor technology. 2Q 2006

5. Scaling digital circuitry is a key capability used by digital designers to reduce the costs of their designs. Since most systems that would use ND-VCs will be predominately digital, it is important that there be an equivalent scaling capability for the ND-VCs. To address the need for scaling ND-VCs, we are developing metrologies for non-digital scaling processes.

DELIVERABLES: Develop methodologies and standards for an equivalent ND-VC scaling approach and demonstrate its viability via our micro hotplate gas sensor technology. 3Q 2004

6. The testability of ND-VCs represents another significant challenge since standards and methodologies for non-digital circuits do not exist. The most promising approach to address testability is to use Built-In-Self-Test (BIST) techniques. To facilitate this approach we will develop methodologies and standards for adding BIST to ND-VCs and interface them via the digital shell.

DELIVERABLES: Develop methodologies for built-in self test of of ND-VC devices and demonstrate their viability via our micro hotplate gas sensor technology. 4Q 2004

Accomplishments

■ A monolithic micro-gas-sensor system was designed and fabricated in a standard CMOS process (Fig. 1). The gas-sensor system incorporated an array of four micro hotplate-based gas-sensing structures. The system utilized a thin film of tin oxide (SnO_2) as a sensing material. The interface circuitry on the chip has digital decoders to select each element of the sensing array and an operational amplifier to monitor the change in conductance of the film. The chip is post-processed to create micro hotplates using bulk micro-machining techniques. Detection of gas concentrations in the 100 parts-per-billion range was achieved. This represents a factor of 100 improvement in sensitivity compared to existing MEMS-based micro-hotplate gas sensors.

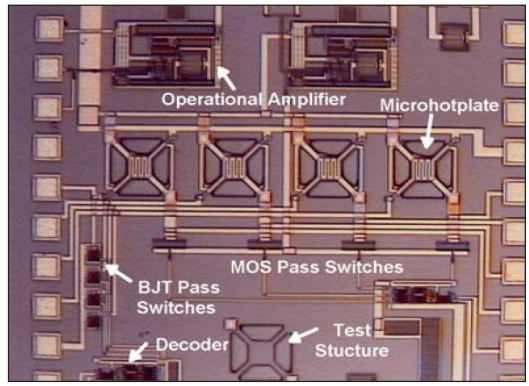


Figure 1. Micrograph of gas-sensor system to be used as demonstration vehicle.

■ A monolithic CMOS four element gas sensor VC is designed and submitted for fabrication. The design includes both analog and digital integrated circuits. The digital part of the circuit has an 8-bit analog-to-digital converter (ADC). The objective of the design is to make it compatible with the SoC design methodology (Fig. 2).

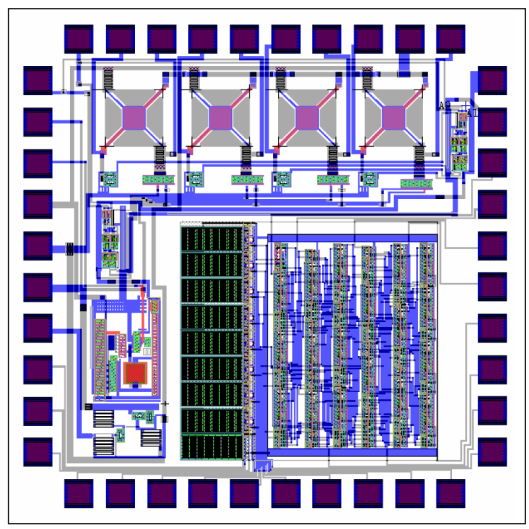


Figure 2. Layout of the four element gas sensor VC with analog-to-digital control.

Recent Publications

Afridi, M. Y., Suehle, J. S., Zaghloul, M. E., Berning, D. W., Hefner, A. R. Hefner, Semancik, S., Cavicchi, R. E., "A Monolithic Implementation of Interface Circuitry for CMOS Compatible Gas-Sensor System," ISCAS-2002

Afridi, M. Y.; Suehle, J. S.; Zaghloul, M. E.; Berning, D. W.; Hefner, A. R.; Cavicchi, R. E.; Semancik, S.; Montgomery, C. B.; Taylor, C. J., "A monolithic CMOS microhotplate-based gas sensor system," IEEE SENSORS JOURNAL, VOL. 2, NO. 6, pp. 644- 655, DECEMBER 2002.

Nonlinear Device Characterization

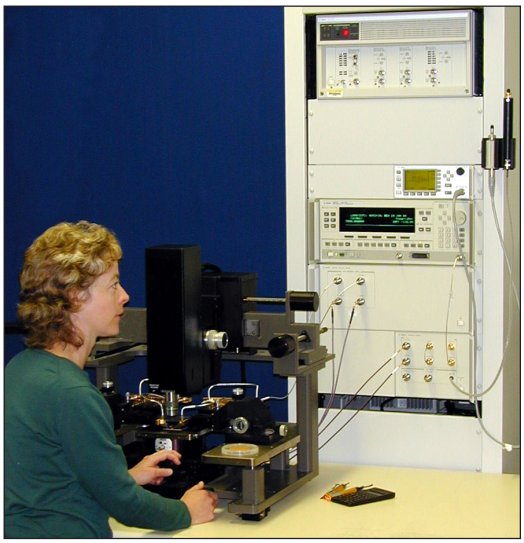
Technical Contact:
Don DeGroot

"Agilent Lightwave Division would like to encourage NIST's continued work to develop the nose-to-nose characterization, so that the technology can become more widely available."

Dennis Derickson, Agilent technologies, Inc.

Goals

Develop and support general methods of characterizing nonlinear components, circuits, and systems used in digital wireless communications; refine and transfer these methods through interactions with industrial research and development laboratories.



Dr. Kate Remley performs large-signal measurements of an RF power amplifier using the Nonlinear Network Measurement System.

Customer Needs

Radio-frequency measurements are applied extensively in the deployment of commercial wireless communication systems. They are crucial to all stages of system development, from device modeling to circuit design and system performance characterization. NIST's RF and microwave measurement teams are addressing the critical need for accurate measurements of nonlinear electrical networks and supporting industrial standards development.

Technical Strategy

The Nonlinear Device Characterization (NDC) Project is developing and verifying measurement-based descriptions of devices, circuits, and systems that contain nonlinear elements. The RF power amplifier is a key nonlinear component with which engineers are currently contending. Industrial experts estimate that the RF power amplifiers account for 60-70 % of base station costs and 20-30 % of the total wireless link cost. Traditional microwave circuit design has relied on the ability to cascade circuit elements through simple linear operations and transformations, but engineers lose the ability to predict circuit performance across operating environments, or states, when their circuits include a nonlinear element. Presently, there is a critical need for fundamental RF measurement techniques to develop and validate nonlinear models and commonly applied figures of merit. Contributions in this area will significantly improve design-cycle efficiency and trade between manufacturers, and will eventually facilitate improvements in communications through the full incorporation of nonlinear models at the system design level.

The NDC Project recently acquired and established a new measurement facility known as the Nonlinear Network Measurement System (NNMS). The system provides the most general approach to measuring large-signal responses. It is a stimulus-response network analyzer that supplies periodic signals, and then acquires broadband incident and reflection waveforms at the device under test. The NIST facility will be used as a reference system in measurement and model comparisons. The project team is developing accurate calibration and measurement techniques for the NNMS, including validation of the Nose-to-Nose calibration technique, a practical and available method of measuring the phase relations of components in signals with 50 GHz bandwidths. The project team is now refining the statement of measurement uncertainty in the Nose-to-Nose method and will apply it to NNMS measurements.

The Nonlinear Network Measurement System is being applied first to canonical circuits to compare general measurements with predictions made by circuit simulators and new behavioral models. We have applied these techniques to identify stable verification circuits that will be used in NIST-sponsored interlaboratory comparisons. Second, the measurement system is being applied to develop and verify artificial neural network (ANN) models for nonlinear circuits being developed in cooperation with the University of Colorado. NNMS data will be used to train ANN models, to verify circuit operation and model predictions, and to validate a circuit optimization approach.

The NDC Project has also started to examine the link between nonlinear circuit descriptions and

system performance simulations. Through collaborations with NIST's broadband standards development effort, members of the NDC Project will assemble a measurement system to test the performance of communication links.

Plans are underway with the University of Colorado to establish a Joint Research Center for Nonlinear Electronics in Wireless at Radio Frequencies (newRF). This Center, funded by industrial members, will support graduate research projects. The graduate research assistants and CU faculty will work with NIST staff on the newRF projects. The Center will increase the effectiveness of the NIST facilities while developing a new class of technical professionals who have the skills required by industry.

Accomplishments

- Defined consistent method for defining the phase relation of signal components that are not at the same frequency.

- Expanded and clarified definition of large-signal scattering parameters, demonstration application to nonlinear rf circuit design.

- Expanded numerical simulations of the Nose-to-Nose calibrations as the basis for an uncertainty statement on the NNMS phase alignment. There are no other methods of identifying the error terms due to the internal sampling electronics used by the Nose-to-Nose equipment. The simulator-based sensitivity study gives us the basis for a first-level uncertainty bound.

- Adapted Multiline TRL Calibration for NNMS and included in commercial software, with Agilent collaborators. All users of current and future NNMS-like instruments will have access to this NIST reference calibration in their daily measurements.

- Added modulated signal capabilities to the NIST NNMS. Demonstrated modulated signal measurements on example RF amplifier. Conducted multiple modulation calibrations to study instrument repeatability. NIST can now use the NNMS to characterize circuits using two-tone and multi-tone signals, and then compare these to commonly used figures of merit.

- Designed interlaboratory measurement comparison for nonlinear network analyzer users. Designed and fabricated prototype verification circuits. Formulated initial comparison method and measures. Performed initial comparisons between NIST and Belgian research labs. Users of NNMS and related nonlinear network analyzers will gain assurance in their ability to identify nonlinear input-output transfer functions or extract model parameters.

- Developed nonlinear models for verification devices. Developed and applied conventional compact diode models. Developed frequency-domain behavioral modeling strategy with the University of Colorado. Developed time-domain behavioral model with guest researcher from K. U. Leuven, Belgium. The interlaboratory comparison of nonlinear network analyzers requires models since we do not have a generalized nonlinear parameter to compare. The models can accurately represent the nonlinear transfer functions of the verification circuits over the state-space that they are characterized, allowing participants to find the differences between their measurements and our model predictions.

- Developed first-generation metrics for comparing data from nonlinear circuit characterizations. These tools can easily summarize the differences found in multi-dimensional data sets common to nonlinear network analysis. The metrics will be used immediately in the NIST-sponsored measurement comparison.

- Developed generalized approach to measurement-based frequency-domain models of nonlinear circuits. Demonstrated ANN models to define and obtain large-signal scattering functions. This approach is proving useful in improving the efficiency of nonlinear circuit design and optimization. It is currently the only definition of large-signal scattering functions that does not assume some level of linearization.

- Concluded second phase of a Passive Intermodulation measurement comparison. Participants determined how well their measurements compared to ensemble averages for characterizations of a verification device with ultra-low passive intermodulation response.

- In collaboration with Professor K. C. Gupta of the University of Colorado at Boulder, applied artificial neural networks (ANNs) to improve the modeling of on-wafer open-short-load-thru (OSLT) standards and coaxial line-reflect-match (LRM) calibrations used for calibrating vector network analyzers. The new methods will be used in *Time-domain Network Analyzer (DNACal)* and new NNMS software.

■ Discovered nonlinear error mechanism in the Nose-to Nose calibration. Through an innovative combination of large-signal and small-signal analyses, showed how nonlinear junction capacitance in the sampler circuit induces an error that had been ignored in the initial Nose-to-Nose analysis.

■ Initiated NIST's Nonlinear Network Measurement System (NNMS) and conducted NIST's first large-signal nonlinear device verification experiments. Agilent Technologies delivered the NNMS instrument in fulfillment of a custom equipment contract and extensive collaborative research effort with NIST.

Collaborations

Vrije Universiteit Brussel, Department ELEC. To develop stochastic calibrations for accurate radio-frequency circuit and device measurements.

University of Colorado, Electrical and Computer Engineering Department. To develop new measurement-based behavioral models of nonlinear RF circuits and devices.

NIST ITL Statistical Engineering Division and EEEL Electromagnetic Technology Division. To develop standard nonlinearity, then use it to verify NNMS calibrations and modeling approaches; to extend nonlinear circuit models to system characterization.

K.U. Leuven, Belgium. To develop models for measurement comparison verification devices, and to study instrument repeatability.

Recent Publications

D. C. DeGroot, J. A. Jargon, and R. B. Marks, "Multiline TRL revealed," *60th ARFTG Conf. Dig.*, pp. 131-155, Dec. 2002.

J. A. Jargon, D. C. DeGroot, K. C. Gupta, and A. Cidronali, "Calculating ratios of harmonically related, complex signals with application to nonlinear large-signal scattering parameters," *60th ARFTG Conf. Dig.*, pp. 113-122, Dec. 2002.

J. A. Jargon, K. C. Gupta, and D. C. DeGroot, "Applications of artificial neural networks to RF and microwave measurements," *Int. J. RF Microwave Computer-Aided Eng.*, vol. 12, no. 1, pp. 3-24, Jan. 2002.

J. A. Jargon, K. C. Gupta, D. Schreurs, and D. C. DeGroot, "Developing frequency-domain models for nonlinear circuits based on large-signal measurements," *Proc. XXVIIth Gen. Assembly Int. Union Radio Sci.*, CD-ROM A1.O.6, Aug. 2002.

A. B. Kos, T. J. Silva, P. Kabos, M. R. Pufall, D. C. DeGroot, L. Webb, and M. Even, "Design and performance of an inductive current probe for integration into the trace suspension assembly," *IEEE Trans. Mag.*, vol. 38, no. 1, pp. 50-54, Jan. 2002.

K. A. Remley, J. A. Jargon, D. Schreurs, D. C. DeGroot, and K. C. Gupta, "Repeat measurements and metrics for nonlinear model development," *2002 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 2169-2172, June 2002.

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At-Speed Test of Digital Integrated Circuits

Technical Contacts:
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J. Moreland
P. Kabos
J. Kopanski

"As electronic devices shrink into the nanometer size scales and integrated circuits operate at multi-GHz clock rates, probing their internal characteristics is becoming both more critical and far more difficult than ever before."

Travis M. Eiles, Ph.D.
Intel Corp.

Goals

Develop and demonstrate metrology for the at-speed test of digital integrated circuits. The program will resolve the essential metrology issues of at-speed digital integrated circuit test. It will apply its results to characterizing and calibrating high-impedance probes, develop atomic force microscopes (AFMs) capable of precisely positioning field probes above the surface of the integrated circuit, and push the current on-chip sampling technologies now being explored by the industry.

Customer Needs

The semiconductor industry needs accurate metrology for the at-speed test of digital integrated circuits ("Grand Challenges," page 11, 1997 National Technology Roadmap for Semiconductors). Traditional IC contact probing technology requires large contact pads incompatible with the operation and economic constraints of modern IC designs. Alternative probing approaches use high-impedance probes, non-contact probes, atomic-force microscopes, electron beams, optical beams, or on-chip samplers that respond to either electric or magnetic fields near transmission lines in the circuits. However, while the uncalibrated field measurements performed by these probing systems are suitable for field mapping, they are a far cry from the precise measurements of voltages and currents required for electrical design.

Solving the critical at-speed test calibration issues will add enormous value to the probing systems currently being used or developed for high-performance digital integrated circuits. Developing characterization and calibration methods for high-impedance probes, whether of the conventional type or mounted on atomic-force microscopes, will help speed the development and implementation of these new measurement tools, and so create a new paradigm for the at-speed test of high-speed digital integrated circuits.

The need for noninvasive waveform measurements in silicon integrated circuits is discussed in the Test and Test Equipment section, pages 1-5, 2001 (International Technology Roadmap for Semiconductors).

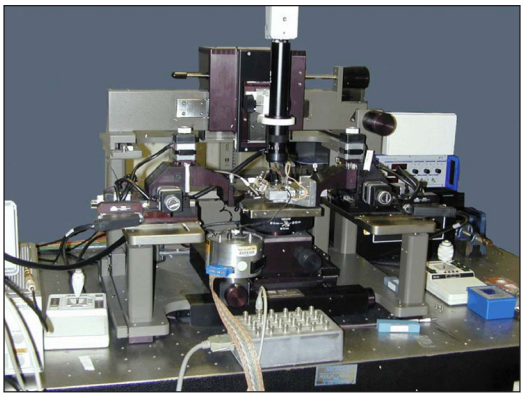

Figure 1. Universal test bed for electric and magnetic field probing on a nanoscale.

Technical Strategy

We will develop calibration artifacts with precisely known high-frequency voltages and circuits suitable for characterizing and calibrating high-impedance probes and samplers of all types. We will focus on fundamental calibration issues: transforming the response of the probes to the electric and magnetic fields above the integrated circuit into accurate voltages and currents inside the circuit.

We will first apply the characterization and calibration procedures to conventional high-impedance probes. To facilitate the development and test of electric and magnetic probes with nanoscale resolution, we are constructing a universal AFM test bed for these probes (see Fig. 1). We will then apply our characterization procedures to miniature AFM probes suspended on custom cantilevers designed for high frequency measurements on the nanoscale. Finally, we will tie our metrology back to fully-characterized electro-optic sampling measurements.

DELIVERABLES: Develop complete electrical characterization for commercial high-impedance probe, including transfer function, invasiveness, and noise immunity. 3Q 2003

DELIVERABLES: Build universal AFM test bed. 3Q 2003

DELIVERABLES: Electrically characterize and AFM probe. 2Q 2004

Accomplishments

- We have designed and tested a prototype sinusoidal waveform standard.

- We have constructed a high-speed electro-optic sampling system.

- We have developed, fabricated and tested a noninvasive AFM scanning probe for measuring local microwave power (see Fig. 2 at right).

- We have developed a method of characterizing and calibrating conventional high-impedance probes for low-invasive waveform measurements (see Fig. 3 at right).

- We have applied our high-impedance-probe characterization method to a probe mounted on an atomic-force microscope.

Recent Publications

P. Kabos, H.C. Reader, U. Arz, and D.F. Williams, "Calibrated waveform measurement with high-impedance probes," IEEE Trans. Microwave Theory and Tech., February 2003.

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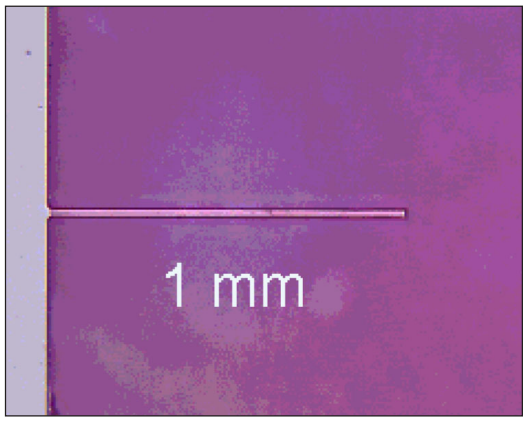

Figure 2. A 1 mm long dielectric bimaterial cantilever AFM probe fabricated at NIST for noninvasively measuring local microwave power.

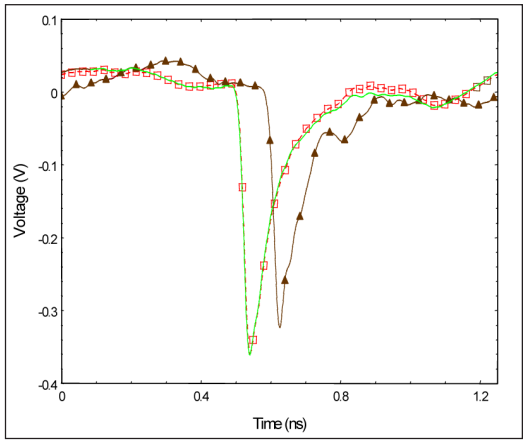

Figure 3. Waveform comparison at the tip of a commercial high-impedance probe. The red curve marked with red squares is the expected waveform. The brown curve marked with triangles is the measured waveform. The green curve is the measured waveform after correction by the new NIST algorithm.

Jitter and Propagation Delay Measurement

Technical Contacts:
N. G. Paulter
D. R. Larson
D. I. Bergman

"Accurate characterization of the jitter on a signal, as well as a system's ability to tolerate jitter are critical… for the designer and manufacturer of communication systems and components."

Brian Scott,
Agilent Technologies

Goals

To develop methods for accurately measuring timing jitter in high bit rate (> 10 GB/s) telecommunication systems and develop systems and protocols for measuring and computing propagation delay through active circuits. This includes the development of artifact standards, data extraction and analysis procedures and algorithms, and measurement systems, each where necessary. Existing measurement methods will be examined to determine consistency amongst them, measurement limitations, and range of applicability. Measurement services will be developed for the measurement of different types of jitter and for propagation delay.

Customer Needs

Jitter is a limiting factor in the performance of high-frequency/high-speed telecommunications and computer systems. A typical eye diagram measurement is shown in Fig. 1. In a telecommunications system, where a series of clock-recovery circuits is typically used, jitter degrades data recovery performance. Jitter measurements on telecommunications components and equipment are needed to assure compatibility between manufacturers and to identify sources of jitter. For microprocessor chips, the jitter in the on-chip phase-lock-loop circuit is used by the manufacturer to sort the microprocessor for clock speed usage. Large errors in the measurement of clock jitter represent manufacturing yield loss. Furthermore, for some high-speed computers, the frequency of the microprocessor clock is a multiple of the system clock frequency, and jitter degrades the timing tolerance of the circuit. The data storage industry is also concerned with jitter in recovery of data from the source media.

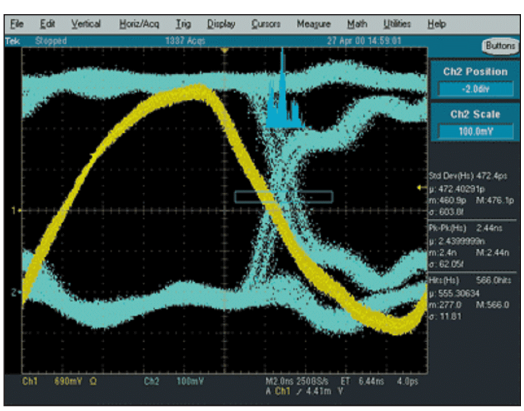

Figure 1. Eye diagram for jitter measurements.

The calibration of jitter measurement equipment to an uncertainty of a few picoseconds is a difficult problem. Several types of jitter measurements that are important are: transition-to-transition jitter, jitter relative to a fixed clock, jitter spectrum, and data dependent jitter. These measurements are important for determining the source of jitter and component compatibility. To test components accurately, jitter generation is important. Industry has reported to NIST that they get inconsistent results from jitter measurements using different techniques and would welcome a neutral party to evaluate the limits of the many measurement methods.

The importance of jitter measurement capability is described in the 2001 International Technology Roadmap for Semiconductors on several pages. In particular, on page 11, it states, "The jitter generated by the transmitter is the key parameter to guarantee transmitter quality. Currently, jitter measurement capability on ATE is in its infancy – there is no instrument available that simultaneously satisfies the noise floor, analog bandwidth, and test time requirements for high performance interfaces."

Propagation Delay – Propagation delay in active circuits is defined as the difference between the occurrence of some event on an output signal relative to that of the input signal. The measurement of this type of delay is not straightforward because the characteristics of the input signal affect both the characteristics of the output signal and the time the output signal exits the circuit. Automated test equipment (ATE) from different manufacturers produce different input signals, and this results in different delays for a given circuit. Furthermore, the ATE results may not emulate actual delays because the ATE signal and/or electrical environment may not represent accurately what is expected by the circuit.

The ability to reproducibly measure propagation delay is an issue. This will require interaction with industry to develop an accepted reference signal and, perhaps, impedance environment. Furthermore, accurate (picosecond) delay measurements will require traceability over the delay ranges (several microseconds) required by industry. Measurement protocols will also have to be established.

Technical Strategy

To develop a precision differential delay system that will be used to measure jitter and propagation delay in electronic circuits and systems. The hardware for providing differential delays to 1 μsec will be designed and developed, and the temperature sensitivity and repeatability of the differential delay settings will be measured. In addition, methods for accurately (uncertainties ± 1 ps) calibrating the discrete differential delays will be developed. A continuously variable differential delay from 0 ns to 1 ns and methods for accurately calibrating the delay transfer function and its temperature sensitivity will also be developed.

DELIVERABLES: Design and build the medium differential delay (1 ns to 16 ns) subsystem. 3Q 2003

DELIVERABLES: Design and build the coarse differential delay (> 10 ns) and fine differential delay (< 2 ns) subsystems. 4Q 2003

DELIVERABLES: Design calibration methods for and calibrate the precision differential delay system. 2Q 2004

Accomplishments

- New project.

Failure Analysis of Integrated Circuits

Project Leader:
David Pappas

Goals

This project is developing magnetoresistive arrays and readout electronics that can image magnetic fields from data storage media and current distributions in integrated circuits. These are targeted to failure analysis of integrated circuits.

Customer Needs

Failure analysis to identify field problems as well as to diagnose design errors in the development phase of integrated circuit production have always been critically important for success. Rapidly escalating circuit complexity has placed ever-increasing demands on failure analysis techniques.

The 2001 International Technology Roadmap for Semiconductors explicitly states the need for defect analysis and failure analysis in Table 19, page 117 in the section titled Test and Test Equipment. On page 327 in the section on Assembly and Packaging is the statement, "Conception and development of tools for rapid electrical and physical fault isolation of package and interconnect technologies is critical."

Technical Strategy

The Magnetic Technology Division has been developing metrology for magnetic data storage since 1996. This program has resulted in advanced measurement techniques for imaging information stored on magnetic media with high resolution and relative ease. The nanoscale recording system **(NRS)** developed under this program is a general-purpose instrument that uses read/write heads similar to those in computer hard-disk or tape drives to read and write data on magnetic media. The NRS can image by rastering either the head, using computer-controlled micrometers with 50 nanometer resolution, or the storage medium, using a piezoelectric *x-y* stage with 1 nanometer resolution. The NRS is being used as a prototype for forensic analysis of audio tapes. We have been able to perform high-speed imaging of tape samples, identify the signatures of erase and write heads, and reconstruct analog and digital data.

The NRS is also capable of magnetic field imaging for non-destructive analysis of integrated circuits and materials. Failure analysis of very-large-scale-integration **(VLSI)** chips at the die level and after packaging is critical to identifying short circuits due to defects and design flaws. Inversion of the magnetic fields above these devices can provide high-resolution images of the current distributions noninvasively. In addition, hidden corrosion and cracks in materials can be imaged using induced eddy-current magnetic-field mapping. We have developed both single-element and multiple-element magnetoresistive probes on a scanning system to measure these fields. The inversion can isolate currents and defects with very high accuracy. We have developed 64- and 256-element linear arrays of multiplexed sensors. The system has been applied to failures in flip-chip high-density processors, random-access memory chips, and failure analysis of fastener materials.

DELIVERABLES: Design, fabricate and test a linear, eight-element anisotropic-magnetoresistance (AMR) "comb" array and controller. Extend the comb array to 64 elements and compare it to on-chip arrays. 3Q 2003

Develop 50 ohm single magnetoresistive probes and characterize their frequency response. Test linear arrays with both in-plane and perpendicular transforms. 3Q 2003

Accomplishments

Applications in Integrated Circuit Failure Analysis — Using a scanning magnetic field microscope,[1] we have analyzed the magnetic fields from defective integrated circuits (Fig. 1).

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[1] We worked with the Federal Bureau of Investigation to upgrade its scanning magnetic field microscope with magnetoresistive sensors. The microscope is used for forensic authenticity analysis of magnetic storage tape evidence, for example, audio cassette and videotapes. The system originally used a VHS inductive tape head sensor coupled to a SQUID magnetometer. The new sensors have higher resolution and incorporate a second-harmonic modulation and sense scheme that rejects thermal anomalies. This allows the sensor to slide in contact with the sample, giving the maximum possible resolution. At present, the resolution allows for 2 micrometer wide tracks with 0.02 micrometer downtrack resolution. Other enhancements to the system were vibration isolation and an electronic triggering method to more closely map the actual position of the head over the media.

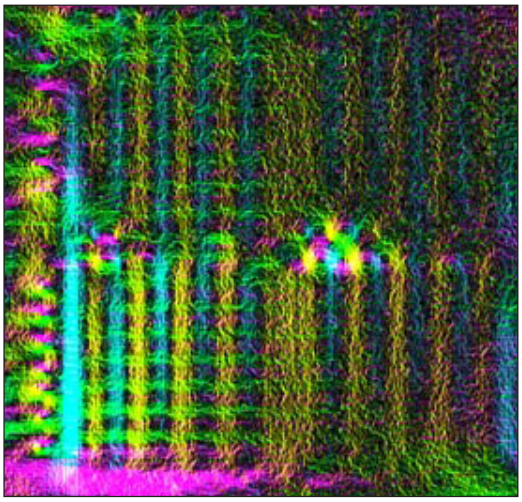


Figure 1. Failure-analysis image of currents in a flip-chip random-access memory. The image is 2.5 centimeters by 2.5 centimeters and shows the currents in the chip as calculated by inverting the z component of the magnetic field using Maxwell's equations.

This application will be focused on helping industry screen production devices for anomalous current drain, thereby increasing enhancing their failure analysis methods.

Recent Publications

"Localization of currents in integrated circuits", A. V. Nazarov, F. D. DaSilva, D. P. Pappas, submitted, Journal of Applied Physics.

Second Harmonic Magneto-Resistive Imaging to Authenticate and Recover Data from Magnetic Storage Media, D. P. Pappas, C. S. Arnold, G. Shalev, C. Eunice, D. Stevenson, S. Voran, M. E. Read, E. M. Gormley, J. Cash, K. Marr, J. J. Ryan, Proceedings of SPIE Conference on Technologies for Law Enforcement, Boston, MA, in press, Nov. 2000.

Manufacturing Support

Cross-cutting all manufacturing disciplines is the need for supporting information technology and processing capabilities. The transition to 300 mm fabs, single-wafer lots, and the extensive use of foundries has made efficient information handling and automation indispensable to the production process. Information technology touches nearly every aspect of semiconductor production and distribution, including process control, tool to tool interconnect, automated material handling and tracking, reticle management, and information interchange across the supply chain. NIST is working with International SEMATECH to provide and maintain an on-line engineering statistical handbook to support process control, and is working with industry on standards required to support information flow across the "engineering chain."

NIST/SEMATECH e-Handbook of Statistical Methods

Goals

The goal of the NIST/SEMATECH e-Handbook of Statistical Methods project is to produce an online resource to help scientists and engineers incorporate statistical methods into their work more efficiently. An online publication and a practical, example-driven format were chosen to make the e-Handbook readily accessible to its target audiences in industry, including the semiconductor manufacturing industry in particular.

Customer Needs

Semiconductor manufacturing requires extraordinary discipline in process control. For example, a typical integrated circuit manufacturing process involves several hundred steps. These steps may include as many as thirty lithographic levels, which require extremely precise alignment with respect to one another. Tight process control is essential to produce a functional circuit. SEMATECH has recognized the importance of statistical process control in semiconductor manufacturing and has developed and maintained expertise in this field since its inception in 1988. Two of the more difficult issues impeding routine implementation of these techniques, however, include educating the users and making the tools easy to use.

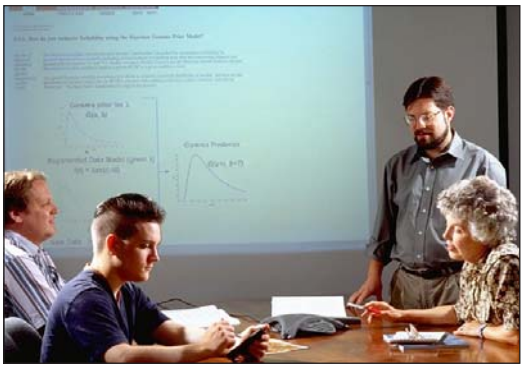
Technical Strategy

NIST and SEMATECH formed a collaboration under the umbrella Cooperative Research and Development Agreement (CRADA), combining the general expertise in engineering statistics at NIST with the semiconductor manufacturing expertise resident at SEMATECH.

DELIVERABLES: Develop and release a version of the e-Handbook on CD for off-line use by customers. 2Q 2003

Accomplishments

- Since release of the final version, work has focused on publicizing the e-Handbook, responding to user feedback, and developing a CD version for off-line use. In the last year, publicity on the e-Handbook has appeared in *Science*, *Quality Digest*, *MicroMagazine.com*, *States News Service*, *National Science Digital Library Report for Math, Engineering, and Technology*, and *American Statistician*.



NIST e-Handbook of Statistical Methods team (left to right, Alan Heckert, Mark Reeder, Will Guthrie, and Carroll Croarkin) reviewing a page from the chapter on product reliability.

Collaborations

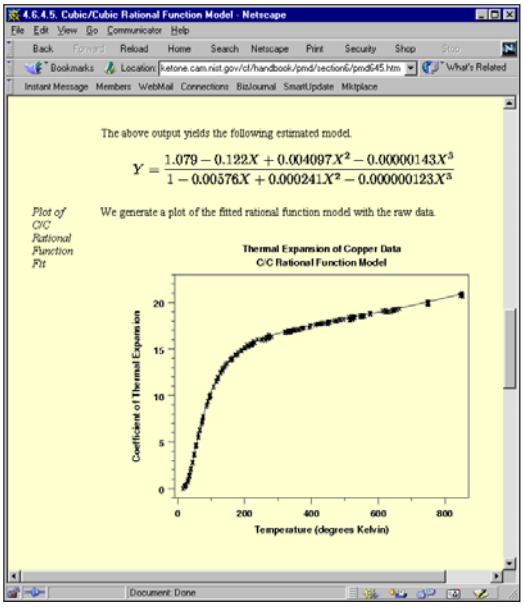
International SEMATECH, Paul Tobias, Jack Prins, Chelli Zey; project planning, organization, writing and editing.

AMD, Barry Hembree; project planning, organization, and writing.

Motorola, Pat Spagon; project planning, organization, and writing.

Recent Publications

NIST/SEMATECH e-Handbook of Statistical Methods, M. Carroll Croarkin and Paul Tobias, editors, http://www.nist.gov/stat.handbook/.



Page from a case study in the process modeling chapter of the Handbook.

Technical Contacts:
W.F. Guthrie
A. Heckert
J.J. Filliben

"I am thoroughly enjoying your Engineering Statistics Handbook. Thanks so much for adding real value to the information available on the Internet!!!"

Paul Zaremba,
Systems Engineer,
Agilent Technologies

Engineering Chain Management in the Semiconductor Industry

Technical Contacts:
B. Goldstein
Y. Li

Goals

This project will investigate and document key issues related to electronic data exchange, supply chain communication, and other automation standardization needs confronting the semiconductor industry. The objective of this project is to facilitate the evolution of an integrated semiconductor "Engineering Chain" which provides each partner with the data needed to make business decisions in a timely manner.

Customer Needs

Increasing technological requirements has led the semiconductor industry to seek further means of cost savings by improving factory productivity, streamlining business models, and accelerating their supply chain. The growing complexity of product development and manufacturing models in parallel with shrinking product lifecycles further exacerbates the challenges the industry faces. Maximizing interoperability among automation systems in the factory and throughout the supply chain will become a greater issue for realizing the semiconductor industry's hopes to reduce time, inventory, and therefore costs.

Integration of FICS [Factory Information Control System] applications with business-level software systems provides accurate factory floor data for supply management, and improved product tracking. Potential solutions will require the standardization of technologies that enable this level of integration. 2001 International Technology Roadmap for Semiconductors, Factory Integration (ITRS), p. 17.

The transition to 300 mm fabs and single-wafer lots has challenged the semiconductor industry in nearly every aspect of production, such as: facility layout; the mix of R&D within a single fab; data analysis of small lots; tool to tool interconnect; automated material handling and tracking of product, non-product wafers and reticles; the division of the production process across a partnership of foundries, designers, production sites, distributors and equipment manufacturers. Chip manufacturers require greater visibility of end product demand to accurately schedule their factories, and require greater technical collaboration with designers, OEMs, and foundries to ensure the manufacturability of the product being designed today using the generation of equipment that will be installed once production starts.

Cost of design is the greatest threat to continuation of the semiconductor roadmap. 2001 ITRS, Design, p. 1.

According to the 2001 ITRS, design complexity has been growing exponentially due to the increasing density and number of transistors to meet performance goals. Intellectual Property (IP) reuse helps companies get complex systems to market quickly by eliminating redundant design effort. Standard formats for IP specifications and tool interfaces for the design of a System-on-a-Chip (SoC) would reduce time to market by eliminating the need for translations. Security mechanisms must also be incorporated to protect IP during transfers.

Other information-exchange gaps in design houses include standard data formats for timing and power to expedite timing closure, reduce design iterations, and promote interoperability among best-of-breed software tools.

The industry trend towards outsourcing is leading towards silos of expertise, exactly when technology advances require a multi-disciplinary approach to problem solving. The production process is being conducted across fabs – not only at the traditional point of packaging and test, but mid-stream in the IC fabrication process. As the wafers change hands, so must the information about that wafer which accumulated during its production life cycle.

Technical Strategy

To help the industry achieve their goal of effective partnerships within an Engineering Chain, this project will engage in industry efforts that would benefit from NIST's neutrality, multi-industry expertise, and broad and detailed knowledge of the Information Technology (IT) standards development process.

DELIVERABLES: Contribute to the 2003 Factory Integration component of the ITRS by co-leading the Engineering Chain Management subteam. 4Q 2003

Attendance at workshops, conferences, and standards meetings held by key organizations in

the semiconductor community such as International SEMATECH (ISMT), Semicon-ductor Equipment Materials International (SEMI) and RosettaNet provides opportunities to assess current areas of IT standards development. As the industry moves towards utilization of mainstream computing technologies including eXtensible Markup Language (XML) and Simple Object Access Protocol (SOAP), the project also provides guidance in leveraging existing best practices from other industries and to promote collaborations among industry partners for mutual benefit.

The investigation also includes an informal survey of semiconductor supply chain partners including designers, chip manufacturers, and equipment suppliers to gauge their existing practices, requirements and priorities. Site visits will provide an opportunity for key industry figures to share their vision of how IT standards would expedite advancement of new technologies and business models.

DELIVERABLES: White paper evaluating semiconductor industry's IT standards needs and priorities as well as an assessment of potential solutions to the current challenges based upon cross-industry solutions facing similar issues. 4Q 2003

As appropriate, the survey also provides an opportunity for providing insights and guidance from similar industry efforts in supply chain and equipment communication standards to facilitate existing standards developments.

In response to industry needs, the survey will validate internal NIST IT projects against the semiconductor industry's requirements. One potential project is the Infrastructure for Integrated Electronics Design and Manufacturing (IIEDM). IIEDM has facilitated neutral XML-based standards development in the electronic exchange of technical and business data in the electronic components supply chain. Similarities in challenges and technologies utilized may provide an opportunity for future collaborations. In addition, experience with standards development in various industries positions NIST to provide impartial cross-industry benchmarks for IT exchange strategies.

DELIVERABLES: Define potential NIST roles in providing technical assistance to facilitate current IT standards development in the semiconductor industry. 4Q 2003

Accomplishments

- Assessed the current and future direction of IT use in semiconductor and mask manufacturing. Site visits conducted at four IC manufacturers, one design house, and one photomask supplier.

- NIST has been co-leading the Engineering Chain Management sub-team of the ITRS Factory Information and Control Systems team. Initial efforts are being made to determine the scope and identify the challenges of creating an effective Engineering Chain.

- Surveyed current standards development activities in semiconductor manufacturing and potential NIST roles in various task forces by participating in a variety of standards activities. Diagnostic Data Acquisition (DDA), XML, Process Control System (PCS), and Equipment Engineering Capabilities (EEC) are possible areas where NIST can play a future role. Leveraging use of mainstream technologies appears to be widely accepted. Data acquisition standards, including issues of data modeling, speed, bandwidth, quality and integrity, have become critical in advancing e-manufacturing efforts. Follow-up discussions with members of SEMI and ISMT indicated interest in enlisting NIST expertise and contacts to leverage best practices from other industries on specific issues such as XML-based standards development for manufacturing, timing and synchronization of equipment data, as well as data security issues.

Collaborations

Alan Weber, Alan Weber & Associates

ITRS Factory Integration Technical Working Group

SEMI XML Task Force

Abbreviations and Acronyms

AC	alternating current
ADR	adiabatic demagnetization refrigerator
AEM	analytical electron microscopy
AES	Auger-electron spectroscopy
AFM	atomic force microscope
ALMWG	Analytical Laboratory Managers Working Group (ISMT)
AMAG	Advanced Metrology Advisory Group (ISMT)
ANSI	American National Standards Institute
ARXPS	angle resolved x-ray photoelectron spectroscopy
ASPE	American Society of Professional Engineers
ATP	Advanced Technology Program (NIST)
BCB	benzocyclobutene
BESOI	bond and etch-back silicon-on-insulator
BGA	ball-grid array
BIPM	Bureau International des Poids et Mésures
BIST	built-in self-test
BST	barium strontium titanate
C-AFM	calibrated atomic force microscope (NIST)
C-V	capacitance-voltage
CAD	computer-aided design
CCD	charge-coupled device
CD	critical dimension
CMOS	complementary metal oxide semiconductor
CMP	chem-mechanical polishing
CRADA	Cooperative Research and Development Agreement
CRDS	cavity ring-down spectroscopy
CSP	chip-scale package
CTCMS	Center for Theoretical and Computational Materials Science (NIST)
CVD	chemical vapor deposition
DC	direct current
DFT	design-for-test
DMA	differential mobility analyzer
DRAM	dynamic random-access memory
DSP	digital signal processing
DUV	deep ultraviolet

EBSD	electron backscatter diffraction
EELS	electron energy loss spectroscopy
EDC	embedded decoupling capacitance
EDS	energy-dispersive spectroscopy
EMC	electromagnetic compatibility
EMI	electromagnetic interference
EPMA	electron probe microanalysis
EUV	extreme ultraviolet
FIFEM	field ion field emission microscope
FIM	field ion microscope
FWHM	full-width half-maximum
GIXR/SE	grazing incidence x-ray reflection/spectrascopic ellipsometry
GIXPS	grazing incidence x-ray photoelectron spectroscopy
HRTEM	high resolution transmission electron microscope
HSQ	hydrogen silsesquoxane
I-V	current-voltage
IGBT	insulated-gate bipolar transistor
IPC	Association Connecting Electronics Industries
ISMT	International SEMATECH
ISO	International Organization for Standardization
ITRS	International Technology Roadmap for Semiconductors
LEED	low-energy electron diffraction
LER	line-edge roughness
LFPG	low frost-point generator
LOCOS	LOCal oxidation of silicon
LPP	laser-produced plasma
LPRT	light-pipe radiation thermometer
MBE	molecular beam epitaxy
MEMS	micro-electro-mechanical systems
MFC	mass flow controller
MMIC	millimeter and microwave integrated circuits
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
MUX	multiplex
NCMS	National Center for Manufacturing Sciences
NDP	neutron depth profiling
NGL	next generation lithography

NEMI	National Electronics Manufacturing Initiative
NIST	National Institute of Standards and Technology
NLO	non-linear optical
NSOM	nearfield scanning optical microscopy
OMAG	Overlay Metrology Advisory Group (ISMT)
PED	Precision Engineering Division (NIST)
PLIF	planar laser-induced fluorescence
PMI	phase-measuring interferometer
PTB	Physikalisch-Technische Bundesanstalt
PZT	lead zirconium titanate
QM	quantum mechanics
RAM	Random-access memory
RGA	residual gas analyzer
RTA	rapid thermal annealing
RTP	rapid thermal processing
SANS	small-angle neutron scattering
SBIR	Small Business Innovative Research
SCM	scanning capacitance microscope
SEM	scanning electron microscope
SHG	second harmonic generation
SIA	Semiconductor Industry Association
SIMOX	separation by implantation of oxygen
SIMS	secondary-ion mass spectrometry
SoC	system-on-chip
SOI	silicon on insulator
SPM	scanning probe microscope
SRC	Semiconductor Research Corporation
SRM®	Standard Reference Material
SSHG	surface second-harmonic generation
SSIS	surface-scanning inspection system
SURF III	Synchrotron Ultraviolet Radiation Facility III
TCAD	technology computer-aided design
TDDB	time-dependent dielectric breakdown
TDR	time-domain reflectometry
TEM	transmission electron microscope
TFTC	thin-film thermocouple
TOF	time-of-flight

TMAH	tetramethyl ammonium hydroxide
UHV	ultra-high vacuum
UV	ultraviolet
WMS	wavelength modulation spectroscopy
VUV	vacuum ultraviolet
XPS	x-ray photoelectron spectroscopy

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