EMI Characterization with Parasitic Modeling for a Permanent Magnet Motor Drive

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ABSTRACT–In this paper , a permanent magnet ac motor drive is tested extensively, and the prominent frequencies in EMI spectrum are identified for their relationship with the noise sources and their propagation paths. Switching characteristics of the power MOSFETs are evaluated by simulation and experiment for the noise source modeling. Major parasitic components and noise propagating mode paths are measured with a time-domain reflectometry method and verified with a 3-dimensional finite element analysis tool. The inverter circuit model is then constructed using pertinent parasitic inductance and capacitance values for the active device modules, the passive components, the leads, and the interconnects. To verify the validity of the inverter model, a comparative study is performed with computer simulations and hardware experiments. The fundamental mechanisms by which the EMI noises are excited and propagated are analyzed, and the significant roles of parasitic elements coupling with device switching dynamics in EMI generation are examined. The results indicate that the identification of parasitic inductance helps verify the noise peaking frequencies. The noise mitigation effects of added dc choke and RC snubbers are also characterized and proven with both simulation and measurement.

1. INTRODUCTION

The electromagnetic interference (EMI) generation and its associated problems in power electronics circuits have been extensively studied for dc/dc converters [1 – 5]. For motor drive applications, especially with low-voltage high current or high torque permanent magnet motors, the EMI is generally more severe than it is for dc/dc converters and commercial industrial drives operating at line voltages. The low-voltage high current devices with fast-switching speed generate high current and voltage slew rates (*di/dt* and *dv/dt*). High slew rates in insulated gate bipolar transistor (IGBT)-based industrial drives have been shown to result in premature winding failure, ground leakage current, shaft voltage and bearing current, etc. [6,7]. These problems can be worse in low-voltage motor drives because the switching speeds of the power MOSFETs are much faster, and the reverse recoveries of the MOSFET body diodes are slower.

Recent studies have indicated that high *dv/dt* is largely responsible for common mode (CM) noise [8 – 10] and high *di/dt* is mainly responsible for differential (DM) noise [11 – 13]. Higher switching *dv/dt* or *di/dt* transitions result in higher EMI emissions. A PWM inverter drive system is very complicated in terms of the power stage, control circuit, interconnections, and packaging. While some EMI phenomena have been described, and some useful conclusions have been drawn in recent studies, the fundamental mechanisms by which the EMI noises are excited and propagated have not been adequately investigated. In addition to the *di*/d*t* and *dv*/*dt* noise sources, the mechanism of EMI propagation through common mode path is quite difficult to identify and can change easily with the environment.

In this paper, a 12 V battery-powered permanent magnet ac motor drive is tested extensively with and without EMI mitigating components such as grounding enclosures, the dc choke, and RC snubbers. Through studies with different circuit configurations, the relationship between the noise source and the mitigating components are identified. In addition to the identification of noise sources, the EMI path related parasitic components are measured and modeled for simulation purposes. Switching characteristics of the power MOSFETs are evaluated and verified with both circuit simulator and hardware experiments. Time-domain reflectometry (TDR) and a three-dimensional finite element analysis-based software tool Spicelink™ [2] are both used for parasitic parameter extraction and verification.

The inverter circuit model is constructed using the major parasitic inductance and capacitance values of the components that comprise the inverter, which are, the active devices, the passive components, device leads, and interconnects. A circuit simulator is used to identify the noise path impedance through frequency-domain analysis and verified with fast Fourier transformation (FFT) analysis after time-domain simulation. The fundamental mechanisms by which the EMI noises are excited and propagated are analyzed, and the significant roles of parasitic elements coupled with device switching dynamics in EMI generation are examined.

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2. INVERTER EMI TEST SETUP

The power circuit of the motor drive system contains an enclosed inverter and an ac PM motor. The inverter power source is a conventional vehicle grade 12-V lead acid battery. In the EMI test setup, a set of line impedance stabilization networks (LISNs) is inserted in between the inverter input and the battery. Fig. 1 shows the EMI test setup for the entire motor drive system. The main path of the conducted EMI is the high frequency switching noise produced by the inverter feeding back through the power inverter circuit, and back to the battery source. The paths for inductances, L_{k1} , L_{k2}, and L_{k3} are originally shorted to earth ground or negative voltage bus, but non-zero inductance values are artificially added to study their impact on the EMI performance. Inductances L_{k4} and L_{k5} are due to wiring cables.

A π-shaped LC filter is inserted between the inverter input and switches to attenuate EMI produced from the switching. With high inductance and capacitance values, the LC filter can reduce the switching noise substantially. The switches are 30-V power MOSFETs with low conduction voltage drops. Each MOSFET is paralleled with an RC snubber. Because the snubber loss is relatively minor in low-voltage systems, the capacitor values can be relatively large to reduce turn-off *dv*/*dt* induced EMI.

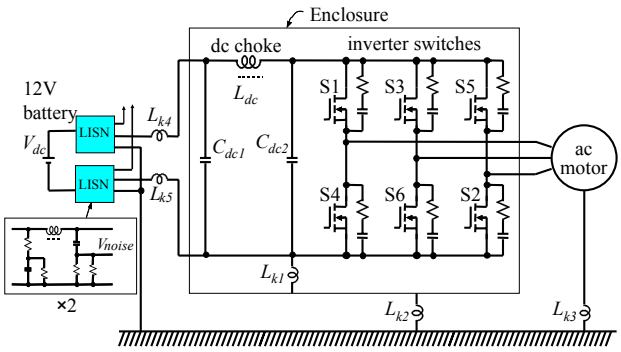


Fig. 1. Power circuit of the entire PM motor drive system.

The LISN provides 50-ohm impedance matching for the entire high frequency range. The output signal V_{noise} of the LISN can be connected to an oscilloscope or to a spectrum analyzer instead of to ground as shown in Fig. 1. A DM and CM separation box can be used at the signal output terminal V_{noise} of either LISN to see which mode of noise is more dominant.

The battery voltage source should not be replaced with a bench top power supply because the bench top power supply output likely contains severe EMI that will invalidate the measurement results. In the physical layout of the test setup, the whole test assembly is sitting on top of a surface that is covered with a copper ground plane. The test object, LISNs, and control box are all mounted on the copper sheet. The battery is located underneath the bench. The copper sheet serves as a common ground that is electrically connected to the power ground.

3. INVERTER EMI TEST RESULTS

Before measuring EMI under operating condition, the background noise pick-up by the LISN is measured to ensure that the measurement results are not corrupted by the background noise. For the entire frequency range, the background noise is generally lower than –90 dBm, and no noise peaks above that are observed.

Fig. 2 shows measured frequency spectra under loaded operating conditions. The test condition for Fig. 2(a) is with all the RC snubbers and the dc choke, L_{dc}, removed. The marked frequency f_1 and its multiples are related to the PWM switching frequency, 20 kHz. Frequencies f_2 (10 MHz) and f_3 (22 MHz) are assumed to be the noises caused by the resonant frequencies of parasitic components, and f_4 (16 MHz) is assumed to be the valley frequency of the parasitic impedance.

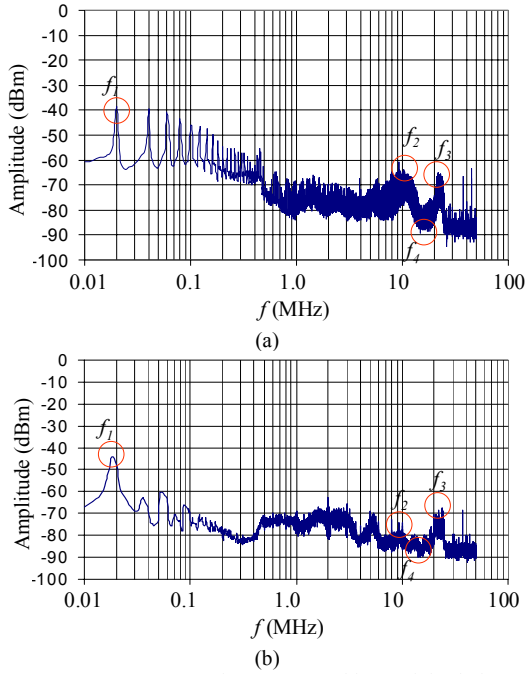
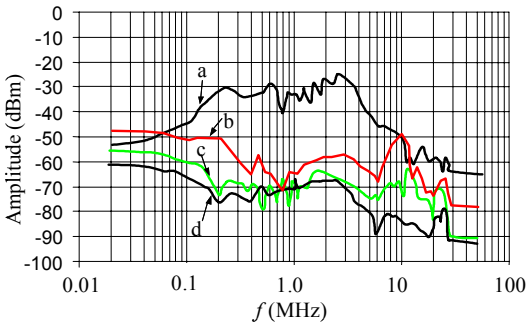


Fig. 2. Inverter EMI test results. (a) RC snubber and dc choke are not connected; (b) RC snubber and dc choke are connected.

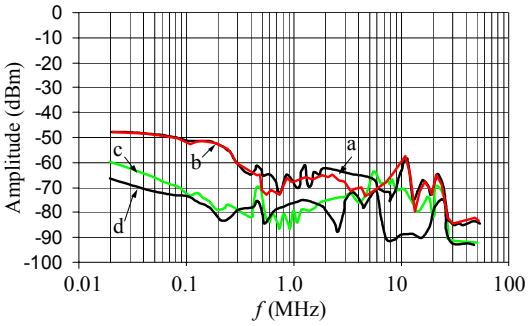
The test condition for Fig. 2(b) is to include all the RC snubbers and the dc choke in the circuit. It appears that the low-frequency switching noises are effectively suppressed with the dc choke, and the 10 MHz noise is suppressed by the RC snubbers, but the 22 MHz noise remains prominent.

In order to identify individual component contribution to EMI, four test conditions with their EMI spectrum envelopes are compared in Fig. 3. Circuit configurations for these four test conditions are listed as follows.

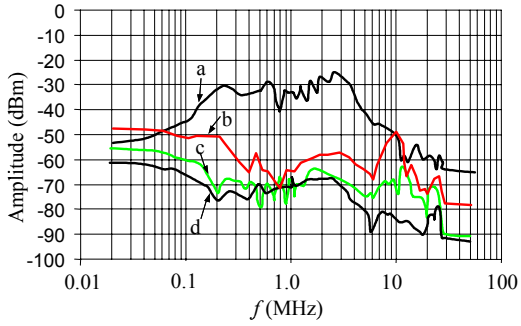
a: Negative dc bus is not grounded, dc choke and RC snubbers are connected.
b: Negative dc bus is grounded, dc choke is shorted, and RC snubbers are disconnected.
c: DC bus is grounded, dc choke is connected, but RC snubbers are disconnected.
d: DC bus is grounded, dc choke and RC snubbers are connected.



(a)



(b)



(c)

Fig. 3. EMI performance envelopes for (a) total EMI; (b) differential mode; (c) common mode.

The first test condition is to have the negative dc bus floating. In this case, the total EMI noise level is much higher than for the other conditions. In comparing DM and CM noise spectra in Fig. 3(b) and (c), it can be seen that the high noise level is common mode coupling rather than differential. Fig. 4 illustrates the conducting directions of the DM and CM noises. With dc bus being floated, the CM noise tends to be coupled through parasitic capacitances.

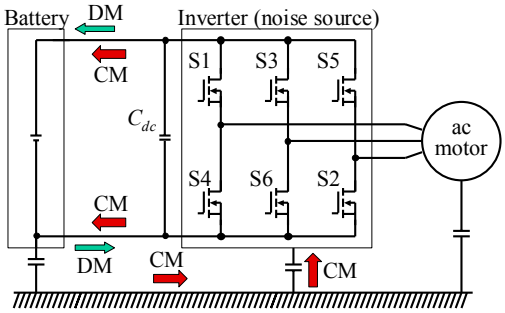


Fig. 4. Conducting paths for DM and CM noises with dc bus being floated.

By comparing curves b and c in Fig. 3(b), it can be seen that the dc choke suppresses the DM noise by 10 to 20 dB for the switching frequency and its multiples up to 3 MHz. The curves b and c of Fig. 3(c) also indicate that the dc choke suppresses the CM noise by about 10 dB over the almost entire frequency range.

The RC snubbers contribution to EMI reduction can be observed between curves c and d in Fig. 3(c). A 30 dB reduction is observed in 10-MHz region where the noise seems to be related to the resonant frequency of the propagation path impedance. Adding snubbers not only slows down the dV/dt during turn-off, but also changes the circuit impedance characteristics. The noise at 22 MHz peaking frequency is somewhat reduced with both dc choke and RC snubbers, but the reduction level is not as significant as that at 10 MHz.

4. Noise Propagation Path Modeling

The parasitic inductance of power MOSFETs and main power circuit components can be measured with the time-domain reflectometry (TDR) method [9]. The method is based on the transmission line theory. Physically it can be explained that an electrical signal traveling through the media of a conductor is partially reflected as it encounters impedance mismatches along the path. The media can be viewed as a series of conductive planes. The signal gets reflected at each plane and some of it may travel back to the source. The reflection coefficient ρ_i, which is defined as the ratio of the reflected voltage to the incident voltage, is simply determined by the media impedances Z_i at the reflection plane. Hence, the impedance profile or Z-profile, defined as the varying impedance along the signal path, can be computed if the reflected signal with respect to delay time is measured. Therefore, any electrical conductor, for example, a lead in a package, can be modeled as a distributed transmission line with varying impedance along its path. In general, it is not practical to use a distributed transmission line model but is more desirable to reduce the model to a string of transmission line segments with reasonable approximation.

The simulated profile can be translated into an equivalent circuit model. Fig. 5 shows the TDR measured transmission line model and its translated equivalent loop inductance

between gate and drain. This model consists of a transmission line, which is assumed to be the paralleled leads of the device package, and a set of LC circuit elements which are assumed to be the wire-bond inductance and package capacitance. Because the capacitance in the equivalent circuit is too small to have any significant impact, the complete parasitic model can be further simplified with a pure inductance, and thus the complete power MOSFET parasitic model can be established. Notice that the measured lead length is taken from the actual printed circuit board layout, and the lead length between gate and drain, between drain and source, and between gate and source are all the same; thus the model shows equal parasitic inductance for gate, drain, and source.

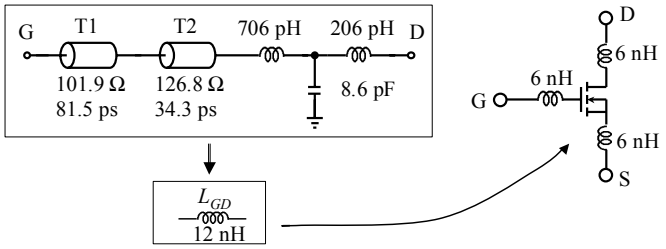


Fig. 5. Model of the power MOSFET with the transmission line and equivalent inductance models. Values shown were obtained from TDR measurements.

The same device parasitics were analyzed through simulation. The resulting inductance and capacitance values are provided in 3×3 matrices, as shown in Table 1. In this table, the diagonal elements of the matrices are self inductances or capacitances, and the off-diagonal elements are the mutual inductances or capacitances, ie., $L_{dd} = L_{gg} = L_{ss}$ = 10.9 nH, $L_{dg} = L_{gd}$ = 4.97 nH, $L_{gs} = L_{sg}$ = 3.19 nH, $L_{ds} = L_{sd}$ = 4.99 nH, C_{dd} = 0.58 pF, $C_{gg} = C_{ss}$ = 0.47 pF, $C_{dg} = C_{gd}$ = 0.23 pF, $C_{gs} = C_{sg}$ = 0.056 pF, $C_{ds} = C_{sd}$ = 0.23 pF.

Table 1. Simulation results of the device parasitics

	Inductance (nH)			Capacitance (pF)		
Lead	drain	gate	source	drain	gate	source
Drain	10.9	–4.97	–4.99	0.58	–.23	–.23
Gate	–4.97	10.9	3.19	–.23	0.47	–.056
Source	–4.99	3.19	10.9	–.23	–.056	0.47

The simulated inductance mathematically represents the component of the inductance that results from the part of the current loop being modeled, such as current flowing into the drain lead and coming out of gated lead. Physically, partial inductance is an approximation of loop inductance and is used in situations where the return path for the current cannot be explicitly specified. This is the case of the device being simulated, and the loop inductance can be obtained by

$$L_{loop\text{-}dg} = L_{dd} + L_{gg} - L_{dg} - L_{gd} = 11.8 \text{ nH}$$

The computed loop inductance matches the TDR measurement result. Note that the loop inductance between gate and source is larger because their spacing is wider. Although the exact model should contain self and mutual coupling inductances, all the self and mutual inductances can be equivalent with loop inductance through circuit analysis. . Therefore, the simplified model representing the loop inductance can still be used to characterize the EMI performance without much deviation on impedance prediction.

The capacitance value gives the relationship between the total charge and potential of each object relative to the ground, or the outside reference boundary with zero potential. The capacitance in between each lead and the reference ground can be calculated as follows.

$$C_{d0} = C_{dd} - C_{dg} - C_{ds} = 0.12 \text{ pF}$$

$$C_{g0} = C_{gg} - C_{gd} - C_{gs} = 0.18 \text{ pF}$$

$$C_{s0} = C_{ss} - C_{sd} - C_{sg} = 0.18 \text{ pF}$$

These capacitances are fractions of a pico Farad and can be neglected in the system simulation.

5. NOISE SOURCE MODELING

It should be noticed that the load inductance is considered open circuit at high frequencies and with LISN impedance matching, the high frequency noise equivalent circuit for one phase leg can be simplified, as shown in Fig. 6. The noise voltage source, V_n, needs to be considered only when the common mode propagation path is present. The noise current, I_n, however, presents in both DM and CM equivalent circuits. The product of noise current and noise path equivalent impedance is the noise picked up by the LISN, V_{noise}.

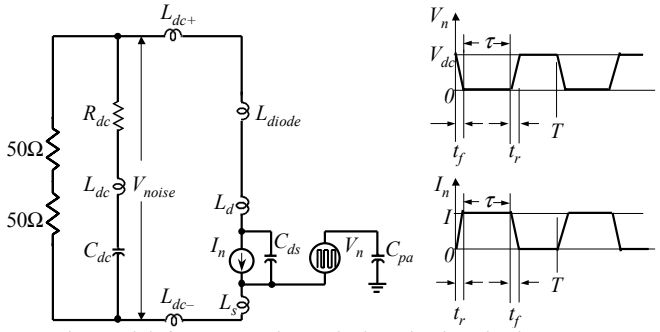


Fig. 6. High frequency noise equivalent circuit and noise source representations.

The switching noise source can be considered as a trapezoidal pulse train. Although the actual waveform will have different rise and fall times (t_r and t_f), to simplify the analysis, it is reasonable to assume the $t_r = t_f$ and both t_r and t_f are the 0 % and 100 % transition durations, not the typical 10 % and 90 %. . The frequency domain representation of the noise current and voltage can then be expressed as in (1) and (2), respectively.

$$I_n = 2Id\frac{\sin(n\pi d)}{n\pi d}\frac{\sin(n\pi t_f/T)}{n\pi t_f/T}\ell^{-j\frac{n\pi(\tau+t_f)}{T}} \quad (1)$$

$$V_n = 2V_{dc}(1-d)\frac{\sin(n\pi(1-d))}{n\pi(1-d)}\frac{\sin(n\pi t_f/T)}{n\pi t_f/T}\ell^{-j\frac{n\pi(T-\tau+t_f)}{T}} \quad (2)$$

$$d = \tau/T \quad (3)$$

In the above expressions, d is the duty cycle, T is the inverter switching period, I is the current amplitude, τ is the on time of the switch and n is the harmonic order. The noise source plot shows an initial –20 dB/dec drop, and an additional –20 dB/dec drop in the high frequency region, which is attributed to the switching period and fall time. A slower switching speed means larger t_f, which subsequently yields a lower cut-off frequency or less noise in high frequency range. Fig. 7 shows the spectral representation of a current source with 30 and 70 ns fall time, respectively. Different fall times can be obtained by varying the gate resistance. A larger gate resistance would result in a lower noise source spectral envelope. However, the downside of a larger gate resistance is a higher switching loss.

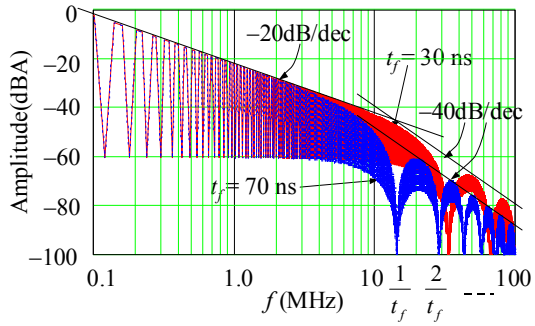


Fig. 7. Spectral representation of noise source for different fall times.

In order to verify the parasitic measurement and to study the EMI effect, a two-quadrant chopper based device tester was fabricated and simulated. Fig. 8 shows circuit diagram of the device tester with component values indicated. The device used here is a 30-V, 180-A power MOSFET in a super TO-220 package. Switches S_1 and S_4 are the main switching devices that turn on and off simultaneously. Switches S_2 and S_3 serve as the freewheeling diodes with their gates shorted. The measurement points are the device voltage v_{ds}, device current i_{s4}, and freewheeling diode current i_{s2}. The leakage inductance L_{lk} value is 6 nH throughout the entire circuit.

Fig. 9 shows the experimental device voltage and current waveforms. During turn-on, the diode reverse recovery current is added to the device drain current, i_{s4}, thus an over-current of 10 A is observed. Current i_{s2} is measured from the other phase leg. It is initially negative because the body diode is conducting. The current rise rate is about 25 A/ns. During turn-off, the current falls 30 A in 50 ns, or di/dt = 0.6 A/ns. A voltage overshoot of 16 V is observed. This voltage overshoot is well correlated to the product of the loop inductance and di/dt. Here the total lead inductance of two MOSFETs is 24 nH, and the total parasitic inductance of the sensor resistor and interconnect is about 2.5 nH. The voltage rise time during turn-off is 24 V in 12 ns, or dv/dt = 2 V/ns. Such a high dv/dt can cause severe EMI noise and is objectionable in any motor drives because it not only produces EMI noise in the inverter, but it also introduces common mode EMI noise through the motor bearing and shaft to ground. References [1 – 3] already reported such a problem in industrial drives.

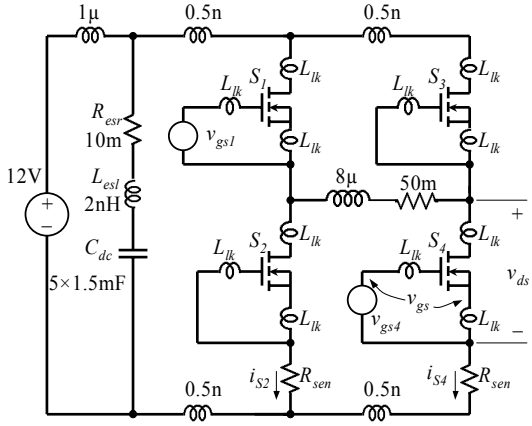


Fig. 8. A two-quadrant chopper based device tester.

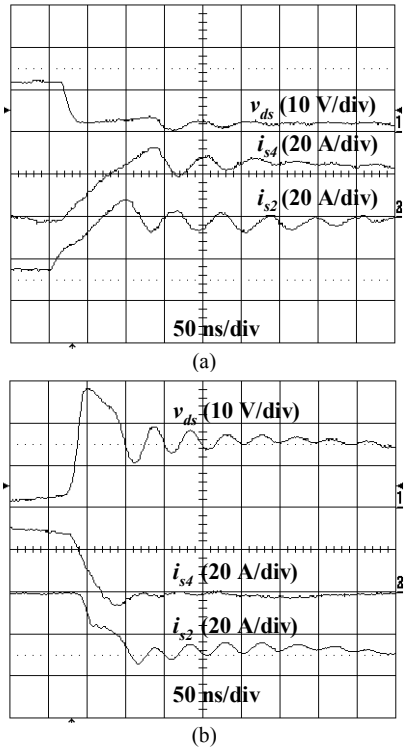


Fig. 9. MOSFET and its body diode turn-on and –off voltage and current waveforms: (a) turn-on; (b) turn-off.

6. SIMULATION VERIFICATION

The EMI simulation for the entire motor drive including inverter and motor is nontrivial, and often results in convergence problems in circuit simulators. The approach adopted here is to simulate the EMI source and EMI propagation paths separately. As described in Section 3, the EMI source to be determined is the device switching, and the EMI path to be determined is the parasitic component. Therefore, in simulation verification, these two parts are simulated separately to avoid numerical problems.

A. Simulation of EMI Source – Device Switching

The device model provided by manufacturer does not include leakage inductance for all three leads, that is, the manufacturer's model sets $L_{lk} = 0$ for gate, drain, and source leads. Simulations with models including and not including L_{lk} show significantly different results. Fig. 10(a) and (b) compare the simulation results of device turn-on behavior with and without including L_{lk}. Without L_{lk}, the turn-on rise time of i_{s4} is significantly shorter. The turn-on current rising rate in simulation with L_{lk} matches that in experimental result, which is about 0.35 A/ns. Note that parasitic of the current sensing resistor and instrumentation probe are not include in the simulation, hence, there is difference in the high frequency oscillation of V_{dc} and i_{s4} between experimental result and simulation result. The frequency of the oscillation in experiment is about 15 MHz while it is about 18 MHz. It should be noticed from Fig. 8, that the voltage v_{gs} is the voltage across the gate and source, not the gate driver output voltage, which normally exhibits small aberrations that have quickly decayed to the noise level of the signal. The waveform in Fig. 10(b) shows the evidence that if the gate driver output voltage exhibits small quickly-decaying aberrations, then the voltage across gate and source will exhibit similar aberrations if $L_{lk} = 0$.

Fig. 11 (a) and (b) compare the device turn-off simulation results with and without L_{lk}. As with the turn-on behavior without L_{lk}, V_{ds} after turn-off shows a higher ringing frequency and a faster dv/dt than with L_{lk} included in the model. With L_{lk} included in the model, the turn-off current falling rate matches it in experimental result showing in Fig. 9(b), which is about 0.5 A/ns. The V_{ds} waveform shows the same voltage overshoot 28V and one cycle oscillation delay after the voltage overshoot as appears in Fig. 9(b). After V_{ds} increases to the first peak, the two cases simulated behave dramatically different. With L_{lk} included in the simulation, the oscillation in V_{ds} is delayed for at least one cycle because V_{gs} does not increase to a level necessary to turn the device fully off. Notice that the device is logic-level driven, a small amount of gate-source voltage can prevent it from fully turning off. Without L_{lk}, V_{gs} will not cause a delay in the oscillations of V_{ds}, and the simulation results will not match the experimental results.

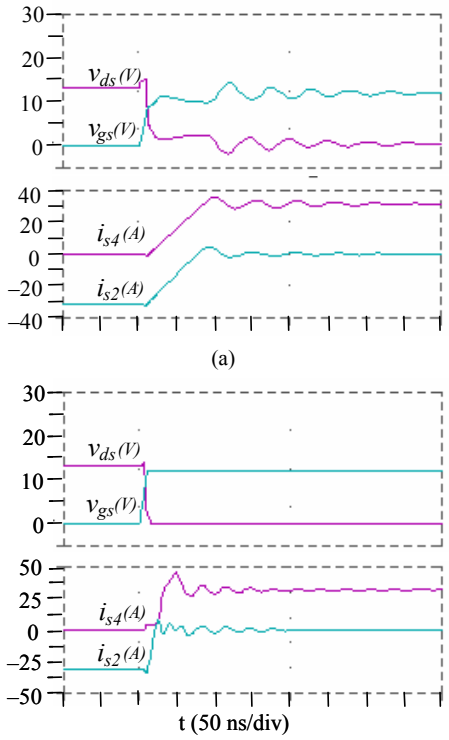


Fig. 10. Simulated turn-on voltage and current waveforms: (a) with leakage inductance included; (b) without leakage inductance.

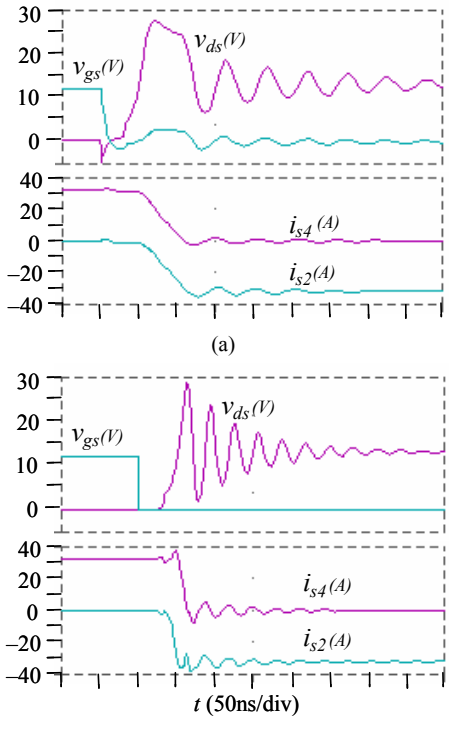


Fig. 11. Simulated turn-off voltage and current waveforms: (a) with leakage inductance included; (b) without leakage inductance included.

To reduce turn-off dv/dt, the simplest way is to add resistor-capacitor (RC) snubbers across the device. The drawbacks to such a solution are additional loss and noise during device turn-on. Fortunately, for a low-voltage drive, the loss associated with $\frac{1}{2}CV^2$ is quite small and can be neglected in overall efficiency considerations. The benefit of adding RC snubbers for EMI reduction is thus not compromised. The experimental unit shown in Fig. 1 includes 1-Ω and 1-μF RC snubbers across each device.

B. Simulation of EMI Propagation Path

Fig. 12(a) shows the magnitude of the transfer function of the EMI propagation path impedance plots without RC snubbers. The simulation setup is to replace one device with the voltage source and apply the small-signal perturbation to see the response at the dc link current, or the LISN pickup.

Fig. 12(a) is the simulated frequency response without RC snubbers and without the dc choke. In this case, the EMI signal peaks at about 10 MHz and 22 MHz, which is consistent with the experimental results shown in Fig. 2 and 3.

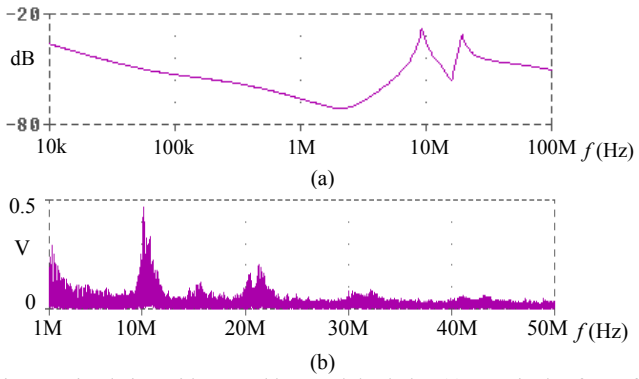


Fig. 12. Simulation without snubbers and dc choke. (a) magnitude of transfer function of noise path, and (b) FFT of noise voltage.

It is well known that the noise voltage picked up at the LISN output can be calculated as

$$V_{noise}(f) = I_n(f) \cdot Z(f) \tag{4}$$

where $I_n(f)$ is the noise source current expressed in (1), and $Z(f)$ is the impedance as a function of frequency shown in Fig. 12(a). According to Fig. 7, the noise source affects the noise cut-off frequency for the inverter studied, and according to Fig. 12(a), the noise path impedance affects the magntiude of the noise spectrum, inlcuding peak noise frequencies. The same circuit is then simulated in time-domain followed with FFT, and the result is shown in Fig. 12(b). Again the EMI peaking frequencies are 10 MHz and 22 MHz.

7. CONCLUSIONS

The determination of EMI source and path in a low-voltage high-current ac motor drive system is non-trivial. In this paper, the inverter switching related noise is identified through both measurement and simulation. The observation of parasitic inductance using TDR measurements and simulations helps verify the occurrence of the voltage spike during turn-off and the current spike during turn-on. The conducted EMI noise caused by the propagation path, which includes parasitic components of bus capacitor, dc bus, and devices, is proven to be identifiable in this paper. The ultimate goal of this EMI study was to understand the causes of EMI and find ways of alleviating or eliminating them.

Throughout the overall empirical and analytical effort, several conclusions can be drawn as follows.

(1) Accurate device and parasitic models are the key to successful prediction of EMI simulation.

(2) PWM frequency related EMI is typically in the tens of kilohertz range and appears to be in the DM propagating path. The PWM noise frequency and its harmonics can be effectively mitigated by a dc link choke.

(3) Device switching is the primary noise source. The switching rise and fall times affect the high frequency noise cut off.

(4) Resonant frequencies of the EMI propagation path impedance are associated with the peak noise frequencies. These frequencies can be identified through frequency domain simulations, allowing avoidance of nontrivial time-domain simulation and its related numerical problems.

(5) RC snubbers help EMI noise reduction in certain peak noise frequencies that are associated with the propagation path impedance and noise sources. Adding RC snubbers is effective noise mitigation for low-voltage inverter drives without incurring excessive power losses.

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