

# Thermal transport in stacked superconductor–normal metal–superconductor Josephson junctions

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Nb/MoSi<sub>2</sub>/Nb stacked superconductor–normal metal–superconductor (SNS) Josephson junctions has proven to be a good candidate for high-density series arrays for Josephson voltage-standard applications. As the junction density increases, self-heating becomes an issue because the high power density per junction (1 W/cm<sup>2</sup>) generates significant power dissipation under typical operating conditions. In this letter, we analyze the heating effect of these sandwich-type SNS junctions using a model to quantitatively estimate and predict thermal-transport properties of the stacked structures. We describe several strategies that reduce heating and demonstrate improved properties of stacked-junction arrays with enhanced cooling capacity. [DOI: 10.1063/1.1606491]

Superconductor–normal metal–superconductor (SNS) Josephson junctions have become the dominant technology for next-generation Josephson voltage metrology because of their inherent stability.<sup>1–3</sup> Our goal is to increase the linear density of such junctions in order to achieve higher voltages and higher output frequencies.<sup>4</sup> Vertically stacked junctions have proven to be the best candidate among the various approaches for achieving this goal.<sup>5–8</sup> However, as the number of junctions in a stack increases, the heat generated within the stack increases and must be transferred to the substrate through the same contact area as that of a single junction. Thus, removing the heat in stacked junctions is a serious challenge because inadequate cooling will limit the ultimate performance that can be achieved in future Josephson voltage-standard systems. Similar considerations will also impact other high-power-density Josephson circuits.

In this letter, we report the use of MoSi<sub>2</sub>-barrier junctions to study the heat transport in SNS junctions. MoSi<sub>2</sub> is a material with higher resistivity than that of the conventional PdAu barrier material, and has proven to be an excellent normal–metal barrier for stacked SNS Josephson junctions.<sup>5,6</sup> A single 5.5 μm×5.5 μm square, 23-nm-thick MoSi<sub>2</sub>-barrier junction typically has a characteristic voltage  $I_c R_n \approx 35 \mu\text{V}$ , a critical current of  $I_c \approx 9 \text{ mA}$ , and normal resistance of  $R_n \approx 4 \text{ m}\Omega$ . The junctions are usually operated at 16 GHz, giving an output voltage of 32 μV per junction when current biased near the critical current. A single junction therefore typically dissipates  $\sim 0.3 \mu\text{W}$ , corresponding to a power density  $\sim 1 \text{ W/cm}^2$ . This is much lower than the  $\sim 5 \text{ W/cm}^2$  for PdAu-barrier junctions with similar electrical properties because the area of MoSi<sub>2</sub> junctions is about five times larger. Regardless of barrier materials, in a stack the power density scales roughly linearly with the number  $N$  of junctions.

Figure 1 shows a schematic cross section of the planar junction geometry. Since our application focus is voltage-standard systems, we desire junctions of higher resistance that generate less power at the same voltage, and larger junc-

tions that have smaller power density at the same power. In addition to small power density, the critical-current uniformity is better in larger junctions for a given degree of etch anisotropy.

As we increase the bias current to an array of junctions above its  $I_c$ , there is a maximum current  $I_{\text{max}}$  at which the superconducting structure goes normal and the voltage abruptly increases, as shown in Fig. 2. The value of  $I_{\text{max}}$  should be far larger than  $I_c$  in order to have a large operating-current range for voltage-standard applications. We also define the maximum power generated in the stack,  $P_{\text{max}} = I_{\text{max}} V_{\text{max}}$ , where  $V_{\text{max}}$  is the voltage at  $I_{\text{max}}$ . By measuring  $P_{\text{max}}$  for junctions in different array test structures on the same wafer with different dimensions of superconducting base electrode and different sizes of base-electrode-to-wiring vias, we conclude that  $P_{\text{max}}$  is limited by heating near the junction. In stacked junctions we observe that  $P_{\text{max}}$  is inversely proportional to the number of junctions in the stack, which indicates that  $I_{\text{max}}$  is directly related to the heat generated in a stack.

If the temperature rise is too great within the junction structure, the junction characteristic will change according to its temperature dependence. Hence, it is important to study the heat flow in a single junction and to adequately cool the junction at its typical operating power. We have established a very reproducible trilayer process such that run-to-run variations in  $I_{\text{max}}$  are small.<sup>6</sup> Equipped with this consistent “ther-

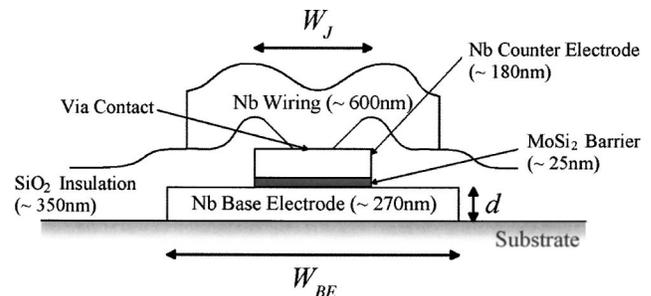


FIG. 1. Cross-sectional view of the SNS junction geometry. Heat is generated in the MoSi<sub>2</sub> barrier and assumed to be transported first through the base electrode and then into the substrate.

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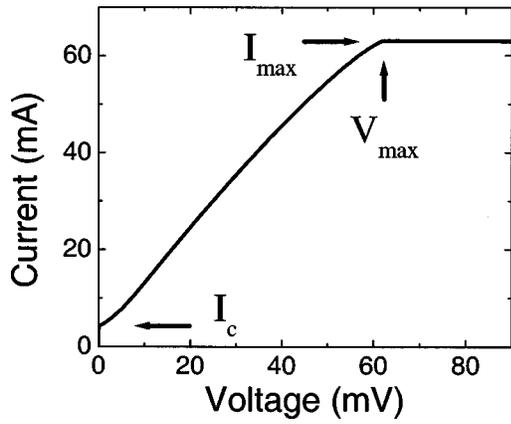


FIG. 2. Current–voltage characteristic of a 100-junction series array.  $I_{\max}$  and  $V_{\max}$  are defined as shown in the figure. The junctions in the measured array are  $4\ \mu\text{m}$  square with a  $16\ \mu\text{m}$  square base electrode on bare silicon with a metal etch stop.

mal fuse” on the chip, we are able to quantitatively investigate the thermal transport properties of different junction structures by measuring  $I_{\max}$ .

For the purpose of modeling the heat flow, we assume that  $I_{\max}$  occurs when the total power generated *within the stack*,  $P_{\max}$  equals  $P_{\text{cool}}$ , the maximum (total) heat flow out of the stack structure. Several factors affect the cooling capacity of the structure, and the nature of the heat flow determines the dependence of  $I_{\max}$  on each design parameter.

Figure 3 displays a linear dependence of  $P_{\max}$  on junction size in single-barrier junctions with the base electrode width fixed at  $16\ \mu\text{m}$ . Data are shown from three wafers with different interfaces between the Nb base electrode and the silicon substrate; one is fabricated on the bare silicon, another has a thin metal etch stop, and the third has thermally grown  $\text{SiO}_2$   $150\ \text{nm}$  thick. The etch stop metals that we tested were PdAu, Al, and Ti, with thicknesses less than  $50\ \text{nm}$ . Neither the type of metal etch stop nor the thickness had any noticeable effect on  $P_{\max}$ . The data in Fig. 3 show that the best cooling occurs when the base electrode is grown on top of the bare silicon wafer.

We modeled the heat transport in our junctions using the results of Skocpol *et al.*<sup>9</sup> and Dieleman *et al.*<sup>10</sup> The chips are

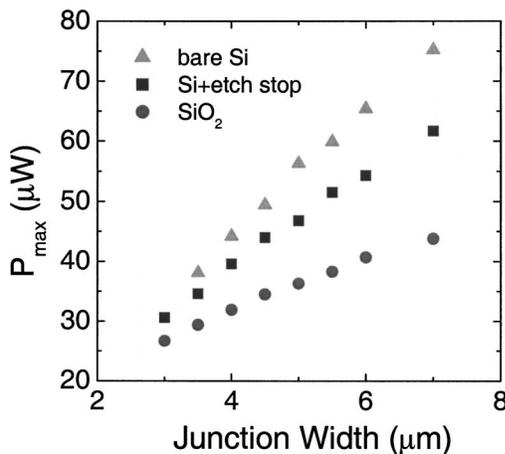


FIG. 3. Maximum power per junction,  $P_{\max}$  vs the junction width,  $W_J$  for different interfaces between base electrode and substrate. The square base electrode size is fixed at  $16\ \mu\text{m}$ . The best cooling occurs when the base electrode is in direct contact with the silicon wafer.

immersed in liquid helium, but because the Kapitza thermal boundary resistance between Nb and liquid helium is large, this is not a dominant thermal path. We assume that the dominant thermal path progresses radially from the junction through the base electrode and then into the substrate.<sup>10</sup> Two thermal parameters determine the heat flow, the thermal conductivity  $\kappa$  of the niobium electrode, and the thermal boundary conductance  $Y$  between Nb and the substrate. If we assume an isothermal, cylindrical junction with an infinite base electrode, the thermal profile of the base electrode is given by<sup>9,10</sup>

$$T(r) - T_{\text{bath}} = \begin{cases} \frac{I \cdot V \eta}{\pi \kappa d W_J K_1(W_J/2\eta)} K_0\left(\frac{r}{\eta}\right) & r > \frac{W_J}{2} \\ \frac{I \cdot V \eta}{\pi \kappa d W_J K_1(W_J/2\eta)} K_0\left(\frac{W_J}{2\eta}\right) & r < \frac{W_J}{2} \end{cases} \quad (1)$$

where  $K_0$  and  $K_1$  are modified Bessel functions,  $r$  is the distance from the center of the junction,  $d$  is the thickness of the Nb base electrode,  $\eta = (\kappa \cdot d / Y)^{1/2}$  is the characteristic thermal healing length in the Nb film,  $W_J$  is the junction width, and  $T_{\text{bath}}$  is  $4\ \text{K}$ , the temperature of the liquid helium bath, which is also assumed to be the substrate temperature. The thermal healing length is a characteristic distance over which heat is transported in the film before equilibrating with the substrate. When the temperature within the cylindrical hot spot exceeds the critical temperature  $T_c$  of the superconducting lead, that is, if  $T(W_J/2) > T_c$ , the junction structure becomes normal. Thus, the maximum power that the junction can dissipate without going normal is

$$P_{\max} = 2\pi\kappa d \left[ \frac{W_J K_1(W_J/2\eta)}{2\eta K_0(W_J/2\eta)} \right] (T_c - T_{\text{bath}}) \approx 2\pi\kappa d \left( \frac{W_J}{2\eta} + \frac{1}{2} \right) (T_c - T_{\text{bath}}), \quad (2)$$

where the modified Bessel functions are approximated as  $xK_1(x)/K_0(x) \sim x + 1/2$  if  $x \gg 1$ . Because  $P_{\max} \approx NI_{\max}^2 R_n \propto W_J$  for  $W_J \gg \eta$  in stacked junctions, where  $N$  is the number of the junctions in a stack, it follows that  $I_{\max} \propto W_J^{3/2} N^{-1/2}$  because  $R_n \propto W_J^{-2}$ . We observe this  $N^{-1/2}$  scaling for  $I_{\max}$  in our stacked junctions. From Eq. (2), the slope in Fig. 3 is proportional to the ratio of the thermal conductivity of the Nb film to the thermal healing length. The linear scaling shown in Fig. 3 is consistent with the assumption of the model that the main heat flow is radial. Therefore, the total cooling power  $P_{\text{cool}}$  will be proportional to the circumference of the junction, with a fixed large base electrode.

The model predicts that if the area of the base electrode is increased, the cooling power will increase until it saturates a few healing lengths outside the junction edge. A theoretical curve for  $P_{\max}$  may be calculated by integrating the local heat flow up to the edge of the base electrode assuming the thermal profile,  $T(r)$ , for an infinite base electrode,

$$P_{\max} = P_{\text{cool}}(W_{\text{BE}}) \approx \int_0^{W_{\text{BE}}/2} Y [T(r) - T_{\text{bath}}] (2\pi r) dr. \quad (3)$$

Figure 4 shows the measured base-electrode size dependence of  $P_{\max}$  with the junction width fixed at  $4\ \mu\text{m}$ . Lines are fit to Eq. (3) with the constraint that the junction is at

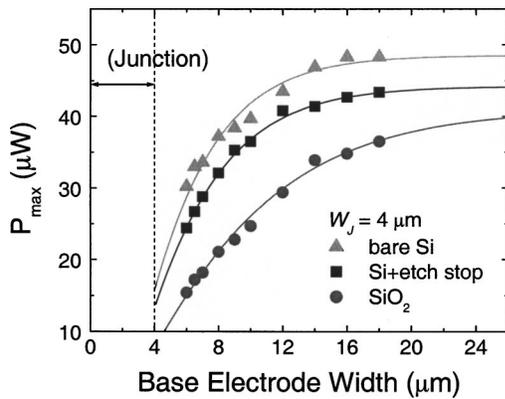


FIG. 4. The maximum dissipated power,  $P_{\max}$  vs the base electrode width  $W_{\text{BE}}$  with the junction size fixed at  $4 \mu\text{m}$ . From the fits, the healing lengths are inferred to be  $1.5 \mu\text{m}$  on bare silicon,  $1.7 \mu\text{m}$  on silicon with a metal etch stop, and  $2.7 \mu\text{m}$  on  $150 \text{ nm}$  of thermal oxide.

$T_c \sim 9 \text{ K}$ .<sup>11</sup> From this fit, we can deduce the thermal healing length in the Nb base electrode for each substrate. These values, together with the slope of  $P_{\max}$  versus the junction size in Fig. 3, lead to an estimate of the thermal conductivity in the niobium film and the thermal boundary resistance between Nb and the substrate. These values are summarized in Table I.

The inferred thermal conductivity values of our sputtered Nb films listed in Table I are in good agreement with the values reported for polycrystalline Nb bulk samples at  $4 \text{ K}$ .<sup>12,13</sup> We note that there are two factors that may cause errors in the estimation of the thermal conductivity values from the measurement. Because we are measuring the thermal parameters at  $P_{\max}$ , the base electrode is not at the bath temperature, but at an elevated temperature close to  $T_c$ , at which there are more quasiparticles available for thermal transport. There is also some cooling that will occur through the top wiring layer, hence the Nb thickness  $d$  in Eq. (2) will be effectively larger than the actual base electrode thickness listed in Table I. Both factors would cause overestimation of the thermal conductivity.

Based on all these results, we compare these test arrays with real fabricated arrays that have a higher linear junction density, but are thermally nonideal because of the small base

TABLE I. Summary of the thermal variables estimated from all the measured wafers. The base electrode thickness,  $d$ , is measured from the wafer, while the thermal healing length  $\eta$ , the thermal conductivity,  $\kappa$ , and the thermal boundary conductance,  $Y$  are inferred from Figs. 3 and 4.

Base contact	$d$ (nm)	$\eta$ ( $\mu\text{m}$ )	$\kappa$ (W/m K)	$Y$ (W/m <sup>2</sup> K)
150 nm SiO <sub>2</sub> on silicon	290	2.7	2.6	$1.0 \times 10^5$
Bare silicon + metal etch stop	280	1.7	3.0	$2.9 \times 10^5$
Bare silicon	210	1.5	4.8	$4.5 \times 10^5$

electrodes used in our standard design. Using our standard lithographic masks, we fabricated and measured an array of five-junction stacks on a silicon wafer with a PdAu etch stop with  $I_c \approx 7 \text{ mA}$ ,  $I_c R_n \approx 30 \mu\text{V}$ , and  $I_{\max} \approx 30 \text{ mA}$  with  $5.5 \mu\text{m}$  stack width, on a base electrode  $7 \mu\text{m}$  wide. For this device  $I_{\max} \sim 4 I_c$ , and thus the power generated during operation is about  $\sim 1/16$  of  $P_{\max}$ , which will increase the junction temperature by  $\sim 0.25 \text{ K}$ . This is a significant improvement because an identical design with two-junction stacks grown on thermal oxide has similar  $I_{\max} \approx 30 \text{ mA}$ . This result shows that even for an array with a high linear density but a small base electrode, the maximum power is increased by improving the base-to-substrate interface.

The measurements and analysis given in this letter provides a practical method for determining thermal transport properties in superconducting thin film devices. In addition, having an analytic model and inferred values of the thermal parameters allows *a priori* quantitative calculation of the heat transport of a structure, thus providing a method for eliminating stacked structures with poor thermal design. This quantitative measurement of thermal transport effects in SNS Josephson junctions provides a framework for future study of other superconductive circuits where thermal effects are important.

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<sup>1</sup>S. P. Benz, C. A. Hamilton, C. J. Burroughs, T. E. Harvey, and L. A. Christian, Appl. Phys. Lett. **71**, 1866 (1997).

<sup>2</sup>R. Pöppel, D. Hagedorn, T. Weimann, F.-I. Buchholz, and J. Niemeyer, Supercond. Sci. Technol. **13**, 148 (2000).

<sup>3</sup>H. Yamamori, M. Itoh, H. Sasaki, A. Shoji, S. P. Benz, and P. D. Dresselhaus, Supercond. Sci. Technol. **14**, 1048 (2001).

<sup>4</sup>R. H. Ono and S. P. Benz, Proc. 7th Inter. Sup. Elect. Conf. (ISEC'99), 21–25 June 1999, Berkeley, pp. 301–303.

<sup>5</sup>Y. Chong, P. D. Dresselhaus, S. P. Benz, and J. E. Bonevich, Appl. Phys. Lett. **82**, 2467 (2003).

<sup>6</sup>P. D. Dresselhaus, Y. Chong, J. H. Plantenberg, and S. P. Benz, IEEE Trans. Appl. Supercond. **13**, 930 (2003).

<sup>7</sup>H. Yamamori, M. Ishizaki, M. Itoh, and A. Shoji, Appl. Phys. Lett. **80**, 1415 (2002).

<sup>8</sup>R. H. Hadfield, G. Burnell, D. J. Kang, M. G. Blamire, P. D. Dresselhaus, and S. P. Benz, Supercond. Sci. Technol. **14**, 1086 (2001).

<sup>9</sup>W. J. Skocpol, M. R. Beasley, and M. Tinkham, J. Appl. Phys. **45**, 4045 (1974).

<sup>10</sup>P. Dieleman, T. M. Klapwijk, S. Kovtonyuk, and H. van de Stadt, Appl. Phys. Lett. **69**, 418 (1996).

<sup>11</sup>The  $T_c$  of the films was measured to be  $9.2 \text{ K}$ . We assume that this current-biased structure has a  $T_c$  between  $8$  and  $9 \text{ K}$ . We choose  $9 \text{ K}$  for simplicity, but an  $8 \text{ K}$   $T_c$  would only lead to  $25\%$  higher thermal conductivities.

<sup>12</sup>K. Mendelssohn and H. M. Rosenberg, Proc. Phys. Soc., London, Sect. A **65**, 385 (1952), K. Mendelssohn and J. L. Olsen, *ibid.* **63**, 2 (1950).

<sup>13</sup>Thermal Conductivity, Thermophysical Properties of Matter Vol. 1, edited by Y. S. Touloukian, R. W. Powell, C. Y. Ho, and P. G. Klemens (Plenum, New York, 1970).