Thickness Evaluation for 2nm SiO_2 Films, a Comparison of Ellipsometric, Capacitance-Voltage and HRTEM Measurements

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Abstract. We have completed a comparison of SiO_2 film thicknesses obtained with the three dominant measurement techniques used in the Integrated Circuit industry: ellipsometry, capacitance-voltage (C-V) measurements and high resolution transmisission electron microscopy (HRTEM). This work is directed at evaluating metrology capability that might support NIST- traceable Reference Materials for very thin dielectric films. Particular care was taken in the design of the sample set to allow redundancy and enable estimates of oxide layer consistency. Ellipsometry measurements were analyzed using a variety of models of the film structure, and C-V results were analyzed using three different quantum-mechanical based algorithms to account for quantized states in the substrate and depletion effects in the polysilicon capacitor electrode. HRTEM results were supplemented with Electron Energy-Loss Spectroscopy. A range of thicknesses was found with each of the methods, but with some overlap of values. HRTEM and STEM values showed less consistency between wafers than the C-V data for the capacitors used and were seen to be more influenced by local variations such as interface non-uniformities. Sources of variation and estimates of uncertainty for the analyses are presented. Implications of these results for Reference Materials are discussed.
Key words: gate dielectrics, silicon dioxide, thin film metrology

INTRODUCTION

As gate dielectric film thicknesses shrink along with other transistor dimensions, process tolerances for film thickness and the resulting demands on measurements have become truly challenging, with 3-σ process tolerance already below 0.1 nm and measurement requirements below 0.01 nm. Ellipsometry continues to be the measurement of choice for in-line monitoring of film thickness because it is rapid and highly precise, although other measurements may also be needed for added film information. Film thickness values obtained from ellipsometry depend on an assumed film structure model, as well as on the optical index values assumed for the silicon substrate and the silicon dioxide film. The resulting thicknesses, therefore, are not absolute, although they can be very precise for a fixed set of assumptions. It is believed that most companies develop a "translation table" to relate ellipsometry-based film thicknesses in terms of how "thick" they are electrically, e.g. as a capacitor dielectric, which is the critical because it indicates electrical circuit performance .

It is highly desirable to be able to verify the performance of ellipsometry tools used for gate dielectric process monitoring, such as through the use of Reference Material(s). Unfortunately, it is difficult to generate Reference Materials for very thin films, with thicknesses traceable to SI units, and also with uncertainties for thickness anywhere close to the requirements stated in the ITRS. The procedure used for full analysis of the conceptually accurate interface-layer model, as used for NIST ellipsometry-based oxide thickness Standard Reference Materials from 10 nm to 200 nm, resulted in uncertainties of film thickness, ± 0.5 nm, that would be considered unacceptable for current needs[1].

While SI unit thickness traceability is not truly required for verifying consistency of ellipsometer performance or "tool-matching", it is a significant consideration for Reference Materials that are used internationally, or where ISO requirements become important. This study utilizes a carefully designed set of 2 nm SiO_2 films to determine the relation of film thickness obtained from several simple ellipsometry models with electrical thickness and SI-traceable physical thickness values. It also identifies the major uncertainties from each type of measurement in this study.

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EXPERIMENTAL OVERVIEW

A set of nine, 150 mm diameter wafers, with thermal oxides, grown at 850 °C for 30 min, was used for these studies. These wafers, seven with blanket oxides and two others with arrays of poly-gate capacitors, were from the center of a furnace stack of 30 wafers. The poly-gate capacitors were fabricated in square arrays at four different sizes in each of the four wafer quadrants. They were arranged so that in each of the four wafer quadrants a different one of the capacitor sizes was proximate to the wafers' central sweet-spot (out to a 25 mm radius about wafer center) The capacitors were designed to have active areas of (16, 36, 64 and 100) x 10^{-4} cm^2. The oxides were grown and the capacitors fabricated at NC State University.

All seven blanket-oxide wafers were mapped by ellipsometry immediately after oxide growth. Wafer to wafer center-spot thickness differences for the blanket wafers was within a range of 0.064 nm. The thicknesses at the 50 mm radius corresponding to the location of the capacitors used for TEM analysis were up to 0.11 nm. larger than the center spot thicknesses.

These measurements served to set limits on the thickness differences that might be expected in this study simply because not all measurements could be made in the same region of the same wafers. They did not provide an estimate of thickness differences resulting from the additional thermal cycles and possible polysilicon/SiO_2 interdiffusion during capacitor fabrication.

The wafers were characterized as follows: the blanket wafers were measured at wafer center by single-wavelength ellipsometry (SWE) immediately following a thermal desorption cycle. The two wafers with capacitors were measured by C-V in the wafer sweet spots to extract thicknesses for comparison with the center-point ellipsometry thicknesses of the blanket wafers. Capacitors of the largest size, located at a distance of 45 mm to 50 mm from each wafer's center, were also measured by C-V and one of these capacitors from each wafer was then sectioned and HRTEM and high-angle annular dark field (HAADF) STEM thicknesses were obtained.

ELLIPSOMETRY MEASUREMENT and ANALYSIS

It has been appreciated for some time that surface contamination will accumulate on the surfaces of wafers with time and, if not removed before ellipsometry measurements, will cause an inaccurate value of a layer thickness to be determined because ellipsometry is generally not capable of separately determining the thicknesses of the contamination layer and the film being investigated. For this study, we chose to remove the contamination by thermal desorption, 300 °C for 5 min on a hot plate, followed by 90 s cooling on a massive copper heat sink, immediately prior to measurement. Ellipsometric measurements were taken at 5 min intervals for one hour; SWE was chosen so that each measurement was fast enough to be considered a snapshot, and did not average over a period of contamination redeposition. After analysis by each of several models, the resulting thicknesses were fitted to a straight line vs. time following removal from the hot plate, and extrapolated to time equals zero to estimate the oxide thickness before any recontamination started.

Three basic models were used to analyze the ellipsometry measurements. *The first*, known to be overly simple, was used because it was expected to give the highest precision and thus serve as a base-line. The model treated the entire SiO_2 film as having a known and constant index of refraction, n, of 1.461, as used for the stoichiometric part of the oxide of previous NIST SRMs for SiO_2 (1). *The second model* assumed a transition, or interlayer, between the silicon substrate and the SiO_2. The interlayer, is a suboxide of silicon that contains the bridging bonding arrangements between the crystalline silicon substrate and the stoichiometric amorphous SiO_2 [2]. This model was employed for analysis of the previous NIST SiO_2 SRMs which were thick enough to allow an estimate to be made of the interlayer parameters. Because the interlayer parameters cannot be determined directly from the very thin oxides in this study, the values for the previous SRMs: thickness = 0.7 nm and refractive index, n = 2.8, were used here, as were a number of other

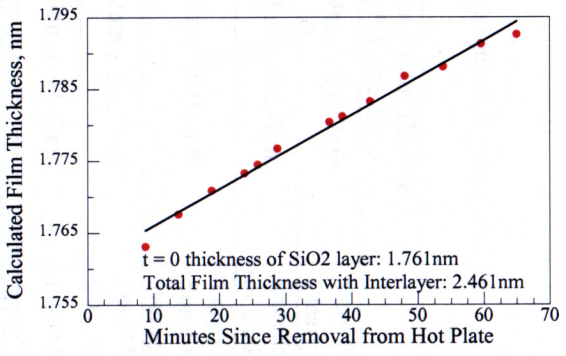

FIGURE 1. SWE results: Interface layer model - with a 0.7nm, index = 2.8 interlayer.

combinations with slightly higher and lower thickness and index values. *The third model* considered the SiO_2 index to be constant, but with a value higher than 1.461 to account for the added optical path length arising from the higher index interlayer[3]. This model was implemented in two ways: 1) allowing the analysis software to find an individual best-fit thickness-index pair for each of the measurements during the one-hour

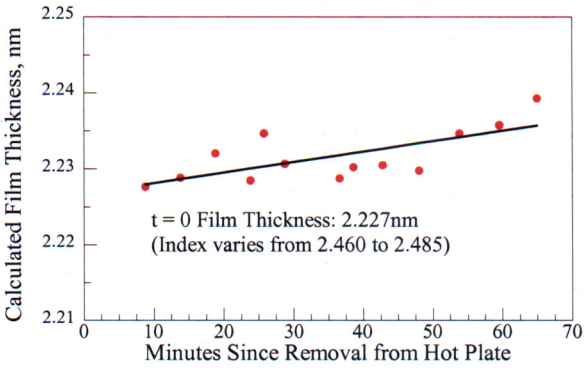

FIGURE 2. SWE results: Single layer model - fit on thickness and index at each point.

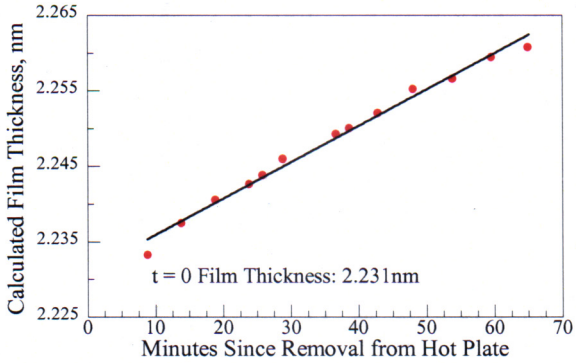

FIGURE 3. SWE results: Single layer model - index fixed at 2.49 – near the pt. by pt. average.

period, 2) searching for a single index value, comparable to the point-by-point values, that provided low residual fitting errors simultaneously for all measurements on a given wafer. While all procedures but the one that fitted the thickness and index separately at each point (Fig. 2) showed a smooth linear trend for film regrowth, as expected, the goodness of fit parameter reported by the fitting algorithms were not always satisfactory. Table 1 summarizes the assessment of results from each of the models used for fitting the ellipsometry data.

CAPACITANCE-VOLTAGE

The C-V measurements were taken at 100 kHz, the highest frequency that did not show roll-off in accumulation due to series resistance. The measurements were taken in steps of 0.05 V from –2.6 V to 2.6 V on 9 capacitors of each size from the sweet spots of both wafers, and also on 9 of the extra large capacitors at a distance of about 50 mm from the centers of the 2 wafers. For each of the capacitor sizes, the capacitance values, in accumulation, of the 2 wafers were well within 1 % of each other; slightly larger differences were found in depletion due to substrate resistivity differences. For the largest size, (XL), capacitors at the 50 mm radius used for TEM measurements, the two wafers had equivalent (within 1%), accumulation capacitance values, but for both wafers the capacitance at 50 mm was about 2.5 % less than at 25 mm suggesting slightly thicker oxide at 50 mm.

TABLE 1. A summary of the results from Single Wavelength Ellipsometry Analyses.

Model	7 wafer Total Film Thickness Avg.* & Std. Dev.	Goodness of Fit to Data and Comments
Single Stoichiometric SiO_2 Layer: SiO_2 Index = 1.461	2.409nm ± 0.012nm	Very Poor- Clearly an inappropriate model
Single SiO_2 Layer: Point-by-point fit on Index & Thickness	2.234nm ± 0.037nm	Excellent, but erratic time trend to thickness values for each wafer
Single SiO2 Layer; Set SiO_2 Index at 2.49 (pt. by pt. average)	2.211nm ± 0.032nm	Very Good Some wafer to wafer variability in average index values
0.7nm, n = 2.8 Interface Layer under Stoichiometric SiO_2	2.472nm ± 0.012nm	Poor** Conceptually correct model
0.7nm, n = 3.2 Interface Layer under Stoichiometric SiO_2	2.659nm ± 0.017nm	Poor**

*A change of assumed angle of incidence of 0.004 deg. (our uncertainty limit) causes thickness changes < 0.004nm; a change of silicon substrate refractive index within range of published values causes thickness change < 0.005nm

** Only use of an angle of incidence well outside the uncertainty limit gave good values for the "goodness of fit" to data with any reasonable variant of the interlayer model

The nine-capacitor average capacitance vs. voltage was calculated at each size for each of the wafers; the averages were calculated separately for the XL capacitors at 25 mm and 50 mm radius. Capacitor areas were obtained for all sizes by using both photographic blow-ups, and a microscope filar eyepiece. To eliminate the effect of field oxide overlap capacitance, a linear regression was done of average capacitance vs. area for each wafer's sweet spot capacitors. This was done separately at each bias voltage used for C-V measurement; correlation coefficients from the regressions exceeded 0.999 for all voltages. The result of the regressions vs. bias voltage was a reconstructed capacitance/unit area C-V curve applicable to the sweet spot capacitors of each wafer, and a capacitance, C_o (V), at zero area, attributed to overlap capacitance. The C_o (V) values were subtracted from the capacitance values at each voltage for the XL capacitors at 50 mm radius.

Oxide layer thicknesses were extracted from the C-V data by using three different quantum mechanical (QM) simulators which account for quantized states in the substrate and depletion in the poly-silicon electrode[4, 5, 6]. Results are summarized in Table 2. Differences in thickness among the QM simulators are expected from previous work[7].

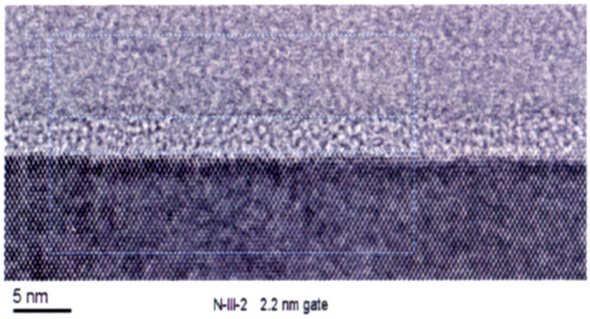

FIGURE 4. HRTEM image of a capacitor section on wafer N-III-2. Thin lines show the electronically generated measurement box used to determine the value of the oxide thickness (central band in photograph)

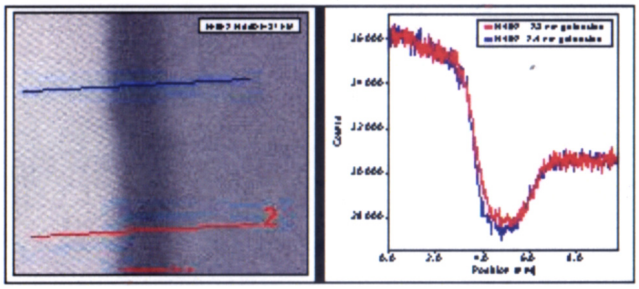

FIGURE 5. Two HAADF-STEM traces from capacitor section used for HRTEM images on wafer N-III-2. The two separate scan traces differed by 0.1 nm in thickness.

Table 2. A summary of the results from C-V analysis by three Quantum-Mechanical Algorithms: Calculated thickness and uncertainty due to two different procedures for capacitor area.

	Sweet Spot Ellipsometry Region			50 mm Radius HRTEM/STEM area		
Wafer / Algorithm	N-III-1	N-III-2	2 wafer average	N-III-1	N-III-2	2 wafer average
IBM Tqm_v6	2.165 ± 0.079 nm	2.169 ± 0.081 nm	2.167 ± 0.080 nm	2.188 ± 0.115 nm	2.191 ± 0.112 nm	2.190 ± 0.114 nm
NIST C-V	2.140 ± 0.078 nm	2.140 ± 0.078 nm	2.140 ± 0.078 nm	2.162 ± 0.113 nm	2.162 ± 0.113 nm	2.162 ± 0.113 nm
NCSU-CVC	2.376 ± 0.087 nm	2.379 ± 0.086 nm	2.377 ± 0.087 nm	2.401 ± 0.126 nm	2.404 ± 0.124 nm	2.403 ± 0.125 nm

HRTEM and HAADF STEM

One extra large capacitor at approximately 50 mm radius was sectioned from each wafer with final thinning performed using 3.5 kV Ar+. The sections were characterized in an FEI Co. TECNAI™ F30 TEM at International SEMATECH (ISMT). The samples were aligned with the electron beam parallel to z = [110] direction of the substrate silicon. HRTEM and HAADF-STEM results were obtained from each of the wafers with results exemplified in Figs. 4 and 5 and summarized in Table 3. There was a wafer to wafer thickness difference found with both of the TEM methods, and also a method to method difference found for both wafers. The wafer to wafer difference is not seen in the C-V results for capacitors from the same regions as the TEM data. The TEM differences are believed to be due to the effects of interface roughness on the localized sampling of the TEM measurements.

TABLE 3. A summary of HRTEM and HAADF-STEM thickness results: Measured vale and estimated absolute-uncertainty.

	HRTEM	HAADF-STEM
Wafer N-III-1	2.4 nm ± 0.2 nm	2.5 nm ± 0.15 nm
Wafer N-III-2	2.2 nm ± 0.2 nm	2.3 nm ± 0.15 nm

COMPARISON of MEASUREMENTS and DISCUSSION

The results from the three types of measurements in this study are summarized in Figs. 6 and 7 which group the results according to the region of the wafers used for the measurements. The measurement uncertainties shown are not comprehensive, but represent the major contributions for each of the methods in this study.

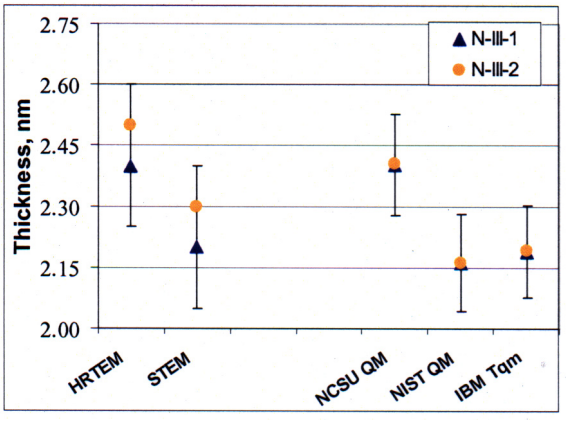

FIGURE 6. Thickness values and uncertainties from TEM and C-V measurements on two wafers.

They represent different considerations for the three types of measurements and are based, at least in part, on the amount, and kind, of replicate measurements for the three techniques.

The original wafer screening by ellipsometry indicated wafer to wafer oxide thickness differences should be less than 0.035 nm for all wafers in this study; the C-V results for the 2 capacitor wafers are even tighter, although that tightness is masked somewhat by assumptions made dealing with the capacitor area data from the two procedures used. On-wafer radial nonuniformity between wafer center and the region used for HRTEM was expected to be less than 0.11 nm from the ellipsometry screening of all blanket oxide wafers, and no more than 0.05 nm different from the sweet-spot area (~ 25 mm radius) by capacitor measurement.

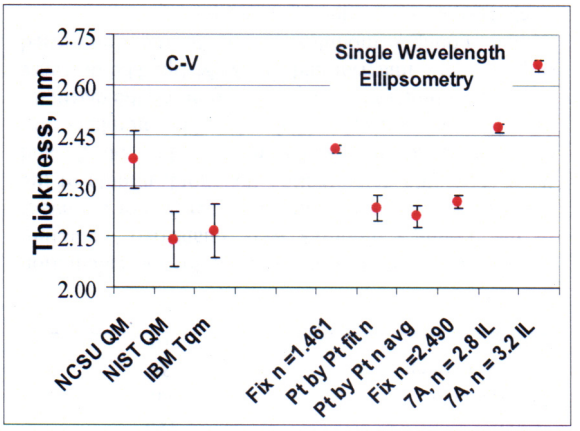

FIGURE 7. Thicknesses within wafer sweet Spots: Averages and standard deviations as follows - C-V (2 wafers); SWE (7 wafers).

For the ellipsometry measurements, the error bars for each of the models evaluated represent the 7 wafer standard deviations of the time = 0 thickness values; additional uncertainty due to angle of incidence and other instrumental effects adds an estimated ± 0.007 nm. Ellipsometry results yield a range of values with simple models that are within the uncertainties of both C-V and TEM results. All models except the "point-by-point fit of index" give a smooth linear description of wafer recontamination with time; however, only the use of an effective fixed index of refraction value near the "point-by-point" average gave both a smooth linear description and a very good fit to the measured ellipsometry parameters, Δ and Ψ. All the models used, even the interlayer model, are simplifications of the real film structure. As film thickness becomes very small, the ability to fit the measurement data well is highly dependent on using the correct model or else finding an optimal simplification such as the effective fixed index in Fig. 3.

For the C-V measurements, the largest internal uncertainty is due to the difference in capacitor area measurements resulting from the photo and filar eyepiece methods used; the availability of a CD SEM would have improved dimensional accuracy. Variability of results among the capacitors of a given size was much smaller than the uncertainty due to absolute area. The dominant overall factor in the C-V analyses is the effect of the QM correction algorithm used, see Fig. 6. It is not yet known which of the available QM simulators is the closest to being accurate.

The uncertainty error bars shown for HRTEM and HAADF-STEM, Fig. 6. are estimates of absolute uncertainty for the basic measurements. The use of a TEM with a spherical aberration correction would have reduced the uncertainty for the HRTEM measurements.

An extended discussion of HRTEM and STEM analysis of thin dielectric films is not possible here; the reader is referred to reference 8.

The spread in ellipsometry and C-V thickness values are principally dependent on models used to analyze the data, with only minor dependence on sample uniformity concerns. The spread in TEM results is dominated by sample layer interface nonuniformity that is not the same for both wafers in the regions sampled by the TEM foils. The core uncertainties of the TEM results relative to absolute thickness values, 0.2 nm for HRTEM and 0.15 nm for HAADF-STEM, listed in Table 3 are the principal limit to obtaining SI length unit traceability for thickness values even if sample uniformity and interface abruptness problems are eliminated.

CONCLUSIONS

The sample set design was found to be an effective way to provide information on material nonuniformity concerns related to the fact that it is not possible to perform all 3 measurements on the same wafer spot. However, comparison of thickness measuring techniques requiring both blanket and capped-oxide wafers requires still better wafer-to-wafer and on-wafer radial uniformity of thickness, and particularly, less interface roughness.

The results obtained indicate that it should be possible to select an effective ellipsometry analysis model for developing Reference Materials in good agreement with "centerline" TEM and/or electrical thickness scales. This would be subject to improving sample uniformity to enable tightening of TEM results and assist resolution of the best QM algorithm for analysis of C-V measurements.

However, it does not yet appear possible to develop thin oxide film reference materials with uncertainties in the sub 0.01 nm range, i.e. consonant with ITRS tool precision requirements, when accuracy considerations (traceability to the SI unit for length) are factored in. The principle limitation in this case is the core uncertainty of TEM thickness values as shown in Table 3.

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* Certain commercial products are identified here to adequately specify the experimental procedure. Such identification does not imply recommendation or endoresment by NIST nor does it imply that the equipment is necessarily the best available for the purpose.

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