Silicon Carbide Power MOSFET Model and Parameter Extraction Sequence

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Abstract— A compact circuit simulator model is used to describe the performance of a 2 kV, 5 A 4-H silicon carbide (SiC) power DiMOSFET and to perform a detailed comparison with the performance of a widely used 400 V, 5 A silicon (Si) power MOSFET. The model's channel current expressions are unique in that they include the channel regions at the corners of the square or hexagonal cells that turn on at lower gate voltages and the enhanced linear region transconductance due to diffusion in the nonuniformly doped channel. It is shown that the model accurately describes the static and dynamic performance of both the Si and SiC devices and that the diffusion-enhanced channel conductance is essential to describe the SiC DiMOSFET on-state characteristics. The detailed device comparisons reveal that both the on-state performance and switching performance at 25 °C are similar between the 400 V Si and 2 kV SiC MOSFETs, with the exception that the SiC device requires twice the gate drive voltage. The main difference between the devices is that the SiC has a five times higher voltage rating. At higher temperatures (above 100 °C), the Si device has a severe reduction in conduction capability, whereas the SiC on-resistance is only minimally affected.

NOMENCLATURE

A	Device active area (cm^2)
A_{ds}	Drain-body junction area (cm^2)
A_{gd}	Gate-drain overlap area (cm^2)
C_{dsj}	Drain-source junction capacitance (F)
C_{gd}	Gate-drain capacitance (F)
C_{gi}	Gate-inversion layer capacitance (F)
C_{gdj}	Gate-drain junction capacitance (F)
C_{gs}	Gate-source capacitance (F)
C_{oxd}	Gate-drain overlap oxide capacitance (F)
dV_{Tl}	Low current threshold voltage differential (V)
ε_{semi}	Semiconductor dielectric constant (F/cm)
F_{xjbe}	Fraction depletion charge at gate-drain overlap edge
F_{xjbm}	Fraction depletion charge at gate-drain overlap middle
I_{mos}	MOSFET channel current (A)
I_{mosl}	Low current region component of I_{mos} (A)
I_{mosh}	High current region component of I_{mos} (A)
k	Boltzmann's constant (J/K)
K_f	Linear region transconductance factor
K_{fl}	Low current region transconductance factor
K_p	Saturation region transconductance (A/V^2)
K_{psat}	Extracted saturation region transconductance (K_p), (A/V^2)
K_{plin}	Extracted linear region transconductance (K_fK_p), (A/V^2)
μ_n	Bulk electron mobility ($cm^2/V{\cdot}s$)
N_b	Base dopant density (cm^{-3})
n_i	Intrinsic carrier concentration (cm^{-3})
P_{vf}	Pinch-off voltage factor
q	Fundamental electronic charge (C)
R_b	Epitaxial layer resistance (Ω)
R_s	Series drain resistance (Ω)
T	Chip surface temperature (K)
θ	Transverse electric field parameter (V^{-1})
V_{bi}	Built-in junction potential (V)
V_{bigd}	Built-in potential of gate-drain overlap region (V)
V_{dds}	Drain-source terminal voltage (V)
V_{ds}	MOSFET channel voltage (V)
V_{gs}	Gate-source voltage (V)
V_{Td}	Gate-drain overlap depletion threshold (V)
V_{Tdi}	Gate drain overlap inversion threshold voltage (V)
$V_{Tdiedge}$	V_{Tdi} at body edge of gate-drain overlap (V)
V_{Tl}	Low current MOSFET channel threshold voltage (V)
V_{Th}	High current MOSFET channel threshold voltage (V)
W	Quasineutral drift region width (cm)
W_b	Metallurgical drift region width (cm)
W_{dsj}	Drain-body depletion width (cm)
y	Pinch-off voltage exponent

I. INTRODUCTION

Recently, silicon carbide (SiC) power devices have begun to emerge with performance that is superior to that of silicon (Si) power devices. For a given blocking voltage, SiC minority carrier conductivity modulated devices, such as a

PiN diode, are expected to show an improvement in switching speed by a factor of 100 as compared to Si, while majority carrier SiC devices are expected to show a factor of 100 advantage in resistance compared to Si [1]. Prototype devices have already demonstrated improvements over Si technology for devices of various current and voltage ratings, and SiC Schottky diodes have been made commercially available.

In order for circuit designers to fully utilize the advantages of the new SiC power device technologies, compact models are needed in circuit and system simulation tools. In [2] a compact SiC power diode model for use in the Saber® circuit simulator [3] was described and an extraction sequence for this model was developed in [4]. The comprehensive SiC diode model is capable of accurately describing the static, dynamic, and electrothermal performance of SiC Schottky, Junction-Barrier Schottky, and PiN diodes. It is anticipated that SiC power device models with extracted parameter sets will be provided in circuit simulator libraries and will be used to provide insight into the performance advantages of SiC power diodes.

The purpose of this paper is to develop a new model and parameter extraction sequence for SiC power MOSFETs. The model is used to describe the performance of a 2 kV, 5 A 4H-SiC Double implanted MOSFET (DiMOSFET) and to perform a detailed comparison with the performance of a widely used 400 V, 5 A Si Vertical Double-Diffused power MOSFET (VDMOSFET). The model is based upon the latest version of the power MOSFET model utilized in the Hefner IGBT model [5], where the parameters of both the Si and SiC MOSFETs can be extracted using the IGBT Model Parameter ExtrACtion Tools (IMPACT) software [6]. Both the model and extraction tools are enhanced and extended for the purpose of this work to include the temperature dependent material properties of SiC materials as well as the additional device physics required to describe the DiMOSFET structure.

II. Silicon Carbide DiMOSFET

SiC power MOSFETs are expected to have advantages over existing Si technology similar to that of the above mentioned SiC diodes. With a high critical electric field (~ 2 MV/cm), reasonable bulk electron mobility (~ 800 $cm^2/V{\cdot}s$), and high saturation velocity (~ $2{\cdot}10^7$ cm/s) [7,8], 4H-SiC is attractive for implementation of high voltage, high-speed power devices. These physical properties are suitable for making high performance 4H-SiC unipolar devices capable of blocking 1 kV – 3 kV. For the same range of blocking voltages, typical silicon power devices utilize conductivity modulation in the drift layer to reduce the forward drop, resulting in reduced switching speeds.

Fig. 1 shows the simplified cross section of the unit cell structure of a recently introduced 2 kV, 5 A SiC DiMOSFET that has fast switching performance [9]. The structure of the DiMOSFET is similar to that of the VDMOSFET used for Si power MOSFETs, in that the p-well and n^+ source regions typical of the VDMOSFET structure still exist in the

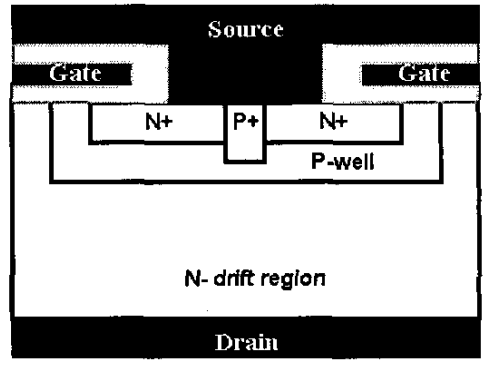

Fig. 1. Cell structure for a 5 A, 2 kV SiC DiMOSFET.

DiMOSFET structure. The main difference between the two structures is that the DiMOSFET p-well and n^+ source regions are much more shallow than those of a Si VDMOSFET due to the much lower impurity diffusion coefficients inherent in SiC.

For the fabricated devices shown in Fig. 1, the MOSFET channel length is 1.5 μm and is defined by the p-well and n^+ implants. The cell pitch is 16 μm, and the packing density of the gate periphery is 1250 cm/cm^2. A $2.5 \cdot 10^{15}$ cm^{-3} doped, 20 μm thick n-type drift layer is used in the device. In the on-state region of operation, electrons flow laterally from the n^+ source through the MOSFET channel formed in the implanted p-well and then vertically between adjacent cells and through the lightly-doped drift layer to the drain contact. For a 2 kV Si MOSFET, the drift layer resistance dominates the on-resistance of the device, whereas the specific on-resistance is dominated by the channel resistance for the SiC DiMOSFET structure [9].

The fabrication of the DiMOSFET begins with an n-type SiC wafer with a $2.5 \cdot 10^{15}$ cm^{-3} doped, 20 μm thick epitaxial layer. The p-wells are formed by aluminum implantation followed by a heavy-dose nitrogen implant for the n^+ source regions. A heavy-dose of aluminum is implanted to form the p^+ contacts to the p-wells, in addition to the floating guard rings that terminate the edges. All implants are performed at 1600 °C in Ar. A 2 μm oxide layer is deposited and patterned to serve as the field oxide, which is followed by gate oxidation. A 500 Å thick gate oxide is thermally grown at 1200 °C in dry O_2, then annealed in NO at 1175 °C for 2 hours, as described in [10]. Next, a 0.25 μm molybdenum layer is sputtered and patterned for the gate metal. The contacts to the source, drain, and p^+ regions are formed with alloyed Ni. The gate is then metallized with a 0.25 μm thick Ni/Au layer to reduce the gate resistance. A Plasma-Enhanced Chemical Vapor Deposition (PECVD) oxide layer is then deposited as an inter-metallic dielectric, and via holes are opened for the contacts. Finally, a 2 μm thick Ti/Pt/Au layer is deposited using e-beam evaporation and then lifted-off as the final metal layer.

TABLE I. POWER MOSFET EQUATIONS

MOSFET Channel Currents

$$I_{mos} = I_{mosh} + I_{mosl}$$

$$V_{Th} = V_T + \frac{K_{fl}}{1-K_{fl}} dV_{Tl}$$

$$V_{Tl} = V_T - dV_{Tl}$$

Linear Region:

$$y = \frac{K_f}{K_f - \frac{P_{vf}}{2}}$$

$$I_{mosl} = \frac{K_{fl} K_f K_p \left[(V_{gs} - V_{Tl}) V_{ds} - P_{vf}^{\,y-1} V_{ds}^{y} (V_{gs} - V_{Tl})^{2-y} \right]}{(1 + \theta(V_{gs} - V_{Tl}))}$$

$$\text{for} \quad V_{ds} \le \frac{V_{gs} - V_{tl}}{P_{vf}}$$

$$I_{mosh} = \frac{(1-K_{fl}) K_f K_p \left[(V_{gs} - V_{Th}) V_{ds} - P_{vf}^{\,y-1} V_{ds}^{y} (V_{gs} - V_{Th})^{2-y} \right]}{(1 + \theta(V_{gs} - V_{Th}))}$$

$$\text{for} \quad V_{ds} \le \frac{V_{gs} - V_{th}}{P_{vf}}$$

Saturation Region:

$$I_{mosl} = \frac{K_{fl} K_p (V_{gs} - V_{Tl})^2}{2(1 + \theta(V_{gs} - V_{Tl}))} \qquad \text{for } V_{ds} > \frac{V_{gs} - V_{tl}}{P_{vf}}$$

$$I_{mosh} = \frac{(1-K_{fl}) K_p (V_{gs} - V_{Th})^2}{2(1 + \theta(V_{gs} - V_{Th}))} \qquad \text{for } V_{ds} > \frac{V_{gs} - V_{th}}{P_{vf}}$$

On-State Equations

$$V_{dds} = V_{ds} + I_d (R_b + R_s)$$

$$R_b = \frac{W}{qAN_b\mu_n} \qquad \text{where} \qquad W = W_b - W_{dsj}$$

$$\mu_n(T) = \frac{947}{1 + \left(\frac{N_b}{1.94 \cdot 10^{17}} \right)^{0.61}} \cdot \left(\frac{T}{300K} \right)^{-2.15}$$

Transient Equations

$$W_{dsj} = \sqrt{\frac{2\varepsilon_{semi}(V_{ds} + V_{bi})}{qN_b}}$$

$$C_{dsj} = A_{ds}\varepsilon_{semi}/W_{dsj} \quad \text{where} \quad A_{ds} = A - A_{gd}$$

$$W_{gdj} = \sqrt{\frac{2\varepsilon_{semi}(V_{dg} + V_{Td})}{qN_b}}$$

$$C_{gdj} = A_{gd}\varepsilon_{semi}/W_{gdj}$$

$$C_{gd} = \begin{cases} C_{oxd} & \text{for } V_{ds} \le V_{gs} - V_{Td} \\ C_{oxd} C_{gdj} / (C_{oxd} + C_{gdj}) & V_{ds} > V_{gs} - V_{Td} \end{cases}$$

$$C_{gi} = \begin{cases} C_{oxd} & \text{for } V_{gs} \le V_{Tdi} \\ C_{oxd} \left(\frac{V_{gs} - V_{Tdiedge}}{V_{Tdi} - V_{Tdiedge}} \right) & V_{gs} < V_{Tdiedge} \;\&\; V_{Tdiedge} > V_{Tdi} \end{cases}$$

$$V_{Tdi} = V_{Td} - V_{bigd} - \frac{F_{xjbm} A_{gd}}{C_{oxd}} \sqrt{2\varepsilon_{semi} q N_b (V_{bigd} + V_{ds})}$$

$$V_{Tdiedge} = V_{Td} - V_{bigd} - \frac{F_{xjbe} A_{gd}}{C_{oxd}} \sqrt{2\varepsilon_{semi} q N_b (V_{bigd} + V_{ds})}$$

III. POWER MOSFET MODEL DESCRIPTION

The model used in this work is based upon the latest version of the power MOSFET formulation utilized in the Hefner IGBT model [5]. The model has been enhanced by adding the temperature dependent material properties of 3C-, 4H-, and 6H-SiC, which can be selected using the material type parameter switch. The model contains features that have been shown to be important to describe the dynamic performance of vertical power MOSFETs including the two-phase nonlinear gate-drain overlap capacitance, negative gate voltage inversion of the gate-drain overlap, and nonlinear body-drain depletion capacitance. The MOSFET channel current expressions used in the model are unique in that they include: (1) the channel regions at the corners of the square or hexagonal cells that turn on at lower gate voltages and (2) the enhanced linear region transconductance due to diffusion in the nonuniformly doped channel. The enhanced linear region transconductance is particularly important for the SiC power MOSFET as described in the results section below.

A. On-State Model Characteristics

Table I gives the basic equations used in the model. The left-hand side of Table I gives the MOSFET channel current-related equations, and the right-hand side gives the on-state voltage and transient-related equations. The MOSFET channel current I_{mos} is composed of two MOSFET channels in parallel; one that dominates in the very low current region, I_{mosl}, due to conduction at the corners of the MOSFET cells and another that dominates in the high current region, I_{mosh}, due to the main portion of the MOSFET cells. The corner regions have a lower threshold voltage and transconductance

than the main channel resulting in a "soft threshold" effect. Therefore, it is necessary to assign each region a unique threshold voltage, V_{Tl} and V_{Th}, and transconductance factor K_{fl} and (1- K_{fl}), through the use of the additional parameters K_{fl} and dV_{Tl}. The expressions for V_{Tl} and V_{Th} are formulated to simplify parameter extraction and to allow the model to reduce to the same parameter set in the high current region with or without the soft threshold effect.

The linear region expressions for I_{mosl} and I_{mosh} include the effect of carrier diffusion in the channel due to nonuniform channel dopant density. This effect yields different values for the linear region and saturation region transconductance parameters. The model incorporates this effect using a saturation region transconductance parameter K_p and a linear region transconductance factor K_f, where K_f is the ratio of the linear region transconductance parameter to the saturation region transconductance parameter. The transition between the saturation and linear region or "pinch-off region" is further refined by the pinch-off voltage parameter P_{vf}. The expressions for I_{mos} and y in the linear region are formulated such that the current and its first derivative are continuous at the pinch-off voltage. Both the linear and saturation region expressions include the reduction in channel mobility due to the high transverse electric field for high gate voltages through the parameter θ.

The drain-source terminal voltage V_{dds} consists primarily of the voltage across the MOSFET channel V_{ds}, the voltage across the epitaxial layer resistance R_b, and the voltage across the source series contact resistance R_s. The main advantage of the SiC MOSFET compared to the Si MOSFET is that the value of R_b is reduced because a larger value of N_b and a smaller value of W_b can be used for a given device blocking voltage rating. The temperature dependence of SiC bulk mobility $\mu_n(T)$ has been studied extensively by others [11] and is important in determining the on-state voltage. The bulk

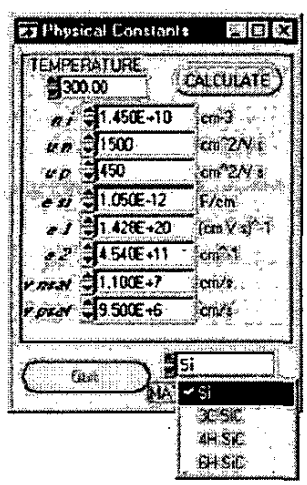

Fig. 2. Temperature dependent material parameters for 4H-, 6H-, and 3C-SiC added to IMPACT extraction tools.

mobility varies with the SiC polytype and is given in Table I for 4-H SiC. This is one of the material properties that is selected using the material type parameter switch in the model.

B. Transient Model Characteristics

The transient characteristics of the model are described by the depletion and oxide capacitance equations in Table I, in addition to the constant gate-source capacitance C_{gs} due to the gate-source overlap and gate metallization capacitance. The drain-source junction capacitance C_{dsj} is determined by the drain-body depletion width W_{dsj} and the area of the drain-body junction A_{ds}. The depletion capacitance depends on the value of the drift region dopant density N_b and the built-in potential of the junction V_{bi}. The built-in potential is a function of the temperature dependent intrinsic carrier concentration n_i for the material.

The gate-drain capacitance C_{gd} has a depletion capacitance component that depends on the gate-drain overlap area A_{gd} and the gate-drain overlap depletion threshold V_{Td}. For drain-gate voltages (V_{ds} –V_{gs}) less than –V_{Td}, C_{gd} is equal to the gate-drain overlap oxide capacitance C_{oxd}. For drain-gate voltages greater than –V_{Td}, C_{gd} is equal to the series combination of C_{gdj} and C_{oxd}. For sufficiently negative gate voltages, an inversion layer forms beneath the gate-drain overlap, resulting in a capacitance from the gate to the inversion layer, C_{gi}. Because the gate-drain overlap inversion layer contacts the body region that is shorted to the source contact, the main effect of the inversion capacitance is to increase the gate-source capacitance. For $V_{gs} < V_{Tdiedge}$, an inversion layer begins to form adjacent to the body-drain junction. The inversion layer capacitance increases linearly with increasing negative gate voltage until $V_{gs} < V_{Tdi}$, where the entire area beneath the gate-drain overlap becomes inverted and C_{gi} becomes equal to C_{oxd}. Both $V_{Tdiedge}$ and V_{Tdi} are functions of the neck region built-in potential V_{bigd} that is calculated from the extracted value of the base doping N_b, the gate-drain overlap accumulation threshold voltage V_{Td}, and the fractions of gate-drain depletion charge imaged on the gate from the adjacent body regions both in the center of the neck region F_{xjbm} and at the body edge of the neck region F_{xjbe}.

IV. Parameter Extraction Using IMPACT

Recently, a software package called IGBT Model Parameter ExtrACtion Tools (IMPACT) was introduced to automate laboratory instrument control and parameter determination for IGBTs [6]. To extend IMPACT to be applicable to SiC power MOSFETs, a material type switch was added to select and calculate the temperature dependent properties of the material as shown Fig. 2. For power MOSFETs, the IMPACT package reduces to three programs that extract the power MOSFET model parameters, as shown in Table II. These programs are SATMSR, which measures the saturation current versus gate voltage to extract $K_{psat} \equiv K_p$, V_T, θ, K_{fl}, and dV_{Tl}; LINMSR, which measures the linear

TABLE II. IMPACT PROGRAMS AND EXTRACTION CHARACTERISTICS FOR MOSFET MODEL PARAMETERS

Parameter symbol	Parameter name	Program	Extraction Characteristic
A	Device active area		Chip Size
V_T	Threshold voltage	SATMSR	Saturation current vs. Vgs
$K_p = K_{psat}$	Saturation region transconductance		Saturation current vs. Vgs
θ	Transverse electric field parameter		High saturation current vs. Vgs
K_{fl}	Low current transconductance factor		Low saturation current vs. Vgs
dV_{Tl}	Low current threshold voltage differential		Low saturation current vs. Vgs
$K_{plin} = K_p \cdot K_f$	Linear region transconductance parameter	LINMSR	On-state voltage vs. Vgs
R_s	Drain series resistance		On-state voltage vs. Vgs
N_b	Drift region dopant density		On-state voltage vs. Vgs
C_{gs}	Gate-source capacitance	CAPMSR	Gate charge at low gate voltage
C_{oxd}	Gate-drain overlap oxide capacitance		Gate charge at high gate voltage
A_{gd}	Gate-drain overlap area		Gate-drain charge
V_{Td}	Gate-drain overlap depletion threshold		Gate-drain charge
F_{xjbe}	Gate-drain overlap depletion charge factor at edge		Gate charge vs. Vgs
F_{xjbm}	Gate-drain overlap depletion charge factor at middle		Gate charge vs. Vgs

region on-state voltage versus gate voltage for a constant drain current to extract $K_{plin} \equiv K_p K_f$, R_s, and N_b; and CAPMSR, which measures gate and gate-drain charge characteristics to extract C_{gs}, C_{oxd}, A_{gd}, V_{Td}, F_{xjbm}, and F_{xjbe}. The values of W_b and A are assumed to be known from the device structure. The extraction sequence is performed over an applicable temperature range to extract the temperature coefficients of the model parameters.

A. Saturation Region Parameter Extraction Using SATMSR

Fig. 3 shows the SATMSR front panel. In SATMSR, the saturation current versus gate voltage is used to extract the MOSFET transconductance parameters for the saturation region K_{psat}, the high current region θ, the low current region K_{fl} and dV_{tl}, and the threshold voltage V_T. To perform the extraction, the MOSFET saturation current I_{mos}^{sat} is measured as a function of gate voltage, and the resulting square root of

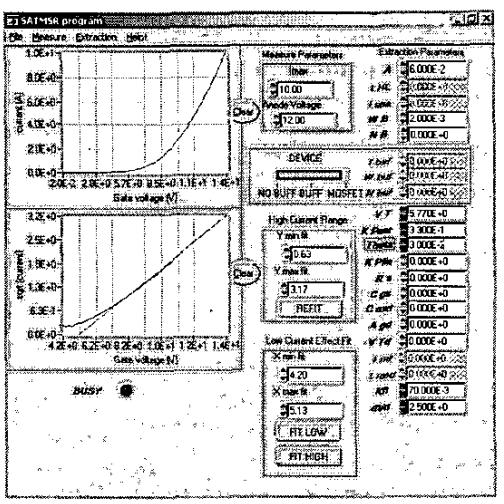

Fig. 3. SATMSR front panel demonstrating extraction of K_p, V_T, θ, K_{fl}, and dV_{Tl}.

I_{mos}^{sat} versus gate voltage is used to extract the model parameters. Commercial programmable semiconductor curve tracers are used to aid in the parameter extraction process. Since these instruments use the collector voltage as the sweep variable and the gate voltage as the step variable, the program uses the gate offset voltage and the cursor readout to generate the continuous graph of current versus gate voltage.

The front panel of the SATMSR program incorporates several pull-down menus that allow the user to perform different measurement functions according to the device characteristics and the curve tracer required for the current range of interest. The panel also allows the user to specify the maximum allowable device current I_{max} during the measurement and the anode voltage of interest V_{anode}. When a measurement is performed using the measure pull-down window, the gate voltage is varied, and the gate voltage and drain current values are transmitted to the computer for analysis.

After a measurement is performed, the user selects the extraction process from the extraction pull-down menu. The first extraction step performs a least squares fit to the simplified model equation

$$\sqrt{I_{mos}^{sat}} = \sqrt{\frac{K_{psat}}{2}}\left(V_{gs} - V_T\right). \qquad (1)$$

The resulting K_{psat} and V_T are displayed on the user interface parameter value list. The user can then extract the high-current parameter θ and refine the extracted value of K_{psat} using the "Refine K_{psat} and θ" button in the extraction pull-down menu. Next, the "Fit Low" and "Fit High" buttons are used to extract K_{fl} and dV_{tl}. These buttons perform a least-squares fit to the saturation region's low- and high- current equations shown in the left-hand column of Table I. The low- and high-current ranges for the fits are estimated by the program but can be adjusted by the user. Fig. 4 demonstrates

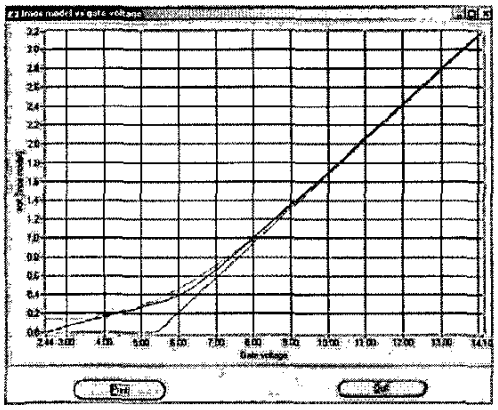

Fig. 4. SATMSR final fit window demonstrating low- and high-current fit.

the final fit of the square-root of the MOSFET saturation current to the saturation region measured data demonstrating the different slope in the high- and low-current regions.

B. Linear Region Parameter Extraction Using LINMSR

Fig. 5 demonstrates the front panel of the LINMSR extraction program. In this program, the linear region on-state voltage versus gate voltage for a constant anode current is used to extract the linear region transconductance K_{plin}, the series resistance R_s, and the base dopant density N_b. These values are calculated from the model equations that are valid for the linear region where the values of the parameters extracted from the previous extraction steps (those from the SATMSR program) are used as known values in the equations.

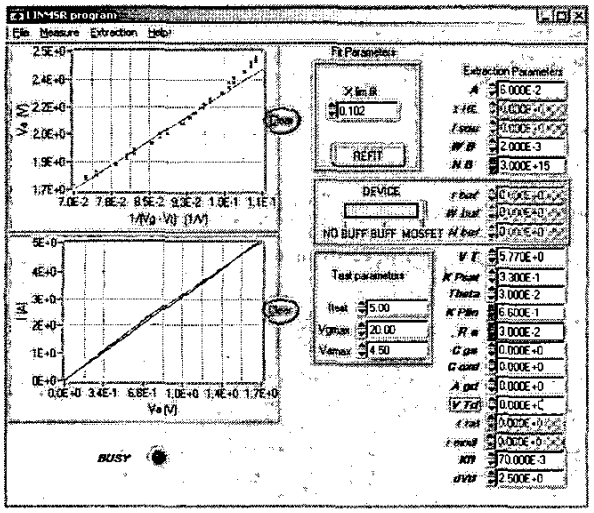

Fig. 5. LINMSR front panel demonstrating extraction of K_p R_s, and N_b.

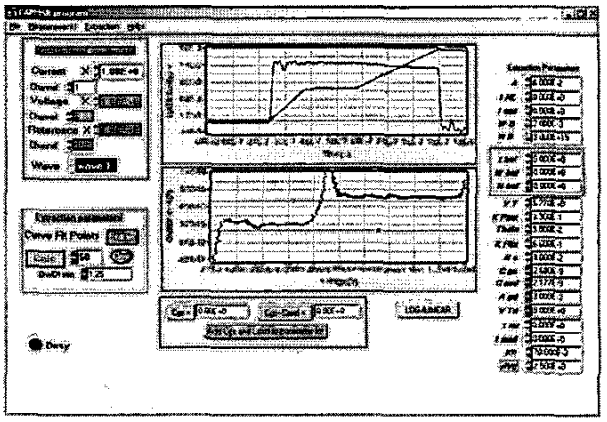

Fig. 6. CAPMSR front panel demonstrating the extraction of C_{gs}, C_{oxd}, A_{gd}, and V_{Td}.

To perform the measurement, the user enters the test current I_T, the maximum gate voltage V_{gmax}, and the maximum anode voltage V_{amax} on the user interface. Since the programmable semiconductor curve tracers apply voltage and measure current, LINMSR uses an iteration algorithm to establish the constant drain test current, which is described in [6]. The iteration results in measuring the on-state drain voltage that results in the selected current for each gate voltage.

After the measurement is performed, the extraction is performed using a least-squares fit to the extraction equation that is valid in the linear region of operation:

$$V_{on} = V_r + \frac{I_T}{K_{plin}\left(V_{gs} - V_T\right)} \tag{2}$$

where

$$V_r = (R_b + R_s)I_d + \frac{I_d\theta}{K_{plin}}. \tag{3}$$

The slope of the linear fit determines K_{plin} and the intercept determines V_r. Using the extracted value of V_r and the parameters extracted from the previous steps, the value of N_b is calculated using the expression for R_b in Table 1. These extracted values are displayed in the list of parameters on the user interface.

C. Gate Charge Characteristics Extraction Using CAPMSR

Fig. 6 demonstrates the front panel for the CAPMSR program. This program uses the gate- and gate-drain charge characteristics to extract the gate-source capacitance C_{gs}, the gate-drain overlap oxide capacitance C_{oxd}, the gate-drain overlap area A_{gd}, and the gate-drain overlap depletion threshold V_{Td} as described in [12]. The program uses the extraction equation

$$C(V)=\frac{I}{dV/dt} \tag{4}$$

to extract the above listed parameters. The user controls the minimum value of dV/dt and the number of derivative points for each calculation. The values of C_{gs} and C_{oxd} are determined from I_g and dV_{gs}/dt during the first and second phase of the gate charge curve respectively. The values of V_{Td} and A_{gd} are determined by I_g and dV_{dg}/dt during the plateau portion of the gate charge curve. Finally, the values of F_{xjbm} and F_{xjbe} are determined by I_g and dV_{gs}/dt for negative gate voltages and different drain voltages.

V. Measured and Simulated Results

In this section, the model presented in Section III is used to describe the performance of a 2 kV, 5 A 4H-SiC Double implanted MOSFET (DiMOSFET) as described in Section II and to perform a detailed comparison with the performance of a widely used 400 V, 5 A Si Vertical Double-Diffused MOSFET (VDMOSFET). To do this, the model parameters are extracted for each device at several temperatures using the extraction sequence described in Section IV. Table III shows the parameters extracted for the Si and SiC MOSFETs at 25 °C.

TABLE III. Model Parameters at 25 °C

Parameter	Si	SiC
A	$0.1\ cm^2$	$0.06\ cm^2$
W_b	$50\ \mu m$	$20\ \mu m$
Nb	$3.1 \cdot 10^{14}\ cm^{-3}$	$3 \cdot 10^{15}\ cm^{-3}$
V_T	$3.4\ V$	$5.77\ V$
K_p	$3.3\ A/V^2$	$0.33\ A/V^2$
θ	0	$0.03\ V^{-1}$
K_f	1.7	2
R_s	$0.02\ \Omega$	$0.03\ \Omega$
Kfl	0	0.07
dV_{fl}	$0\ V$	$2.5\ V$
P_{vf}	0.7	0.95
V_{Td}	$3.4\ V$	$0\ V$
A_{gd}	$0.075\ cm^2$	$0.03\ cm^2$
C_{gs}	$1.114\ nF$	$2.68\ nF$
C_{oxd}	$2.066\ nF$	$2.18\ nF$
V_{bigd}	$0.6\ V$	$2.8\ V$
F_{xjbe}	0.5	0.5
F_{xjbm}	0.75	0.75

A. Steady-State Output Characteristics

Figs. 7 and 8 show the simulated and measured output characteristics for the 2 kV SiC and 400 V Si MOSFETs at 25 °C and 100 °C. The on-state resistance at 25 °C is similar between the Si and SiC MOSFETs, although the SiC device requires twice the gate drive voltage. Comparing the SiC and

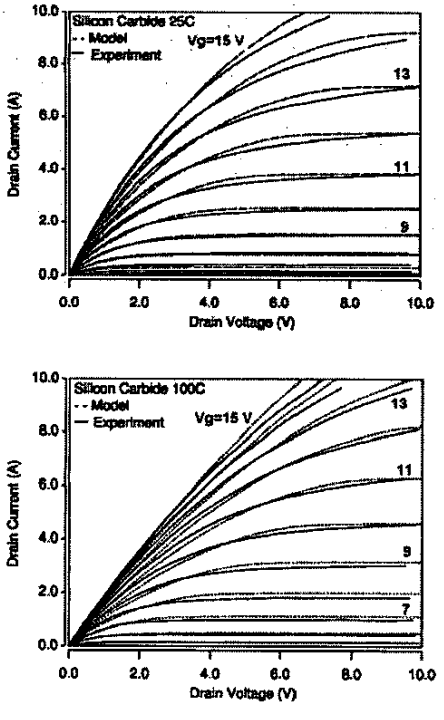

Fig. 7. Silicon carbide MOSFET simulated (dashed) and measured (solid) output characteristics as a function of gate voltage for (a) 25 °C and (b) 100 °C.

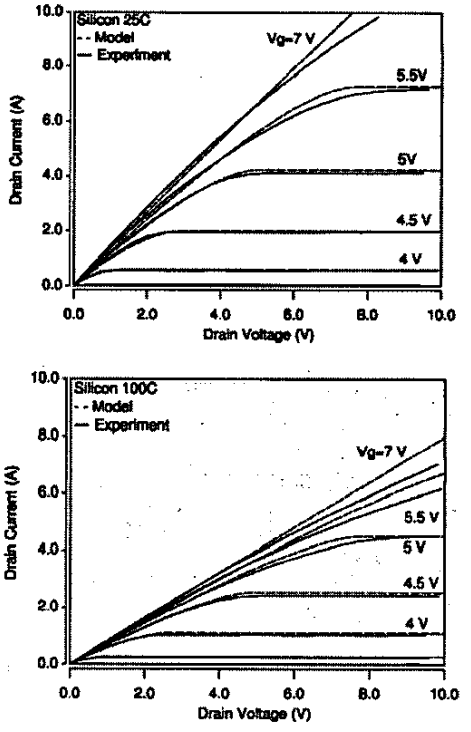

Fig. 8. Silicon MOSFET simulated (dashed) and measured (solid) output characteristics as a function of gate voltage for (a) 25 °C and (b) 100 °C.

Si on-state curves, the Si curves are linear in the on-state region and have a pronounced change in curvature as the saturation or pinch-off region is approached. This occurs because the Si power MOSFET has a large epitaxial layer resistance in series with the MOSFET channel and the channel has a very high transconductance. This causes the Si device to exhibit a resistive-type slope in the linear region prior to pinch-off.

The SiC curves on the other hand, gradually transition from the linear region to the saturation region. In SiC MOSFETs, the epitaxial layer resistance is much smaller and the channel resistance is higher, thus making the MOSFET channel a more significant contributor to the on-state voltage. This is due to the low channel surface mobility of SiC compared to Si. Because the SiC curves have less resistance in series with the MOSFET channel, the enhanced linear region transconductance model of [5] is essential for these devices. Furthermore, because the transconductance is much smaller for SiC, the on-state voltage is closer to the pinch-off voltage, and the model for the transition region is more important.

At 100 °C, the Si device has a severe reduction in conduction capability, whereas the SiC on-resistance is only minimally affected. This occurs because the drift region resistance is a smaller portion of the on-state resistance in the SiC device and because the channel mobility does not decrease with temperature for the SiC device. In the SiC MOSFET, the channel mobility increases with temperature as more interface traps become occupied with the larger concentration of electrons available for conduction, whereas the bulk mobility decreases with temperature as carrier scattering dominates [9]. The resulting effect is an increase in channel conductance K_p and K_f, and an increase in the drift layer series resistance R_b.

B. Transient Switching Waveforms

Figs. 9 and 10 show the Si and SiC MOSFET simulated and measured turn-on waveforms versus gate resistance under resistive load conditions [13]. The simulated test circuit emulates the well-characterized test circuit using a gate driver with a 15 ns rise time to 15 V, a gate inductor L_g = 10 nH, a drain series resistor R_L = 10 Ω, a drain series inductor L_L = 1 nH, and a drain supply voltage of 50 V. The gate resistor R_g was varied to provide different turn-on speeds for the devices.

The turn-on process begins with the driver circuit ramping to 15 V. Gate current immediately begins to flow as the gate capacitances C_{gs} and C_{gd} are charged. Once V_{gs} increases to the threshold voltage V_T, current begins to increase through the drain and the drain voltage begins to fall. As the drain voltage drops, the gate voltage remains relatively constant (plateau region) as the gate current charges the gate-drain capacitance. The charging of the gate-drain capacitance occurs in two phases: in the first phase for high drain voltages, the drain voltage falls more rapidly because C_{gd} is dominated by the depletion capacitance and is relatively small, then in the second phase when V_{gd} becomes less than V_{Td}, the drain voltage falls more slowly because C_{gd} is equal to C_{oxd} and is much larger. As the drain voltage begins to approach the on-state voltage, C_{gd} is not being charged and the gate voltage begins to rise again toward the gate supply voltage as C_{gs} and C_{oxd} are charged.

The turn-on waveforms are similar for the Si and SiC MOSFETs except that the SiC MOSFET requires one-half the gate resistance to achieve the same speed because the gate capacitance parameters are approximately twice as large. The same speed could also be achieved using the same gate resistors but with twice the gate drive voltage for the SiC MOSFET as compared to the Si MOSFET. The ion implantation method used to construct the DiMOSFET results in shallower p-well depths with less resistance between the p-wells. As a result, the gate-drain overlap area A_{gd} in the SiC DiMOSFET can be made much smaller than for the Si VDMOSFET. Furthermore, neck region implants can be avoided, resulting in a reduction in V_{Td}. This results in a lower effective C_{gd}, which increases the speed during the plateau region.

VI. Conclusion

A power MOSFET model applicable to Si and SiC power MOSFETs was presented. Results were shown for a widely used 400 V, 5 A Si power VDMOSFET and a new 2 kV, 5 A SiC power DiMOSFET. The model was validated for the forward conduction and switching characteristics over a wide temperature range. The results demonstrate good agreement between the model and experiment for both technologies. The IMPACT parameter extraction tools were extended to be applicable to the power MOSFET model parameter extraction sequence and the SiC material parameters.

The SiC MOSFET demonstrated similar on-state performance to that of the Si VDMOSFET while having a five times larger blocking voltage and a better ability to maintain forward conduction capability at high temperatures. The switching performance was similar for the Si and SiC devices except that the SiC device required twice the gate drive voltage. The new model provides insights into the SiC MOSFET performance and provides the capability to simulate the performance of the new technology in different circuit applications.

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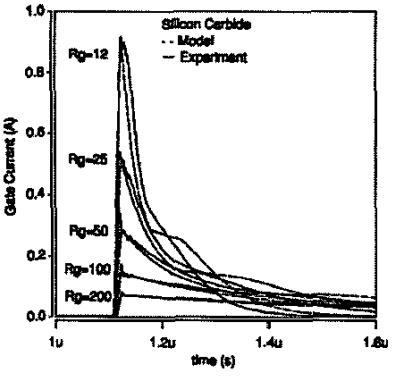
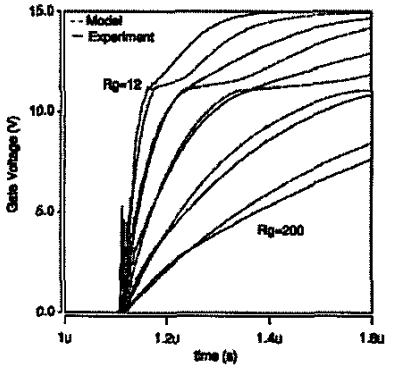
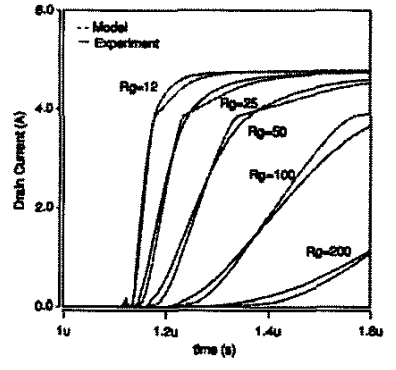






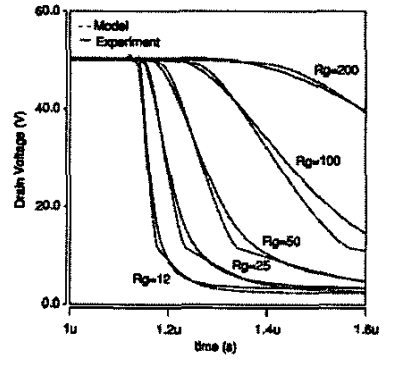
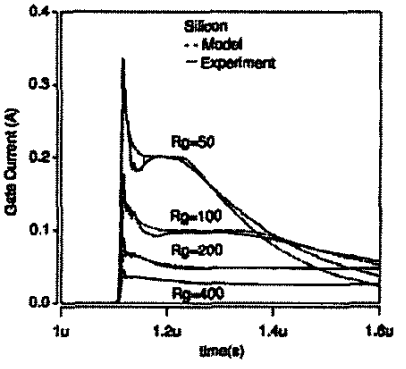
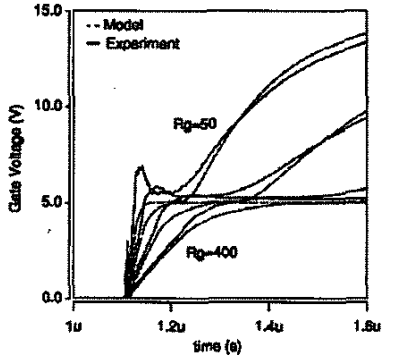
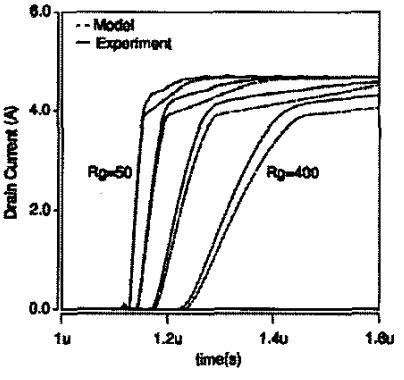


Fig. 9. Silicon carbide MOSFET simulated (dashed) and measured (solid) turn-on waveforms as a function of gate resistance: (a) gate current, (b) gate voltage, (c) drain current, and (d) drain voltage.







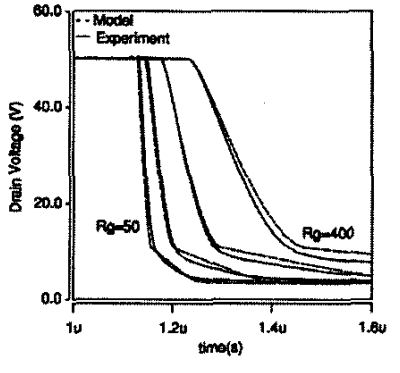


Fig. 10. Silicon MOSFET simulated (dashed) and measured (solid) turn-on waveforms as a function of gate resistance: (a) gate current, (b) gate voltage, (c) drain current, and (d) drain voltage.

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