Dynamic Error Correction of a Digitizer for Time Domain Metrology

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Abstract — A method for numerical correction of distortion in a digitizer used for metrology applications is described. Investigation of the digitizer's error behavior in the phase plane leads to the development of an analytic error model that describes the digitizer's distortion behavior. Of particular significance is the model's ability to describe nonlinear error in the fundamental spectral component manifest as amplitude and frequency-dependent gain and phase error. When fitted only to the harmonic distortion content of the digitizer's output data, the model generates an amount of fundamental that correctly accounts for the error in the digitizer's gain that is not due to linear system response. The model is therefore able to improve not just the total harmonic distortion (THD) performance of the digitizer but its ac rms measurement accuracy as well. At 1 MHz, the model linearizes the digitizer to 70 µV/V over a range of 1 V to 8 V and reduces harmonic distortion by > 20 dB. It is believed that this is the first time that results of this nature have been reported in the literature.

I. INTRODUCTION

Efforts at NIST over the last decade to measure ac rms accurately through waveform sampling have resulted in the development of and reporting on two sampling probes based on latching (sampling) comparators. One of these probes, built around a custom-designed, application specific integrated circuit (ASIC), offers rms measurement capability from dc to 200 MHz with uncertainty less than 0.1 % [1]. The other probe, designed for accurate, low frequency use, measures ac rms from dc to 1 MHz with uncertainty less than 10 µV/V at 100 kHz [2]. Either of these sampling comparator probes when used in conjunction with a NIST-designed wideband sampling voltmeter (WSV) mainframe [3] forms the comparator portion of a successive approximation analog to digital converter (ADC) that samples in equivalent-time. The sampling mainframe provides the reference digital-to-analog converter (DAC) that samples in equivalent-time. The combination of data collection and analysis software, the hardware and software comprise the NIST Sampling Comparator System (SCS).

Phase plane compensation (PPC) is a method for reducing dynamic errors in ADCs. Introduced by Rebold and Irons [4], PPC makes use of a multi-dimensional correction table that stores pre-determined ADC errors indexed by selected parameters of the measured signal. The PPC method and refinements have been reported by numerous researchers [5]-[10]. A notable result of these efforts is the increase in ADC spurious free dynamic range by 10 dB over a bandwidth of 80 MHz [8]. The PPC method described in [8] fits a generic model to an ADC's harmonic distortion content. The model describes an error surface in the phase plane that can be used to compensate the ADC's harmonic distortion behavior.

This paper describes a model-based method for correcting dynamic errors in a digitizer. The approach is similar to that described in [8] but differs in that specific attention is given to the selection of model vectors and their ability to model correctly the fundamental component of the signal spectrum. Previous work with phase plane compensation is thus extended to include compensation for error in the fundamental component that is not part of linear system response, i.e. nonlinear gain error. Results of applying the new method to improve the accuracy of the NIST SCS are reported.

II. MOTIVATION

The principal aim of this work is to use post-sampling signal processing to improve the measurement accuracy of the low frequency probe. Because the low frequency probe has an architecture similar to that of the ASIC probe and because earlier work [11] suggests that the ASIC probe's error behavior can be reasonably described by a phase plane error table, a phase plane compensation approach for correcting dynamic errors in the low frequency probe was chosen for study. It is believed from the outset, however, that a conventional phase plane approach is likely to be insufficient to fully correct dynamic errors in the low frequency probe. The reason will be explained in the subsequent discussion.

III. BACKGROUND

A. Phase Plane Compensation

An error model for correcting ADC dynamic error relates ADC error at any given sample time to a set of signal parameters believed to be associated with the underlying ADC error mechanism(s). A PPC error model is typically implemented as a look-up table that incorporates measurements of an ADC's error behavior as a function of signal state and slope. State and slope are

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chosen as table indices because ADC dynamic errors can result from aperture error that is slew-rate dependent [10].

One way to generate a phase plane look-up table is to exercise an ADC across its working state/slope space with an ensemble of spectrally pure sine wave signals varying in peak amplitude from near zero to full scale. Fig. 1 illustrates the procedure. Table indices span the range of signal state and slope and are discretized into a suitable number of bins. For each data record, a best-fit sine wave is computed either with a least squares sine fitting method [12][13] or the Discrete Fourier Transform (DFT). Errors, e, taken as the difference between the data and the fit, are entered into the table at the state and slope bins corresponding to the signal state and slope at which each error occurs. A given table entry will typically be computed as the average of all errors occurring within a state/slope bin from many different calibration waveforms.

Error sources for which PPC is ineffective are listed in [5]. These error sources include thermal tails, metastability, and decode errors from thermometer code glitches. By design, the low frequency probe has little or no thermal error, and as a successive approximation ADC, it cannot have thermometer code glitches. Although metastability has not been studied, it is believed an unlikely source of dynamic nonlinearity in the probe.

B. The ASIC Probe

The sampling comparator probe built around the ASIC sampling comparator is described in detail in [1]. A simplified schematic diagram of the sampling comparator is shown in Fig. 2. At its heart, the sampling structure consists of six transistors – two for a differential input tracking amplifier, two for a differential regenerative latch, and two for an emitter-coupled current-steering switch to toggle between the tracking and latching stages. This simple circuit structure produces very flat gain over a wide bandwidth, a property required by several NIST measurement applications. The simple structure also results in a simple and smooth error surface in the phase plane. Fig. 3 illustrates the ASIC probe’s error surface over an amplitude range of ±2 V and a slope range of ±1.2 x 10^9 V/s. The error surface was generated using 100 MHz, low-pass filtered sine waves.

C. The Low Frequency Probe

The sampling comparator probe designed for accurate, low frequency use is discussed in detail in [2]. The probe is built with discrete circuit components on a multi-layer printed circuit board. The architecture is similar to that of the ASIC sampling comparator except that an additional front-end tracking stage is included as illustrated in Fig. 2. This stage, consisting of matched JFET transistors, provides a low noise, high input impedance differential input stage with a full scale input range of ±10 V.

Although the low frequency probe’s gain is flat to within 10 µV/V from dc to 100 kHz, over the frequency range of 100 kHz to 1 MHz, the probe’s gain flatness exhibits a dependence on signal amplitude. Fig. 4 plots the probe’s frequency response from 100 kHz to 1 MHz at several different amplitudes measured against a NIST-calibrated thermal transfer standard. Examination of the rms of sine fit residuals indicates that the variation in frequency response over the range of signal amplitudes is not attributable to harmonic distortion. In other words, the
rms of sine fit residuals (which are in quadrature with the fundamental) is too small to account for the observed variation. Therefore, the family of curves in Fig. 4 must be indicative of nonlinear error in the fundamental. We describe this behavior as distortion occurring at the fundamental spectral component, and we adopt the term “first order distortion” to describe this error. Similarly, we use the term "zeroth order distortion” to describe any error in offset that arises from probe nonlinear behavior.

A phase plane error surface for the low frequency probe is shown in Fig. 5. The surface was generated using 1 MHz, low-pass filtered sine waves. The surface is noticeably more complex than that of the ASIC probe. It is also interesting to observe the phase plane error surface for the low frequency probe with the JFET front-end stage bypassed. This error surface is shown in Fig. 6. Here, the error behavior is very similar to that of the ASIC probe. This suggests that, at least with these probes, dynamic errors depend more on comparator architecture than on mode of construction (i.e., integrated circuit versus discrete implementation).

IV. CORRECTION OF IN-PHASE DISTORTION

A problem shared by previous applications of PPC is an inability to measure the degree to which a sampler introduces first order distortion. Because errors recorded in the phase plane look-up table come from the difference between the ADC data and best-fit estimates of the ADC input signal, any error in the sine wave’s fundamental component gets fitted and thereby removed from the error estimate. In addition, an error table indexed only by state and slope is generally not able to accommodate first order nonlinear behavior that varies with frequency. To understand why, consider a group of sine waves at different frequencies but with the same peak amplitude. At the peaks of each waveform, the values of slope are all identically zero. Since the peak amplitudes of each waveform are also identical, data samples at the peaks of each waveform access the same table entries. The table will therefore be effective only if the error behavior at the peaks is identical for each waveform. This will generally not be the case.

V. DISTORTION MODEL

Another strategy for addressing distortion of the fundamental is to use an analytic error model instead of an error look-up table for characterizing the error behavior of the digitizer. The goal of this approach is to construct a model that fits well to the harmonic content of the digitizer and, if possible, also produces the correct amount of fundamental that is in error. Once an appropriate set of basis functions is selected, linear regression is used to fit the harmonic content of the model to the probe's harmonic distortion. The error behavior of the probe is thus written as

\[ e = U \beta \]  

where \( U \) is an \( m \times n \) matrix whose columns are the model basis functions and whose rows correspond to data
samples, and $\beta$ is an $n \times 1$ vector of regression coefficients. $e$ is an $m \times 1$ vector of ADC errors obtained from sine fit residuals or the DFT and therefore contains no fundamental.

Basis functions to describe the error behavior of the low frequency probe are chosen along a line of reasoning as follows: The error surfaces of the ASIC probe and of the low frequency probe absent the JFET front-end stage suggest a nearly quadratic error dependence on slope and almost no dependence on state. Such an error mechanism produces only offset (zeroth order distortion) and second harmonic distortion and is consistent with actual probe measurement results. The inclusion of the JFET front-end stage adds a comparable amount of third and smaller amounts of fourth, fifth, and seventh harmonic distortion components. Therefore, a reasonable approach is to choose basis functions consisting of higher powers of slope. We start with a five column matrix

$$V_1 = [y^2 \ y^3 \ y^4 \ y^5 \ y^7]$$

containing the second through fifth and seventh powers of signal slope. We use the notation $\dot{y}$ to express the first derivative of the vector $y$ with respect to time.

To allow for the possibility of non-uniform propagation delay of each of these components, the time derivative of each term is included in the model as well. Derivative terms permit the time position of each vector to vary relative to the data to which the model is fitted. (This follows from the fact that for small $\Delta T$, the first order Taylor series of $f(x+\Delta T) \approx f(x) + f'(x)\Delta T$.) So, we have

$$U_2 = \left[ \begin{array}{cccc} d(y^2) & d(y^3) & d(y^4) & d(y^5) & d(y^7) \\ \frac{dt}{dt} & \frac{dt}{dt} & \frac{dt}{dt} & \frac{dt}{dt} & \frac{dt}{dt} \end{array} \right]$$

$$= \left[ \begin{array}{cccc} 2\dot{y}^2 & 3\dot{y}^2 & 4\dot{y}^3 & 5\dot{y}^4 & 7\dot{y}^6 \end{array} \right]$$

where $\ddot{y}$ is the second derivative of $y$ with respect to time.

We set $U_a = [U_1 \ | \ U_2]$. Fitting the harmonic content of the model to the harmonic content of the probe requires solving the system of linear equations

$$e = U_a^T\beta$$

where $U_a^T$ equals $U_a$ with the fundamental component removed from each column.

Equation (4) describes the situation with a single calibration signal. As pointed out in [8], in practice, a better determination of $\beta$ requires a more global fit to multiple calibration signals of different amplitudes and frequencies. With multiple calibration signals, (4) becomes

$$\begin{bmatrix} e^{(1)} \\ e^{(2)} \\ \vdots \\ e^{(L)} \end{bmatrix} = \begin{bmatrix} U_a^{(1)} \\ U_a^{(2)} \\ \vdots \\ U_a^{(L)} \end{bmatrix} \beta,$$

$$e_t = U_t^T\beta = U_t^T K \beta^*$$ (5)

where $L$ is the number of calibration signals. The $n \times n$ diagonal matrix $K$ is introduced to provide a normalized design matrix, $U_t^T K$. The elements of $K$ are the reciprocal of the root-mean-square of each of the columns of $U_t$.

From (5), $\beta^*$ can be estimated in a least squares sense as

$$\beta^* = (U_t^T K)^{-1} (U_t^T K e_t)$$ (6)

With $\beta^*$ determined, ADC errors in a given set of data are modeled by computing

$$e_{mod} = U_t^T K \beta^*$$ (7)

where each column of $U_t$ has the same analytic form of the corresponding column in $U_a$ but re-evaluated using the state/slope values from the ADC data being corrected. Note that $U_t$ contains the fundamental spectral component.

Fig. 7 shows an $e_{mod}$ surface in the phase plane when obtained from data collected with the low frequency probe. The calibration signal frequency was 1 MHz, and amplitudes ranged from 0.1 V to 5 V. For comparison with Fig. 5, the fundamental component of $e_{mod}$ has been removed. Agreement between the surfaces in the two figures is very good. However, the model does not fit as well when calibrated over larger amplitudes and with other frequencies included.

![Fig. 7. Phase plane error surface of model generated errors with the fundamental component removed.](image-url)
Additional vectors are needed to assist the modeling effort. Effective ones can be found by considering a source of error in the probe known to be significant at the signal levels and frequencies of interest - nonlinear input capacitance. Fig. 8 shows in more detail the structure of the JFET input stage. \(R_s\) is the output impedance of the source follower, and \(C_g\) is the input capacitance of the differential amplifier. The voltage, \(V_G\), at the input to the differential stage is

\[
V_G = V_{IN} - IR_s = V_{IN} - R_s C_g \frac{dV_G}{dt}.
\]

The input capacitance of the differential stage varies with voltage approximately according to the relation

\[
C_g = C_0 \left(1 + \frac{V_{DD} - V_{IN}}{\psi_0} \right)^{1/3}
\]

where \(C_0\) is the zero bias junction capacitance, \(V_{DD}\) is the supply voltage, and \(\psi_0\) is the pn junction built-in potential [14].

The error in \(V_G\) caused by \(C_g\)'s voltage dependence equals the difference between the actual value of \(V_G\) and the value \(V_G\) would have if \(C_g\) were constant (taken, for example, at \(V_{IN} = 0\)). So, a new vector added to the model is

\[
u_{11} = V_G - V_G|_{V_{IN}=0} = \left(\frac{R_s C_0}{\left(1 + \frac{V_{DD} - V_{IN}}{\psi_0} \right)^{1/3}} - \frac{R_s C_0}{\left(1 + \frac{V_{DD}}{\psi_0} \right)^{1/3}}\right) \frac{dV_G}{dt} = \left(\frac{R_s C_0}{\left(1 + \frac{V_{DD} - V_{IN}}{\psi_0} \right)^{1/3}} - \frac{R_s C_0}{\left(1 + \frac{V_{DD}}{\psi_0} \right)^{1/3}}\right) y.
\]

Again, we opt to include in the model higher powers of this term on the assumption that the same mechanism that produces errors proportional to powers of slope will act similarly upon this error component. Experimentation suggests that the time derivatives of these terms are not needed. Therefore, the complete model (not normalized) is now

\[
U = [U_4 \mid u_{11} \mid u_{21} \mid u_{31} \mid u_{41}].
\]

VI. RESULTS

The model's ability to linearize the low frequency probe and correct distortion was tested. Calibration signals at frequencies of 200 kHz, 500 kHz, and 1 MHz over peak amplitudes between 2 V and 8 V were used to determine model coefficients.

As an example, Fig. 9 shows the residuals of a least squares sine fit to a 1 MHz filtered sine wave with a peak amplitude of 4.3 V. The data record contained two waveform cycles. Total harmonic distortion was determined using the test method described in [12] and [13]. The probe's corrected THD at 1 MHz was -83.7 dB, an improvement of 28 dB.

Fig. 9. Sine fit residuals from uncorrected and corrected low frequency probe data. The test frequency was 1 MHz.

Table 1 list the probe's uncorrected and corrected total harmonic distortion performance at three peak signal amplitudes and three frequencies. In all but one case, the corrected THD was better than -80 dB. (For 8 V at 1 MHz, the THD was -79 dB).

Fig. 10 shows the corrected and uncorrected zeroth order distortion (nonlinear offset error) measured with sine waves whose peak amplitude was 8 V. At 1 MHz, the offset is reduced from 8.5 mV to about 1 mV.

Fig. 11 shows the corrected and uncorrected phase error (of the fundamental component) measured with sine waves whose peak amplitude was 8 V. Here, the 8000 µrad phase error at 1 MHz is reduced to approximately 400 µrad.

Fig. 12 shows the corrected frequency response of the probe at peak signal amplitudes of 1 V, 3 V, 6 V, and 8 V.
The disagreement of nearly 600 μV/V at 1 MHz between the 1 V response and the 8 V response seen in Fig. 4 has been reduced to the uncertainty of the measurement, approximately 70 μV/V.

<table>
<thead>
<tr>
<th>A1 (V)</th>
<th>THD (dB) f= 200 kHz</th>
<th>THD (dB) f= 500 kHz</th>
<th>THD (dB) f= 1 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>U</td>
<td>C</td>
<td>U</td>
</tr>
<tr>
<td>3</td>
<td>-77.5</td>
<td>-87</td>
<td>-69</td>
</tr>
<tr>
<td>5</td>
<td>-73.1</td>
<td>-86.8</td>
<td>-63.6</td>
</tr>
<tr>
<td>8</td>
<td>-68</td>
<td>-82.5</td>
<td>-58.4</td>
</tr>
</tbody>
</table>

Table 1: Low frequency probe uncorrected (U) and corrected (C) total harmonic distortion.

VII. CONCLUSION

A model-based method for numerical compensation of distortion in a digitizer has been described. The method was developed from experimentation with a custom built digitizer designed for metrology applications. Analysis of the digitizer’s error behavior in the phase plane and a priori knowledge of the digitizer’s nonlinear input properties lead to the development of a linear error model. Although derived from an ad-hoc procedure, the model possesses the correct “built in” relationship between harmonic distortion and fundamental distortion. Accordingly, fitting the model to the digitizer’s harmonic distortion allows the model to compensate not only for harmonic distortion but also for nonlinear error in the digitizer’s gain, offset, and phase.

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REFERENCES