Large Area, Ultra-high Voltage 4H-SiC p-i-n Rectifiers

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***Abstract*—This paper reports the design, fabrication and high temperature characteristics of 1 mm^2, 4 mm^2 and 9 mm^2 4H-SiC p-i-n rectifiers with 6 kV, 5 kV, and 10 kV blocking voltage, respectively. These results were obtained from two lots in an effort to increase the total power levels on such rectifiers. An innovative design utilizing a highly doped p-type epitaxial Anode layer and junction termination extension (JTE) were used in order to realize good on-state as well as stable blocking characteristics. For the 1 mm^2 and 4 mm^2 rectifier, a forward voltage drop of less than 5 V was observed at 500 A/cm^2 and the peak reverse recovery current shows a modest 50% increase in the 25 °C to 225 °C temperature range. On the 10 kV, 9 mm^2 rectifier, a forward voltage drop of less than 4.8 V was observed at 100 A/cm^2 in the entire 25 °C to 200 °C temperature range. For this device, the reverse recovery characteristics show a modest 110% increase in the peak reverse recovery current from 25 °C to 200 °C. A dramatically low Q_{rr} of 3.8 μC was obtained at a forward current density of 220 A/cm^2 at 200 °C for this ultra high voltage rectifier. These devices show that more than three orders of magnitude reduction in reverse recovery charge is obtained in 4H-SiC rectifiers as compared to comparable Si rectifiers.**

***Index Terms*—P-i-n, rectifier, reverse recovery, SiC.**

I. Introduction

POWER devices made with silicon carbide (SiC) are expected to show great performance advantages as compared to those made with other semiconductors. This is primarily because 4H-SiC has an order of magnitude higher breakdown electric field (2–4 $\times 10^6$ V/cm) than Si and GaAs and an electron mobility only $\sim 20\%$ lower than silicon. A high breakdown electric field allows the design of SiC power devices with thinner and higher doped voltage-blocking layers. High voltage p-i-n rectifiers made using conventional semiconductor materials are restricted to < 50 kHz and $< 120\,^{\circ}$C, thereby severely limiting the availability of advanced electronic hardware used for energy storage, pulsed power, intelligent machinery and solid state power conditioning. These components require high power density, very high frequency and high temperature devices like the 4H-SiC p-i-n rectifier.

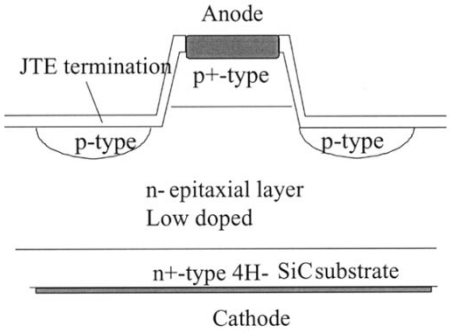

Fig. 1. Cross section of a high voltage 4H-SiC p-i-n rectifier using a highly doped epitaxially grown Anode layer and etched and implanted JTE structure.

The first successful attempt in the demonstration of a > 5 kV 4H-SiC rectifier was done using a 4H-SiC n$^-$ epitaxial layer with a thickness of 85 μm and a doping of 1 to 7 $\times 10^{14}$ cm^{-3} [1]. Other demonstrations [2]–[4] of > 3 kV 4H-SiC p-i-n rectifiers show that extremely high switching speeds and an on-state voltage drop comparable to Si p-i-n rectifiers are achieved when operated at sufficiently high current densities. The biggest challenges facing the realization of such high voltage rectifiers is the design of the edge termination and the growth of high purity, low defect density epitaxial layers with sufficiently high minority carrier lifetimes. Recent advances in SiC epitaxy have enabled the growth of > 50 μm thick 4H-SiC epitaxial layers with good carrier lifetimes. In the recent past, minority carrier lifetimes have been improved to a level that enables the realization of high voltage SiC rectifiers with < 4.5 V on-state drop at 100 A/cm^2.

II. Device Design and Fabrication

A. High Voltage Epitaxial Design

The cross-section of the 4H-SiC p-i-n rectifiers reported in this paper is shown in Fig. 1. The blocking voltage of such a rectifier is determined by (a) the doping and thickness of voltage blocking epitaxial layer (drift region) and (b) the effectiveness of the edge termination technique used to fabricate the device. Generally speaking, the current carrying capability depends on the physical area of the device and the minority carrier lifetime in the drift layers. In order for the device to sustain a high electric field during the reverse bias operation, it is essential to reduce the substrate induced defects, such as micropipes and epitaxially

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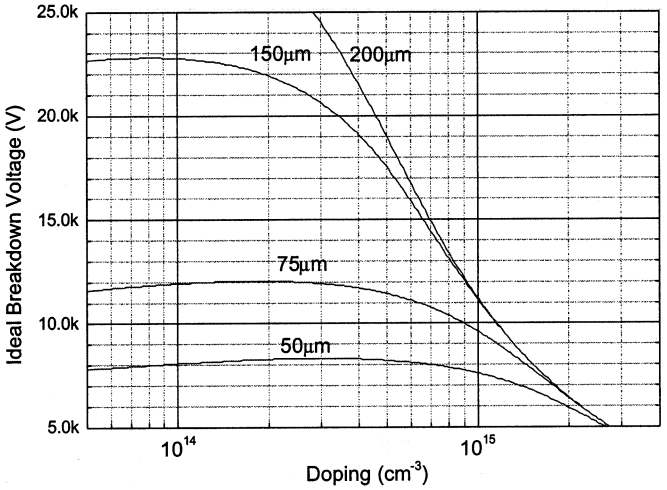

Fig. 2. Ideal blocking voltage as a function of epitaxial doping and thickness.

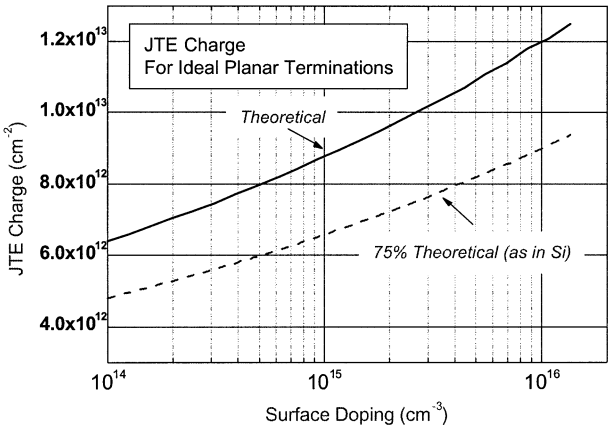

Fig. 3. JTE charge versus surface doping of the voltage blocking layer for a SiC device.

induced defects. A non-punchthrough drift region design corresponds to the case where drift region thickness is equal to or larger than the parallel plane avalanche breakdown width [5]. In the case of a punchthrough drift layer design, the epitaxial layer thickness is smaller than the parallel plane avalanche breakdown width. In a typical ultra high voltage design, a punchthrough design is used in order to keep the thickness of the epitaxial layer as small as possible. For such a case, the drift region thickness can be derived from basic depletion equation

$$W = \frac{\varepsilon \cdot E_C(N_D)}{q \cdot N_D} - \sqrt{\left[\frac{\varepsilon \cdot E_C(N_D)}{q \cdot N_D}\right]^2 - \left[\frac{2\varepsilon \cdot V_B}{q \cdot N_D}\right]} \quad (1)$$

where V_B is the device blocking voltage, W is the epitaxial (drift) layer thickness, N_D is the doping of the epitaxial layer, q is the electronic charge, ε is the dielectric constant of SiC, and $E_C(N_D)$ is the critical electric field as a function of the drift region doping. One of the empirically derived relationships showing the dependence of critical electric field with drift region doping in 4H-SiC is given by [6]

$$E_C = \frac{2.49 \times 10^6}{1 - \frac{1}{4}\log\left(\frac{N_D}{10^{16}}\right)} \quad (2)$$

Using these formulas, the ideal blocking voltage is plotted as a function of drift region doping and thickness in Fig. 2. Since the edge termination design as well as material defects influences the blocking voltage of these ultra high voltage devices, very large blocking voltage margins (20% for 5 kV devices and 33% for 10 kV devices) are adopted in the design of these devices.

B. Edge Termination Design

From a device design standpoint, the biggest challenge in achieving high voltage p-i-n rectifiers is the design and implementation of an effective edge termination. Such a technique is expected to make the electric field distribution uniform at the edge of the device, approaching the ideal breakdown voltage capability of the epitaxial layer used. Traditionally, many techniques like guard rings, floating field rings and trench guard rings [7] have been used. Another promising edge termination design involves implanting the device edge with an optimum p-type charge (for the typically used n-type epitaxial layer) in order to reduce the electric field gradually from the device edge to the outer periphery of the device structure. This technique is called junction termination extension (JTE) [5]. The optimally activated JTE charge depends upon the background doping concentration of the low doped n-type region. A plot showing the ideal total charge per unit area along a vertical cross-section of the implanted JTE region is shown in Fig. 3. The design of high voltage silicon devices made using JTE typically utilize a JTE charge 25% below the ideal predicted charge by theoretical analysis. This is because JTE charge in excess of the ideal value results in a sharp reduction in the obtained breakdown voltage, while a charge smaller than the optimum does not drastically affect the breakdown voltage of the device. The JTE charge corresponding to 75% is also plotted in this graph for silicon carbide.

C. Effect of Lifetime on Diode On-State Voltage Drop

Achieving a high level of carrier lifetimes in the thick, SiC epitaxial layers is critical to obtaining acceptable on-state voltage drop in 4H-SiC p-i-n rectifiers. Key lifetime limiting factors in thick epitaxial layers are a) compensating dopant species; b) unintentional metallic impurities; c) morphology of the epitaxial layers during and after the growth; and d) thickness and doping uniformity of thick epitaxial layers. For the extremely thick epitaxial layers used in these diodes, hot wall epitaxial reactors were used. Using these reactors, higher carrier lifetimes can be obtained.

The dominant components in the on-state voltage drop in a p-i-n diode are given by

$$V_F = V_{P+Cont.} + V_M + V_{P+N-} + V_{N+N-} + V_{Subs}$$

where V_F is the on-state voltage drop in a p-i-n diode, $V_{P+Cont.}$ is the p^+ contact resistance V_M is the "middle region" (i-region) voltage drop, V_{P+N} and V_{N+N-} are the junction drops at $P+N-$ and $N+N-$ junctions, and V_{Subs} is the resistive voltage drop in the substrate. In the past, a high value of $V_{P+Cont.}$, was obtained [1]. V_M is determined by the extent of

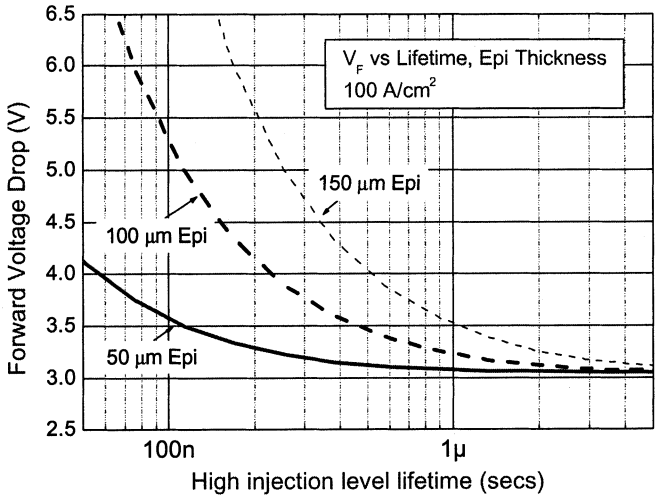

Fig. 4. Forward voltage drop on p-i-n diodes as a function of lifetime and epitaxial thickness.

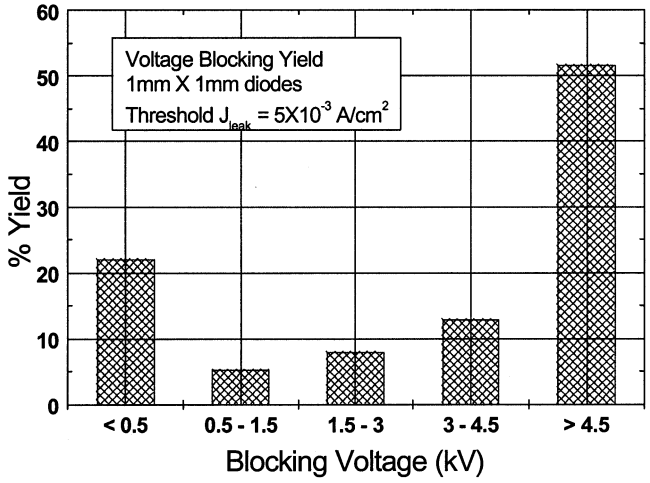

Fig. 5. On-wafer yield of $> 50\%$ was obtained for 1 mm^2 rectifiers capable of blocking > 4.5 kV for a leakage current density threshold of 5×10^{-3} A/cm^2.

carrier modulation in the i-region of the p-i-n diode and is dependent on the carrier lifetime by the following relationship [5]

$$V_M = \frac{3kT}{q}\left(\frac{W}{2L_a}\right)^2 \quad \text{for } W \le 2L_a$$

$$V_M = \frac{3\pi kT}{8q} e^{W/La} \quad \text{for } W \ge 2L_a$$

where k and T are Boltzmann's constant and operating temperature, L_a is the ambipolar diffusion length, which is given by $L_a = \sqrt{D_a \cdot \tau_{HL}}$, D_a is the ambipolar diffusion constant given by $D_a = \mu_a \cdot kT/q$, and τ_{HL} is the high level injection carrier lifetime. The ambipolar carrier mobility μ_a is given by $\mu_a = \mu_n\mu_p/(\mu_n + \mu_p)$. Here, μ_n and μ_p are the minority carrier electron and hole mobility in the voltage blocking drift layer.

V_{P+N-} and V_{N+N-} are dependent on the minority carrier concentrations at the two end-regions of the N$-$ drift layer. A detailed analysis of these voltage drops requires an iterative solution [5], which is not very easily calculated. If a reasonably high injection level is assumed, the sum of these end-region voltage drops can be estimated to be equal to the turn-on voltage of the SiC P+N+ junction. Resistive drops like V_{Subs} and $V_{P+cont.}$ are not trivial in bipolar device like p-i-n diodes because of extremely high current densities that typically flow through these devices, as compared to majority carrier devices like Schottky diodes. The on-state voltage drop of a p-i-n as a function of carrier lifetime and epitaxial layer thickness is plotted in Fig. 4. This figure shows that a higher carrier lifetime results in better conductivity modulation, with on-state voltage drop approaching the built-in voltage drop of a P+N+ junction. As expected, a thicker epitaxial layer requires a higher carrier lifetime in order to achieve a lower on-state voltage drop p-i-n diode. However, it is encouraging to note that beyond a carrier lifetime of 3 μs, even a 150 μm epitaxial layer is well modulated. Hence, SiC is expected to offer extremely high switching speeds even for devices made using such large thicknesses.

D. Device Parameters and Fabrication

For the 1 mm^2 and 4 mm^2 rectifiers, a 50 μm thick voltage blocking epitaxial layer with a doping of 9×10^{14} cm^{-3} were grown on low micropipe density (< 30 μP/cm^2) 4H-SiC n$^+$ substrates. The 9 mm^2 rectifiers were fabricated using a 150 μm thick voltage blocking epitaxial layer with a doping of 1 to 3×10^{14} cm^{-3}. To achieve a high, activated, p+ concentration, the Anode region was also epitaxially grown. The fabrication sequence of these rectifiers is as follows: an optimum dose of Boron was implanted at a high temperature after reactive ion etching through the 2 μm p+ Anode cap layer with more than 5×10^{18} cm^{-3} doping. The JTE dimension of 100 μm was used for 5 kV devices, and 400 μm for 10 kV devices. This implant was annealed at 1600 °C under Si overpressure condition, followed by a 2 μm LPCVD SiO_2 deposition. Thereafter, backside Ni ohmic metal, and titanium was deposited as anode metal. These metals were annealed at a high temperature to form the p-i-n anode and backside cathode contacts. These metals were followed by a 2 μm Ti/Pt/Au deposition to reduce the resistance and enable wire bonding. Rectifiers with active anode areas of 1 mm $\times$ 1 mm (total die size 1.15 mm $\times$ 1.15 mm) and 2 mm $\times$ 2 mm (total die size 2.15 mm $\times$ 2.15 mm) were fabricated alongside each other on 50 μm thick epitaxial layer wafers. On wafers with 150 μm epitaxial layers, devices with active Anode areas of 3 mm $\times$ 3 mm (total die size 3.5 mm $\times$ 3.5 mm) were fabricated. These devices had rounded edges to minimize concentration of electric field during their reverse bias operation. Devices were diced, brazed and wire-bonded for further characterization.

III. Characterization of 1 mm^2 and 4 mm^2 Rectifiers

A. Static Characteristics

After their fabrication, these rectifiers were extensively measured for static and dynamic characteristics. The goal for this study was to obtain a good yield of 4H-SiC rectifiers with a > 4.5 kV blocking voltage and a < 4 V on-state voltage drop

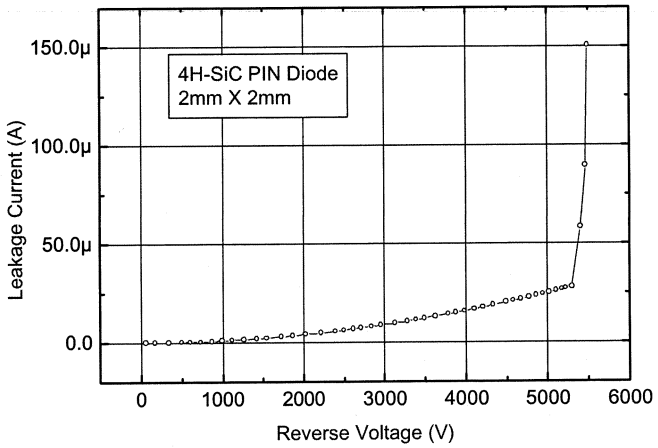

Fig. 6. Blocking characteristics of a 5.3 kV rectifier capable of carrying $>$ 20 A.

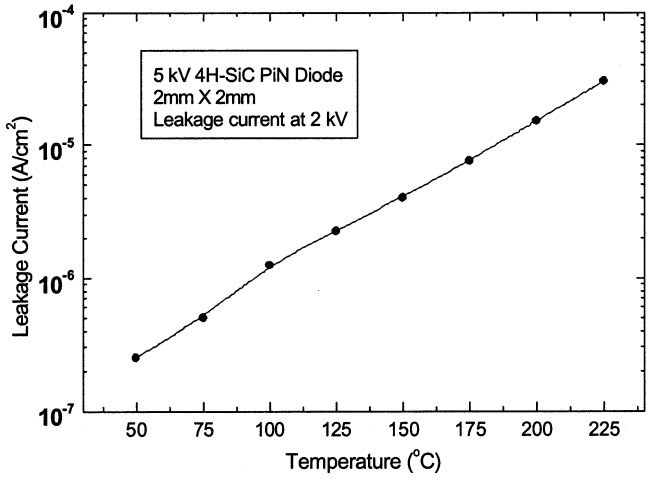

Fig. 7. Leakage current density was less than 4×10^{-5} A/cm^2 at 225 °C at 2 kV for a 0.04 cm^2 rectifier, even after an exponential increase with temperature.

at 100 A/cm^2. This would pave the path for a further increase in their power handling capabilities, as reported later in this paper. The on-state voltage drop was found to be very uniform (i.e., ± 0.2 V for good devices) across the wafer and was not a yield-limiting factor. The robust edge termination design outlined above and its associated processing allowed us to obtain a yield of $>$ 50% for 1 mm^2 rectifiers capable of blocking $>$ 4.5 kV when using a leakage current density threshold of 5×10^{-3} A/cm^2. The percentage distribution of *all* 1 mm^2 devices obtained from the wafer versus blocking voltage ranges is shown in Fig. 5. As seen from this figure, 27% of all devices block less than 1500 V, primarily due to materials defects such as micropipes. The reverse bias characteristics of a 2 mm $\times$ 2 mm rectifier are shown in Fig. 6.

The measured leakage current density was $< 10^{-3}$ A/cm^2 at 5 kV and thereafter it increases dramatically at about 5.3 kV. The breakdown characteristics were not catastrophic, with the device surviving after the applied voltage was reduced. High temperature (up to 225 °C) measurements were performed only at 2 kV because of equipment limitations. The leakage current increases exponentially with temperature, but was still found to be less than 4×10^{-5} A/cm^2 at 225 °C at 2 kV for a 4 mm^2 rectifier, as shown in Fig. 7. In standard commercial Si power devices, a leakage current density of $< 10^{-2}$ A/cm^2 is considered acceptable for defining blocking voltage. These results show that the edge termination design adopted for these devices is quite robust even at high temperatures.

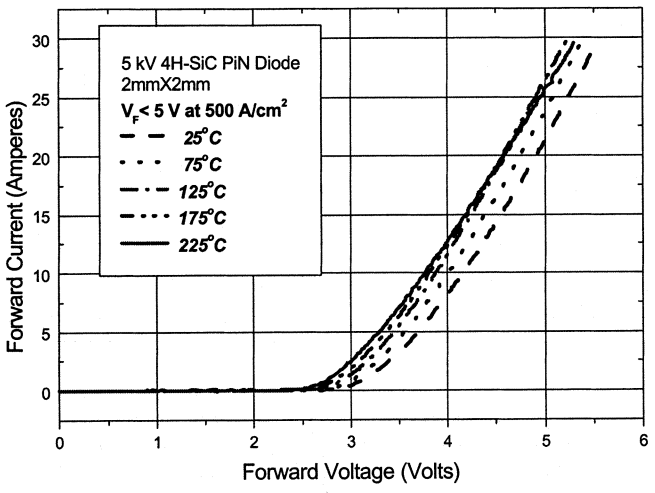

Fig. 8. Measured temperature dependence of on-state characteristics.

The forward current–voltage (I–V) characteristics show excellent on- state voltage drop. At a high current density of 1250 A/cm^2 (50 Amperes on a 2 mm $\times$ 2 mm device), the on-state voltage drop was only 6.9 V, which was significantly affected by the wire bonding resistance. The measured temperature dependence of the on-state characteristics for a 5 kV SiC p-i-n rectifier device with a typical current of 20 A (4 mm^2), is shown in Fig. 8. The decrease in on-state voltage with temperature is indicative of the increase in lifetime with increasing temperature for a conductivity modulated device and a decrease in bandgap of the PN junction. However, at a high temperature of 225 °C, a reduction in carrier mobility starts to increase the differential on-resistance across the drift layer. This leads to a crossover in the I–V characteristics at a high current density of 500 A/cm^2. In the entire 25 °C to 225 °C range, the change in on-state voltage drop remains in a somewhat insignificant 0.4 V range, as seen from Fig. 8. This shows that SiC p-i-n rectifiers are stable with temperature. In case of Si diodes, over 40% reduction in on-state voltage drop was measured in the 25 °C to 125 °C range [8]. This results in poor current sharing when such devices are operated in parallel because of the generation of 'hot spots' that hog a large amount of current.

B. Reverse Recovery Measurements

Detailed switching measurements were conducted on some 5 kV blocking 4H-SiC p-i-n rectifiers. The most important dynamic characteristics for a rectifier are its reverse recovery characteristics and their variation with operating temperature. The reverse recovery tests were performed for various values of di/dt. Fig. 9 shows the current versus time waveforms of the 20 A, 5 kV SiC p-i-n rectifiers for three different reverse di/dt values. At the conventional 40 A/μs, the peak reverse current was only 65% of the forward current. As the reverse di/dt was increased to 100 A/μs and 1700 A/μs, the peak reverse current

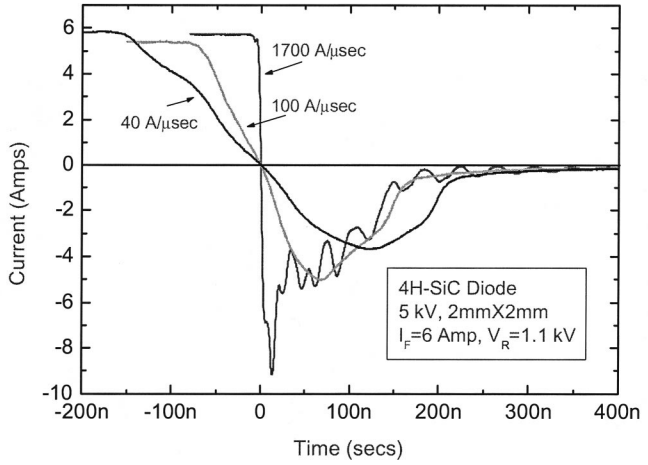

Fig. 9. Reverse recovery characteristics show a 2× increase in the peak reverse recovery current when the reverse di/dt was increased from 40 A/μs to an extremely high 1700 A/μs.

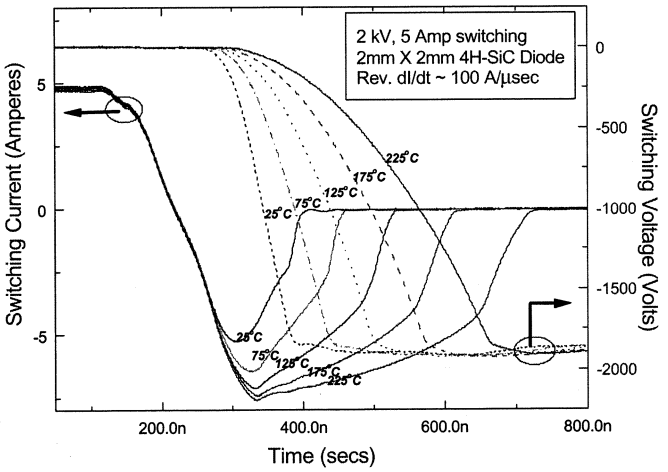

Fig. 11. Current and voltage waveforms of a 5 kV rectifier switched at 25 °C, 75 °C, 125 °C, 175 °C and 225 °C.

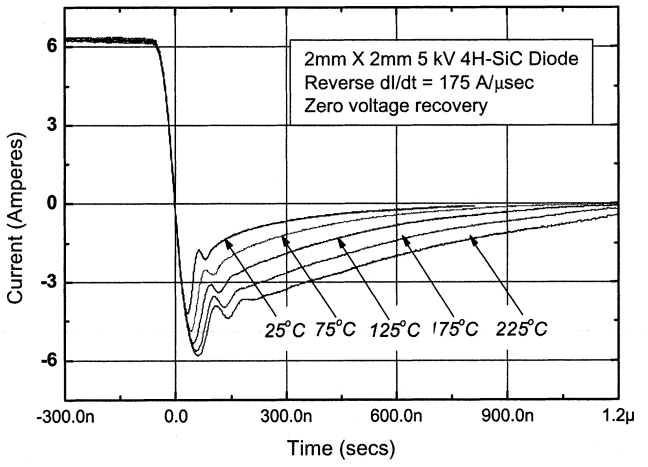

Fig. 10. High temperature reverse recovery characteristics show a modest increase in the peak reverse current as the operating temperature is increased from 25 °C to 225 °C.

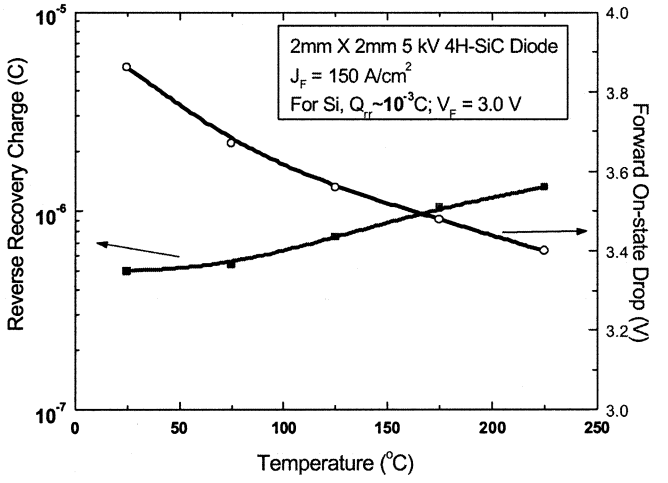

Fig. 12. Reverse recovery charge and on-state voltage drop as a function of temperature for a 5 kV p-i-n diode.

to forward current ratio increased to 90% and 150%, respectively. As compared to high voltage Si p-i-n rectifiers, this is a relatively insignificant change, considering that extremely high reverse di/dt values were used. One hypothesis for this effect is that the amount of reverse recovery charge is at least three orders of magnitude smaller than Si diodes.

C. High Temperature Switching Measurements

The temperature dependence of the rectifier switching characteristics for a 2 mm × 2 mm 5 kV device is shown in Fig. 10. These measurements are taken at a relatively high reverse di/dt of 175 A/μs, when the rectifier is switching near zero voltage at 6.2 A. Usually, the reverse bias applied does not affect the reverse recovery characteristics. As seen from this figure, the peak reverse current increases by a modest 50% when the temperature was increased from 25 °C to 225 °C. The total reverse recovery charge, which is the area under the I–t curve when the rectifier is undergoing reverse recovery, increases by approximately 100%, as the operating temperature is increased from 25 °C to 225 °C. These rectifiers show repeatable switching characteristics as the operating temperature was increased from 25 °C to 225 °C. The turn-off time increases from 0.2 μs to 0.65 μs while switching 125 A/cm^2 (5 A) and 2 kV with a reverse di/dt of 100 A/μs, as shown in Fig. 11. A level of 2 kV was chosen as the highest voltage possible for the pulse generator used in this measurement. These rectifiers do not show a "snappy" recovery and have substantially smaller noise signatures when compared to 600 V silicon p-i-n rectifiers.

D. On-State and Switching Trade-Off

Fig. 12 shows that the on-state voltage drop changes from 3.9 V to 3.4 V at 150 A/cm^2 as the operating temperature is increased from 25 °C to 225 °C. Under the same conditions, the measured reverse recovery charge increases from 0.5 $\times 10^{-6}$ C to 1.3 $\times 10^{-6}$ C. This is a $\mathbf{10^3}\times$ reduction in $Q_{\rm rr}$ as compared to comparably rated Si (in terms of blocking voltage) rectifiers. It is worthwhile to note that reverse recovery charge shows a 4–6× increase with temperature from 25 °C to 125 °C, even for ultrafast Si rectifiers [8]. Two factors contribute to the dramatically

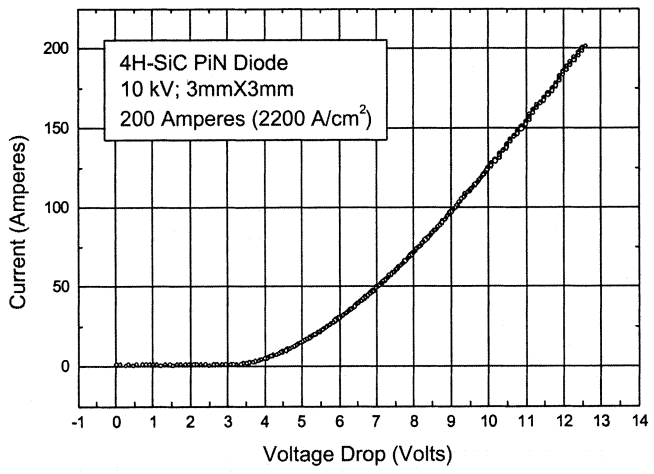

Fig. 13. Pulsed (250 μs) on-state characteristics of a 4H-SiC p-i-n rectifier capable of blocking 10 kV taken using standard high power TEK371 curve tracer.

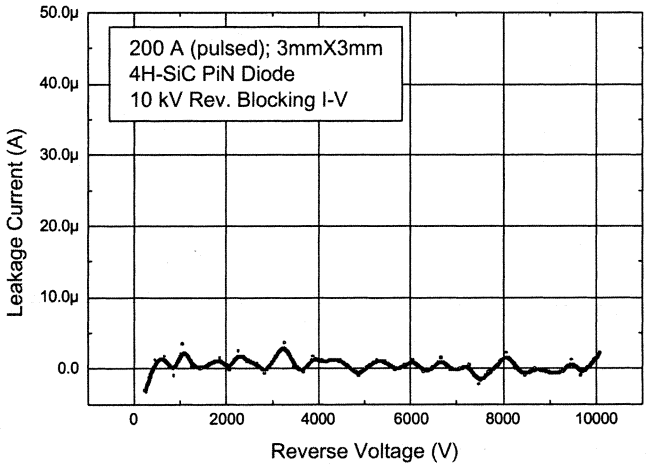

Fig. 14. Blocking characteristics of a 10 kV rectifier capable of carrying >200 A (pulsed).

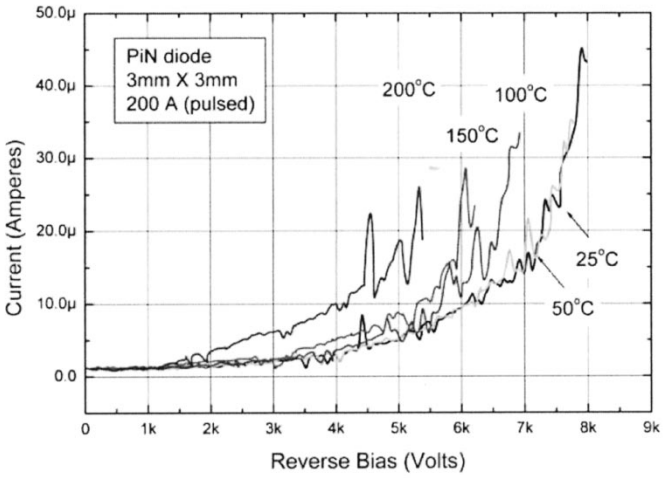

Fig. 15. Reverse I–V characteristics of a packaged 8 kV p-i-n rectifier fabricated alongside the 10 kV blocking rectifier.

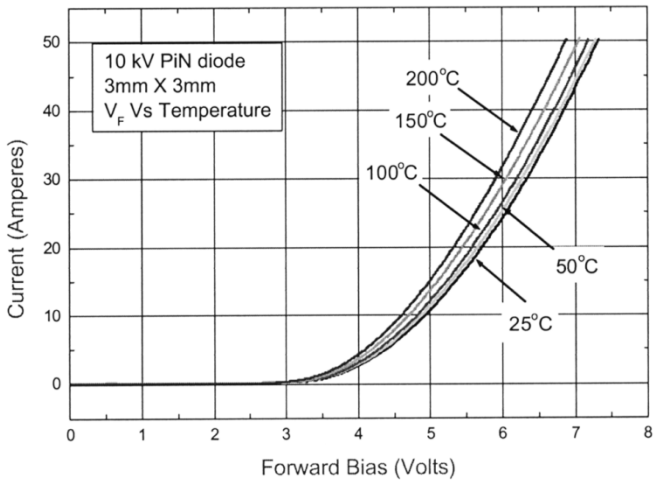

Fig. 16. Forward I–V characteristics of a packaged 8 kV p-i-n rectifier fabricated alongside the 10 kV blocking rectifier.

smaller reverse recovery charge ($Q_{\rm rr}$) in 4H-SiC rectifiers as compared to similarly rated Si rectifiers: a) the 20–25$\times$ thinner voltage blocking layers with 20$\times$ higher doping dramatically reduce the total volume of excess charge in the drift layer and b) the carrier lifetime required for these thinner voltage blocking layers can be $> 10\times$ smaller than those required for Si devices for a similar mid-region voltage drop. A much smaller carrier lifetime and thinner voltage blocking layer in 4H-SiC results in a very stable on-state voltage drop with temperature.

IV. Characterization of 9 mm^2 Devices

A. Static Characteristics

The on-state voltage drop was found to be very uniform across the wafer on which these diodes were fabricated. At 2 kA/cm^2, the differential on-resistance was only 3 mΩ-cm^2, as shown in Fig. 13. The reverse bias characteristics of a 3 mm $\times$ 3 mm rectifier are shown in Fig. 14. The measured leakage current density was $< 10^{-4}$ A/cm^2 at 10 kV and increases dramatically thereafter. The device survived after the voltage was reduced and then reapplied. High temperature (up to 200 °C) measurements on 8 kV capable packaged devices fabricated alongside the 10 kV rectifier show that the leakage current increases with voltage beyond 150 °C, resulting in a blocking voltage of about 5.3 kV at the leakage current threshold of 20 μA, as shown in Fig. 15. The choice of this leakage current is quite arbitrary and was limited by the highest leakage current capability of the measurement equipment. The measured temperature dependence of the on-state characteristics for a 10 kV, 9 mm^2 SiC p-i-n rectifier is shown in Fig. 16. The decrease in on-state voltage with temperature is indicative of the increase in lifetime with temperature for a conductivity modulated device and a decrease in bandgap of the PN junction. However, at a high temperature of 200 °C, a reduction in carrier mobility starts to increase the differential on-resistance across the drift layer. In the entire 25 °C to 200 °C range, the change in the on-state voltage drop remains in a somewhat insignificant 0.4 V range.

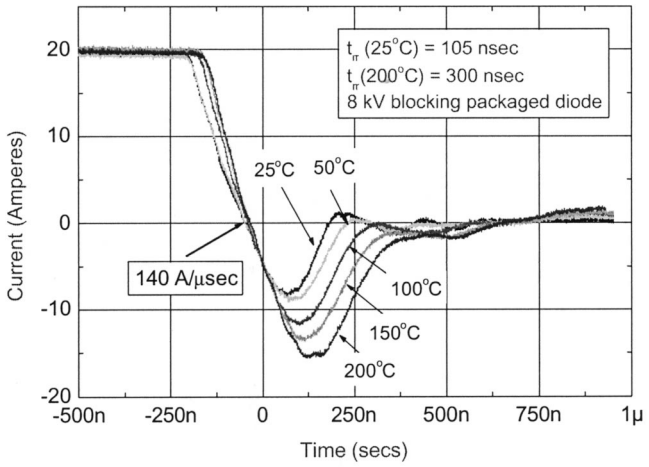

Fig. 17. High temperature reverse recovery characteristics show a modest increase in the peak reverse current as the operating temperature is increased from 25 °C to 200 °C.

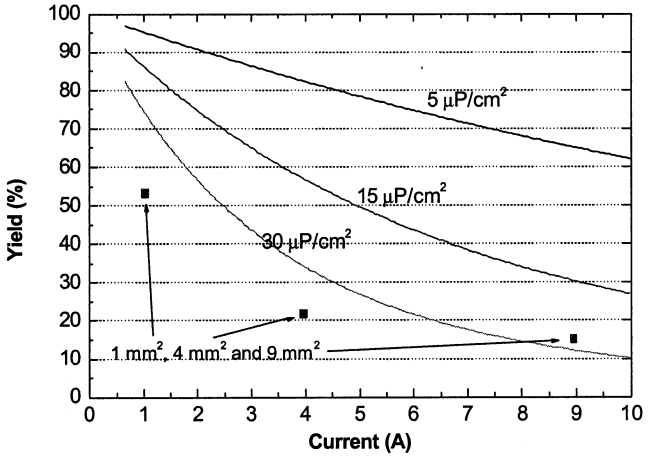

Fig. 18. Theoretical and experimentally obtained yields on 1 mm^2, 4 mm^2 and 9 mm^2 devices at 4.5 kV, 4.5 kV, and 7 kV.

B. Reverse Recovery Measurements

Detailed switching measurements were conducted on some 8 kV blocking 4H-SiC p-i-n rectifiers fabricated alongside the 10 kV rectifiers. The temperature dependence of the rectifier switching characteristics for a 3 mm $\times$ 3 mm 10 kV device is shown in Fig. 17. These measurements are taken at a relatively high reverse di/dt of 142 A/μs, when the rectifier is switching 600 V at 20 A. As seen from this figure, the peak reverse current increases by a modest 110% when the temperature was increased from 25 °C to 200 °C. The total reverse recovery charge, which is the area under the I-t curve when the rectifier is undergoing reverse recovery, increases by approximately 100%, as the operating temperature is increased from 25 °C to 200 °C. These rectifiers show fairly stable switching characteristics as the operating temperature was increased from 25 °C to 200 °C. The turn-off time increases from 0.2 μs to 0.7 μs while switching 220 A/cm^2 (20 A). It is very encouraging to note that the total reverse recovery charge increases from an insignificant 1.17 μC to 3.8 μC as the temperature was increased from room temperature to 200 °C. These rectifiers do not show a "snappy" recovery and have substantially smaller noise signatures when compared to silicon p-i-n rectifiers.

V. Discussion

A. Yields on 1 mm^2, 4 mm^2, and 9 mm^2 Diodes

Usually, fairly uniform on-state characteristics are obtained across the wafers since the advent of hot-wall epitaxial reactors and good anode metal processing. However, the yield due to blocking voltage on 4H-SiC devices is dependent on many material, processing and design related issues. Material related issues include: micropipes on the wafers, epitaxial growth related defects and crystal defects like dislocations and stacking faults. It is difficult to quantize the effect of each of these factors on device yields, but great deal of data on these effects have been studied in reference [9]. Processing related issues are related to ion implant activation of JTE termination species, uniformity of the mesa etch and quality of the dielectric used in passivation of edges. Design related effects on yield are edge diameter of diodes and the choice of dose for JTE implant. As mentioned earlier, it is very difficult to separate the influence of all these parameters on device yields. Assuming a random distribution of defects, device yield is given by

$$Y = e^{-A \cdot d}$$

where Y is the yield, A is the area of the device and d is the defect density in per cm^2. Many researchers propose that the biggest yield-limiting factor in modern high voltage devices is micropipes. A plot of yield as a function of device size and micropipe defect density is shown in Fig. 18. As shown earlier, the yield on 1 mm^2 diodes was 52% at 4.5 kV. For 4 mm^2 devices, the obtained yield was approximately 20% at $>$ 4.5 kV; and for 9 mm^2 it was 22% at $>$ 7 kV. All these devices show quite abrupt breakdown characteristics at room temperature. All these devices were fabricated using similar processing techniques. However, the 9 mm^2 devices were fabricated roughly 18 months after the 1 mm^2 and 4 mm^2 devices and might have benefited from the better micropipe densities obtained in more recent wafers.

B. V_F Drift With Time

Recently, a peculiar problem has been identified to challenge the use of these high performance rectifiers in widespread use. This is the increase of forward voltage drop (V_F) in bipolar p-i-n diodes with time, as they are kept biased for a reasonably long time. Due to the very low stacking fault energy of SiC, stacking faults may nucleate from specific pre-existing defects in SiC bipolar device structures and grow under typical forward conduction conditions [10], [11]. Extensive growth of these defects can attenuate the electron-hole plasma present in the device during forward operation and lead to an increase in the forward voltage of the overall device structure. Degradation of the forward voltage is a significant barrier to fully exploiting the capabilities of SiC bipolar devices, especially in applications that employ several devices in parallel for current sharing.

This phenomenon was observed in both these sets of devices. For a 4 mm^2, the V_F increases from 4.11 V to 4.19 V over 130 hours as the on-state current was maintained at approximately

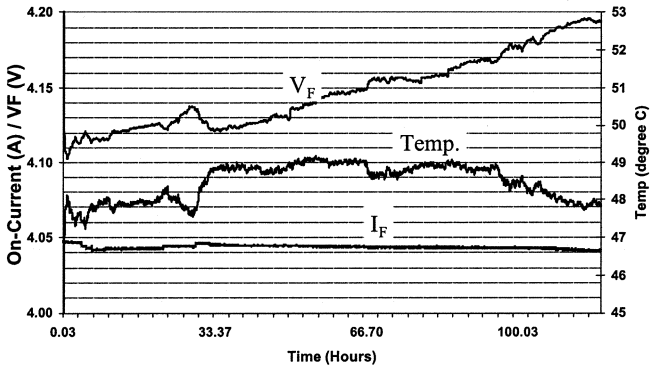

Fig. 19. V_F drift on 4 mm^2 devices shows an increase from 4.11 V to 4.19 V at 100 A/cm^2, as the temperature was held relatively constant.

100 A/cm^2 and the temperature was held relatively constant, as shown in Fig. 19. This is an active part of our research now and our research has determined that the effect of any specific process change must be evaluated in the context of a complete device fabrication methodology. However, several critical areas will require additional scrutiny.

VI. Conclusion

Switching speed is the primary source of losses in most high voltage (> 3 kV) power conditioning circuits. This paper shows the design, fabrication and high temperature operation of ultra high voltage 4H-SiC p-i-n rectifiers, which demonstrate orders of magnitude faster switching operation than conventional rectifiers. A much smaller carrier lifetime and thinner voltage blocking layer in 4H-SiC results in a very stable on-state voltage drop with temperature. The robust edge termination design shows low leakage and good high temperature performance. These characteristics are very significant for the realization of next generation, advanced military and utility hardware.

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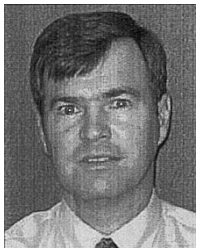

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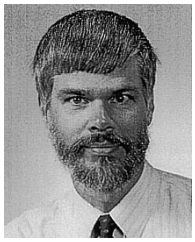

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John W. Palmour (M"95) received the B.S. and Ph.D degrees from North Carolina State University, Raleigh, in 1982 and 1988, respectively. His major was in materials science and engineering, with a minor in electrical engineering. His doctoral research concentrated on processing techniques and transistor development in SiC, and he demonstrated a SiC MOSFET operating at 650 °C.

He became a Co-founder of Cree, Inc., Durham, NC, where he is the Director of Advanced Devices. He has been responsible for the development of high-voltage, high-temperature 4H-SiC power diodes, MOSFETs, and thyristors, as well as high-frequency SiC MESFETs and planar n-channel and p-channel 6H-SiC MOSFETs. He is also responsible for Cree's development of microwave GaN HEMTs. He has coauthored over 175 publications in various conference proceedings and refereed journals, and is an inventor on 17 issued U.S. patents concerning semiconducting SiC. He also serves on the Board of Directors for Cree, Inc.