Wire Bonding to Advanced Copper, Low-K Integrated Circuits, the Metal/Dielectric Stacks, and Materials Considerations

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***Abstract*—There are three areas to consider when designing/implementing wire bonding to advanced ULSI damascene–copper chips having copper metallization and low dielectric-constant polymers embedded beneath them (Cu/LoK). These are:**

1) **the copper-pad top-surface oxidation inhibitor coating-metal/organic/inorganic. (Current work involves evaluating the metal and inorganic options);**
2) **the low dielectric constant materials available;**
3) **under-pad metal/polymer stacks and support structures necessary for bondability and reliability.**

There are also various polymer/metallurgical interactions, resulting in long term packaged-device reliability problems, that can occur as the result of the wire bonding process over low modulus, LoK materials with barriers. These include cracked diffusion barriers, copper diffusion into the LoK polymers, cracking/spalling/crazing of the LoK materials, and bond pad indentation ("cupping"). Low-K polymer materials, with high expansion coefficients and low thermal conductivities, can also increase the stress and further extend any existing damage to barriers. Many of the above problems have previously been encountered when bonding to pads over polymers (MCM-D, polymer buildup-layers on PCBs, PBGAs, flex circuits, etc.), and they share some of the same solutions. Well designed LoK and the underpad structures should have no negative effect on bonding parameters and be invisible to the bonding process.

***Index Terms*—Bondability, copper, diffusion barriers, LoK, polymer, thin film, wire bonding.**

I. Introduction

In ORDER to fully solve the problems of wire bonding to chips with copper bond pads, it is necessary to protect the top surface of the copper from oxidation, sulfiding, etc. This can be achieved with:

1) various metallurgical coatings, such as gold, or aluminum with a barrier;
2) thin organic films (OSPs);
3) thin inorganic films (SiN, SiO_2, Al_2O_3, etc.).

After appropriate surface protection is achieved, then the problems of wire bonding to pads over soft substrates must be addressed. The latter incorporates the knowledge obtained from the past on bonding to multichip modules, where bond pads are often located over low modulus polymers. Cu/LoK chips and multichip modules (MCMs) are part of the same problem and share the same general solutions. However, some special conditions exist for bonding to Cu/LoK structures.

Wire bonds to semiconductor devices have traditionally been made to aluminum pads over silicon or silicon dioxide, which presented both an ideal metallurgy and a rigid platform for thermosonic bonding. However, currently, copper pads can be located over low modulus polymers that are themselves encased in brittle diffusion barriers which can crack during bonding. This can result in bond yield and/or reliability problems. Therefore, it has become necessary for wire bonding (a metallurgical welding process) to include the material properties of complex layers of polymers and diffusion barriers as being equally important in the bonding process as the metallurgy. In cases where the polymers' modulus is low, it is necessary to design special underpad support structures.

II. Top Surface Protective Coatings for Copper Bond Pads

A major problem encountered in bonding to Cu/LoK chips results from the oxidation of the copper during handling, wafer sawing, and especially from the high temperatures of die attach curing and thermosonic bonding. Copper oxide (and to a lesser extent copper sulfide) on the pad will inhibit wire bonding and/or decrease the yield. Several approaches have emerged to protect the Cu pad. The first (which is currently in production) is to apply a diffusion barrier, such as titanium nitride, Ta, TiW, etc., over the Cu and then deposit aluminum on top of it [1], [2]. This prevents Al–Cu Intermetallic compounds from forming. It also results in chips that can be bonded with the same parameters as in the past and have the same well-understood bond reliability. In addition, it is wafer-fab compatible. However, the fabrication requires several more deposition, masking, and etching steps and is therefore more expensive. There is also the possibility that, if the bonding process cracks the diffusion barrier, the reliability can be worse than if no diffusion barrier existed. Such could happen if a low-modulus dielectric was below the bond pad and MCM-type *cupping* or *sinking* [3] occurred as described below. Another problem is that the Al/barrier/Cu method has been patented [4], and it may not be available, or may be costly. A summary of possible top-surface coating is given in Table I.

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TABLE I
COPPER-PAD TOP-SURFACE COATINGS FOR WIRE BONDING

TOP SURFACE METALS FOR BONDABILITY

1. **Copper Itself (oxidation lowers/kills bondability)**
2. **Possible Metals/Stacks to Enhance Bondability**
   a. Au/barrier/Cu, *or* just Au/Cu, presents a reliable known bondable surface
   b. Al/barrier/Cu, also a known surface
   c. Ag/Cu, known reliable interface (Ag migration on fine pitch may be a problem)
   d. Pd/Cu (or with Ni, etc.), a well known reliable interface, but Pd is expensive!
   e. Other (combinations)

NON-METAL OXIDATION INHIBITORS

1. a. Traditional Cu oxidation inhibitors: (benzotriazoles, imidazole ≈ 5-20 nm)
   b. OSPs: (substituted benzimidazoles, e.g., Entek Plus ≈ 200 nm)
   {both have many problems, e.g., corrosive application, shelf life, etc.}
2. Deposited thin (< 5 nm) inorganic films (SiO_2, SiN, Al_2O_3, SiC, etc.)

A. Metallic Top Surfaces for Bondability

Gold has traditionally been the top metal surface of choice on Cu for wire bondability, usually with a Ni barrier between it and the Cu. However, the Ni is an extra manufacturing step and can diffuse through the gold (by grain boundary diffusion), resulting in unbondable nickel oxide on the surface. Fortunately, gold can be directly plated onto Cu. When gold and copper interdiffuse, they primarily form superlattice structures, which are ductile and not considered a reliability hazard. However, as with Ni, Cu will diffuse through and oxidize on the surface, but it diffuses slower than Ni through Au [5]. The diffusion coefficient of the copper (damascene-process) into and through an autocatalytic Au film has not been established. Plating solution additives, such as a few ppm of Pb to slow down grain boundary diffusion, inhibits autocatalytic deposition. Thus, in order to avoid copper diffusing to the Au surface during the various packaging thermal-steps, the Au thickness should be >0.5 μm. Measurements are currently being made of the diffusion coefficient on a *first-time-of-arrival* Auger hot-plate technique so that a more accurate (minimum) thickness can be determined, based on the expected processing time/temperatures.

A constraint in using Au on Cu on a chip (post wafer-fab) is that it should be plated by a nonelectrolytic process, since some of the semiconductor pads may have no ground-return connection. (Much more complex in-fab processes may achieve this, but not on post-fab wafers). To achieve this in our work, a two-step immersion/autocatalytic deposition process had to be adopted, since the available autocatalytic gold would not deposit directly onto Cu. The copper surface was first primed with an immersion gold, which deposited a 10 nm primer coating. This step was followed by a pH-neutral autocatalytic gold build-up [6] to the 0.5–1 μm desired thickness. Ball bonding tests were conducted on these films to establish adhesion and bondability. Then, the films were deposited on silicon test chips having bond pads of $\approx$0.5 μm of damascene-process copper. Bondability was established with manual ball bonders using both 60 kHz and 120 kHz ultrasonic frequencies. The bonding stage was set to 150 °C. The bonds made at both frequencies were approximately 80% welded as evaluated with a ball shear test and ball diameter measurements [3]. The long-term reliability of the Au/Cu interface (bonded or plated) was established by Hall, *et al.* [7], although not for the present damascene–Cu structures. This will be determined in the future.

Silver plating directly onto the copper pads offers another top-metal option. This metallurgy has been used for years on copper lead frames and the bond reliability for gold wire bonds is well understood. However, if Ag top metal is used on chips, there could be a metal-migration problem (if the pad is not recessed below the passivation **and** the chip is not plastic-encapsulated). Recent work [8] suggests that about 3 V (applied, not field strength) is the threshold necessary to start silver metal migration. If so, then modern ICs operating on lower voltage (e.g., $\leq$1.2 V) would not result in metal migration. Thus, the familiar, bondable, silver metallization may be used in the future. However, its migration-reliability must be further verified, especially for fine pitch pads! This solution would also require lower voltage testing/burn-in than is currently used by much of the industry.

B. Organic Coatings

Organic Solderability Preservatives [OSP] (B-1, in Table I) may be a possible alternative. OSPs have been used on PC boards for copper oxidation protection during soldering for over 25 years. One problem in using them for bond pads on Cu/LoK chips is that the application process is not done in the wafer fab and that the deposition solutions used may damage other parts of a very expensive wafer. Also, if the film is thin enough to readily bond through ($\approx$5 nm), then it is environmentally degradable and has a poor shelf-life. Results thus far have not been encouraging.

C. Thin Inorganic Films

Thin inorganic films represent a different class of surface protection. The process is to deposit a thin, hard, brittle, inorganic film such as silicon dioxide or silicon nitride over the copper surface *during wafer fabrication*. Such a hard brittle film on a soft metal will break-up/shatter during wire bonding and be pushed aside as the wire/ball and the bond pad deform in the same manner as the thin, brittle, aluminum oxide films when wire bonding to aluminum bond pads (Fig. 1).

Several of these deposited films are compatible with *and currently used for other purposes* in the normal wafer fabrication processing. They can be applied over the entire wafer, without patterning and preferential removal (mask/etch step). Such films will also protect the copper bond pads from oxidizing during final wafer processing, during assembly and packaging operations such as wafer sawing, die attach curing, and the high temperatures of thermosonic bonding. In application, the inorganic film is applied during wafer processing any time after the copper bond pads are exposed to the wafer surface, but preferably near

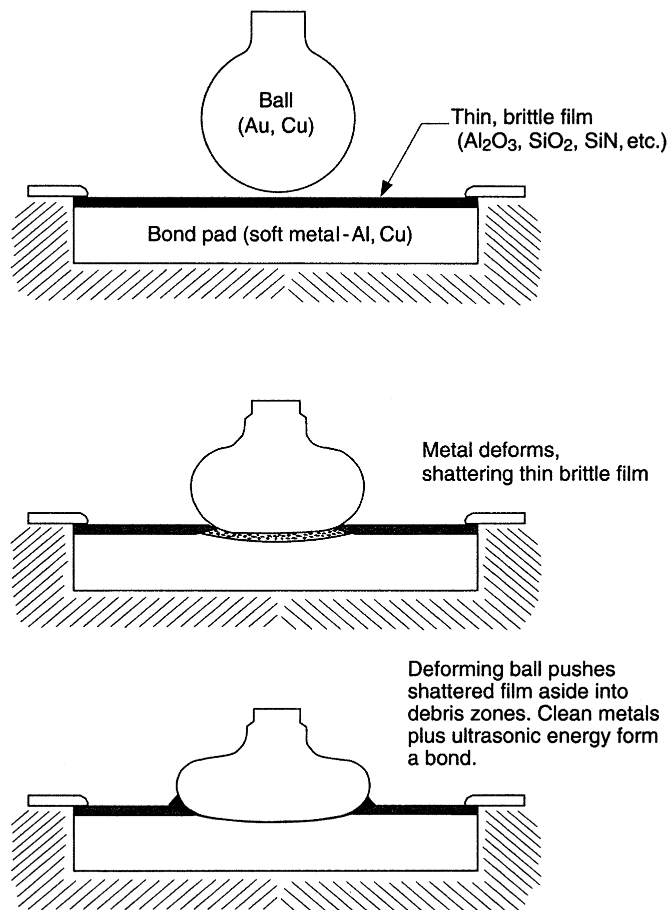

Fig. 1. Pictorial representation of bond formation through a thin inorganic film.

or at the end of processing. A thin nonmetallic inorganic layer of <50 Å (3 nm to 5 nm) is deposited over the entire wafer. (This thickness is similar to the native aluminum oxide on aluminum bond pads that the industry regularly bonds through, but is not intended to be restrictive and may be somewhat thicker or thinner as long as it protects the Cu pad from oxidation and can be bonded.) Normally, it is not necessary to remove the deposited film from any part of the wafer, assuming it is nonconductive. The coated wafer can then be shipped to the assembly and packaging facility and handled in the normal manner. A *cursory* search of the patent literature reveals many patents on depositing thin films on surfaces for various types of protection, but only two were called out for wire bonding use (US Pat. 5 272 376 and 6 352 743 B1), as was the case in [4].

D) Material Properties That Effect Wire Bonding to Copper Through Thin Inorganic Films:

In a materials stack of a thin inorganic film over a metal pad, one should choose the film to have both a low ultimate strength and a low fracture toughness. This permits easy cracking and shattering of the film when the wire/ball descends to the pad. Some examples of possible films that can easily be vapor deposited are SiO_2, SiN, SiC, etc. The material properties of these very thin films are not available at present, and will depend upon the deposition method. They must be measured on the actual films to be accurate. However, footnote[1] gives some properties in ceramic form, which may be indicative. From these, SiO_2 and Al_2O_3 have the lowest fracture toughness and should be the best choices for thin-film oxidation protection of bond pads. Work on the first has started.

As with the inorganic films, there are minimal materials data directly derived from damascene Cu. Most studies of this material are directed toward the deposition, the electromigration, or conductivity properties of such interconnects [9]. For bonding purposes, the underlying copper bond pad metal should be soft and have a low yield strength, so that it deforms easily under the bond-force/ultrasonic-softening process. Annealing at 300 °C *or higher* for 30 min may be necessary, if such time/temperatures are not encountered during other wafer processing steps. The as-received chips with bare copper bond pads (damascene process) supplied by International SEMATECH (ISMT) and used in these studies had a modulus of 128 ± 10 GPa and a nanohardness of 1.8 ± 0.23 GPa. Annealing for 30 min at 300 °C in forming gas did **not** reduce these values, however, a similar argon anneal did reduce the nanohardness to below 1 GPa and the modulus to $\sim$50 GPa. This annealing investigation will continue. Since the hardness and yield strength are usually inversely proportional to the grain size, and since grains in thin films can be sample-size limited, it may be necessary to increase the bond pad thickness as well as to anneal it in order to soften the copper for best gold ball bonding results. We note that Cu balls are harder than gold and may be an alternative wire bonding material for inorganic-film-protected Cu pads.

Unannealed SiN coated copper chips that had been etch-thinned from 5 nm to $\sim$3 nm were gold ball-bonded with both 60 kHz and 120 kHz manual bonders. Results for both frequencies gave only $\sim$40% welded area, which is not acceptable for a production process. In order to establish a base line, these samples had not been annealed, as discussed above. The fracture toughness of SiN is higher than Al_2O_3 or SiO_2 (in ceramic form—see footnote 1) and thus this material may not be the best protective coating for wire bonding; and in addition a softer metal would be required. This work is continuing.

Experimental work for verifying the use of the above films will include those easiest and most available to deposit, silicon nitride and silicon oxide. The copper bond pads on test wafers as well as the silicon nitride samples supplied by ISMT had approximately 5 nm thickness over the Cu bond pads, which for some tests was etched back to $\approx$3 nm.

One potential problem in protecting copper with thin inorganic films is that wafer probing (especially on fine pitch pads) will damage them and expose the bare Cu, which will oxidize at thermosonic bonding temperatures. A very recent paper [10] described some of these problems and proposed solutions. An additional solution would be to apply the film **after** probing, which would, however, be after the normal wafer processing. In the future, $<0.18\ \mu$m line-width copper chips will be available, and self-testing circuitry could be built into these chips.

[1]Values from **ceramics** for the **fracture toughness** are: SiN $\approx$ 4, $SiO_2 \approx 0.73$, SiC ≈ 3.3, and $Al_2O_3 \approx 2.2$: (MPa $m^{1/2}$).

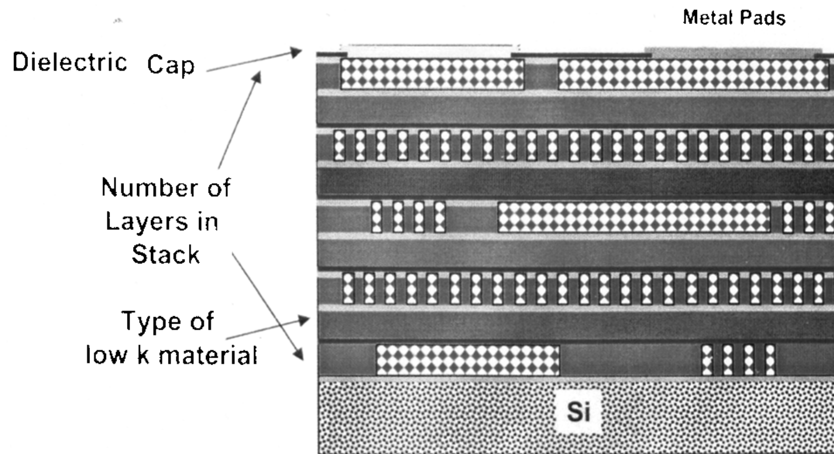

Fig. 2. Copper–damascene/LoK metal/dielectric stack, which indicates the complex structures that must be accommodated for wire bonding. Each layer is separated by thin barriers. Figure permission of ISMT.

This requires only a few special (nonoperating signal/power) bond pads for probing/testing, leaving all normal bond pads intact (un-scoured) and protected. There have been problems in implementing self-testing chips. However, this test method is currently being developed.

III. Wire Bonding to Pads Over Low Modulus Materials

Modern Cu/LoK chips can be extremely complex with 8 or 10 metal layers, separated by dielectrics, which themselves must be surrounded by diffusion barriers. An example of such a structure, which has five metal layers and four via layers plus barriers, is shown in Fig. 2. Thus, successful bonding to these chips requires understanding the problems and solutions for bonding to pads over low modulus polymers. The appropriate background comes from past experience with MCMs and has been extensively published. A summary is given in [3]. Bond pads on modern MCM-D, flex, etc. substrates usually consist of gold-plated thin-film Cu, or Al, placed on top of one or more layers of relatively soft polyimide (PI), benzocyclobutene (BCB), or polytetrafluoroethylene (PTFE). Variations of both BCB and PTFE have been proposed for use as LoK dielectrics in Cu/LoK chips. Bonding over such low modulus materials has resulted in bond pad *cupping* and delamination from the polymer, lowering the bond yield and reducing the device reliability [3]. Such polymers may also absorb ultrasonic energy, be heated by it, and be softened, further lowering the yield. Rigidizing the pad with a hard metal (Ni, Ti, Cr, etc.) is a normal solution for MCMs, but may not be possible for fine-pitch semiconductor pads.

Another polymer-induced bonding problem occurs when the bond pad area is small, roughly comparable to the deformed bond dimensions (such as for a fine-pitch bond pad). If the polymer is soft (its modulus is less than $\approx$3–4 GPa) or it is heated above its T_g (as during thermosonic bonding), then the entire rigid, but small, bond pad can partially *sink* into the soft plastic during application of the bonding force. Dynamic bond-pad-*sinking* changes (lowers) the effective bond force over the first 20 ms to 50 ms after the capillary (bonding tool) drops. This normally occurs during the time that ultrasonic energy is applied and the bond is formed. The *dynamically* changing bond force requires more U.S. energy or the welding will be incomplete. Some advance autobonders offer force-controlled bonding modes to prevent this. However, if any cupping or sinking occurs it will damage the LoK diffusion barriers and lead to failure. Therefore, some form of underpad support structures compatible with IC fabrication are required. See Section V.

A. Bonding to Integrated Circuits With Copper Bond Pads Over LoK Material

The above discussion of bonding to multichip module pads over soft substrates comprises essential background and understanding for bonding to the most advanced ICs. These ICs have copper metallization as well as low dielectric constant, low modulus dielectrics (Cu/LoK) beneath the bond pads, as opposed to older ICs that had SiO_2 or silicon there. The LoK materials often must be processed with the wafer at high temperatures (up to 425 °C) compared to thermosonic bonding temperatures (150 °C to 200 °C). Therefore, their T_gs are chosen to be high and should not directly pose temperature-dependent bonding problems; except that the already low modulus does decrease somewhat at bonding temperatures.

A significant difference between MCMs and Cu/LoK chips is that bond pads on the latter are required to be small ($<$70 μm and ultimately down to 20 μm pitch, ***ISMT 2001 Roadmap***) resulting in *sinking* into, and/or mechanically damaging the low modulus polymers and barrier films. Also, the metal/dielectric stack can be multilayered and extremely complex. Often on such devices, there can be $>$10 stacked layers of different metals, polymers, barriers, and oxides above the silicon. In addition, one or more stiffening (support layers/structures) may be required between the Cu and the LoK material. Without these, any resulting polymer *sinking* or *cupping* can crack/damage any barrier layers below the bond pad, leading to electrical leakage or degraded high-frequency properties. ***There is no analytical/electrical method for detecting such damage unless it results in immediate electrical leakage/short circuit.*** Otherwise, it remains a long term reliability problem and/or one that can only be revealed by thermo-mechanical stress tests (i.e., temperature, temperature-cycling/shock followed

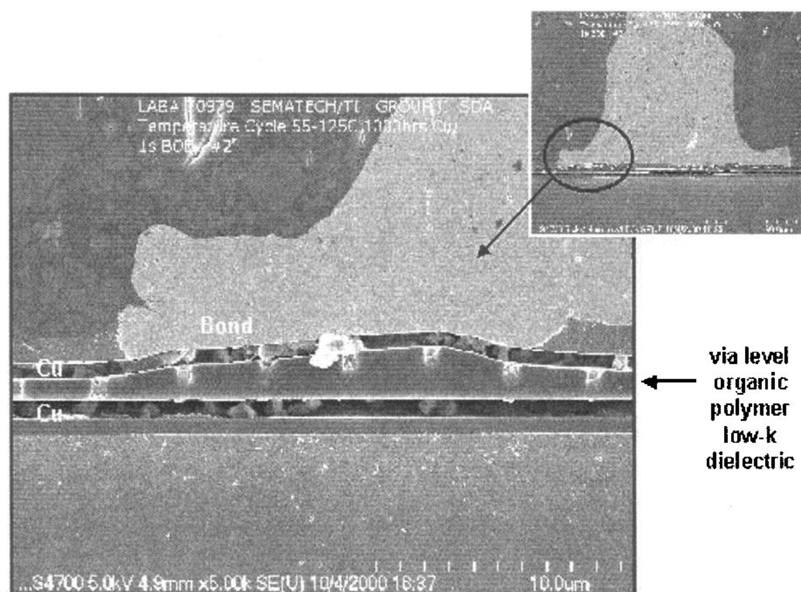

Fig. 3. Wire bond that has been temperature cycled for 1000 h under Mil Std. 883, Method 1010, condition B. Buckling is evident within the LoK layer. Used by permission of L. Stark (Texas Instruments), D. Chesire (Agere Systems), and ISMT.

by electrical measurements). Also, very high temperature (>300 °C with bias) stress-tests may be necessary. An example of the effect of bonding stresses on low-K polymers as revealed by temperature cycles is shown in Fig. 3.

It should be noted that values in Table II were supplied, as noted, in the Reference column. They may change as their manufacturers improve their products.

IV. Polymer Issues

Most of the LoK polymers used/proposed, interact chemically or electrically with copper in the presence of moisture and/or temperature and bias. Therefore, barriers have, of necessity, been introduced to limit such problems. However, those thin, brittle barriers (SiN, Ta, etc. 0.05 μm thick) can be damaged during the wire bonding process, when located on soft LoK materials, if *cupping* or *sinking* occurs. Damage may include cracked diffusion barriers, copper diffusion into the LoK polymers, spalling/cracking/crazing of the polymers, and bond pad deformation. Cracked barriers/etc. cannot be observed by present analytical methods and only produce failure later, during device life or during extended thermo-mechanical/electrical stress testing, as was done in the bond in Fig. 3 above. Also, the passivation surrounding/overlapping the bond pad perimeter can delaminate from the pad (or the pad from the LoK) during bonding, and lead to moisture or other degradation during device life. Most LoK materials have large temperature expansion coefficients. During device temperature excursions, the resultant stresses can also damage barriers or cause delamination.

Currently, there is no consensus on the choice of LoK dielectric materials for use in ICs, and new ones/variations are being introduced frequently. Different IC companies have chosen different materials, depending upon their own processing requirements. Some examples of materials that are being considered/used for such applications are given in Table II. Many of these have very low moduli. Others are easily fractured or crushed. All can result in bonding or reliability problems. The dielectric constant can be lowered by incorporating small air-filled pores. However, the mechanical properties will decline dramatically.

V. Under-Pad Mechanical Support Structures

Careful design of under-pad metal and dielectric support structures is essential to avoid crushing, delamination, cratering, or other damage to the polymer or silicon. One recent paper [11] addressed this problem on Al/LoK (HSQ) structures, using tungsten plug arrays and other support structures as well as HSQ "reservoirs" between the SiO_2 (TEOS) and other metal layers to prevent polymer damage. Those support structures were designed for 80 μm pitch Al bond pads. Currently, 45 μm pitch is in production, and ultimately 20 μm is projected. Thus, there will be greater potential to damage LoK bond pad structures by *sinking* in the future. The design of Al/LoK supported structures in reference [11] is not generally applicable to most proposed Cu/LoK structures.

One possible approach is to use mixed SiO_2, LoK, and copper structures, applying SiO_2 under the copper pad and at the via levels. The LoK is only applied between the Cu signal lines. This offers the stronger mechanical support of SiO_2 for bonding and results in an increased, but still acceptable, low capacity between signal lines for the desired high performance. Some have used Al (over SiO_2) as the top level metal, applying vias under the bond pads, which connect to the buried copper signal and power lines. This has been referred to as a hybrid structure [12]. It avoids the problem of applying a barrier over Cu pads, and depositing Al for bonding, as was described above in Section II). Fig. 4 is an example of a structure having Al applied directly over the SiO_2 and using a via (Al or a tungsten plug) to connect to the Cu conductors below (through an appropriate barrier layer). However, these hybrid structures are extremely

TABLE II
LOW DIELECTRIC CONSTANT MATERIALS PROPOSED FOR Cu-LoK STRUCTURES[a]

Material	Organic – O Inorganic – I	? @ 25°C	Modulus (GPa,) 25°C	Hardness (GPa)	Fracture–Tough ($MPa-m^{1/2}$)[d]	CTE [b] (10^{-6}/°C)	References
DVS–BCB	O	2.6	2.9	0.37	0.37	52	Dow Chem.
SiLK–H	O	2.652.0	2.45	0.31	0.60.42	62	Dow Chem.
Black Diamond (SiO_2 + C)	I /O (the class of OSGs)	2.72.4	7.76	0.13–3.6	0.2 – 0.3	23	Applied Matls.
HSG–R25	O	2.5	2.5	–	–	–	Hitachi Chem.
FLARE	O	2.8	2.5	0.35	–	?60	Honeywell (Allied Signal)
HOSP	O–I	2.5	6	0.4	–	17	Honeywell
HSQ [c]	I	2.7–3.5	4.9	0.85	0.27–0.44	14	Ref. [11]
TEOS (SiO_2)	I	3.2–4.1	72–100	9.5	0.46	1–2	Ref. [11]
Nanoglass silica (gels) pores <5 nm	I	1.3!2.5	0.5–2.3	0.03–0.1	< 0.04 to 0.14	4 up (varies)	Many sources
Parylene AF–4 [e]	O	2.7	2.28	–	–	30–80	Union Carbide
Speedfilm BX [e]	O+5% I	2.1	1.66	–	–	55	W. L. Gore

[a] Trade names are used to describe a material when no other identifier is available. This does not imply any endorsement.
[b] CTEs of organic LoK materials generally increase with temperature. Reported values are average and in the range of 25 °C to 100 °C.
[c] Hydrogen Silsesquioxane (a porous inorganic).
[d] Fracture toughness of "Material" interface with SiO_2, SiN, Ta, or TaN
[e] Discontinued products

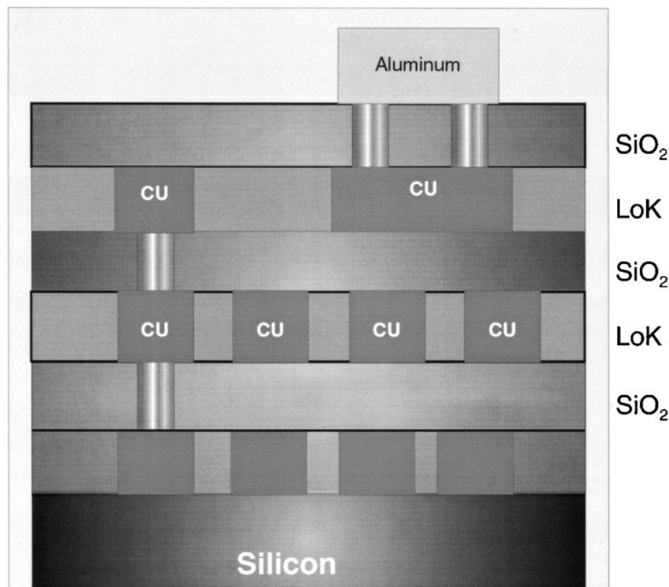

Fig. 4. Hybrid (mixed) dielectric structure of SiO_2 and LoK that avoids special bond pads with coatings.

complex and expensive to manufacture. In addition, the tungsten vias through SiO_2 require 425 °C processing, which limits the choice of LoK dielectrics (currently) to OSGs and one available high temperature organic polymer.

VI. CONCLUSION

The new Cu/LoK chips represent a new technology. Instead of one metal for both bonding and conduction, and one dielectric (SiO_2), there are now many possibilities for each. Each organization makes materials choices optimized for their needs. Currently, the preferred top surfaces for bonding are Al/barrier/Cu, thin inorganic films, or Au. The preferred LoK dielectric is a high-temperature organic or an OSG. The underpad bonding-support structures are still being developed. The desire is that the chosen structures will be invisible to the assembly operation. Work at our laboratories is directed toward developing a compatible gold process (immersion Au followed by autocatalytic Au) and preferred inorganic protective films. Fundamental data such as nanohardness and modulus of the damascene copper were measured. The diffusion coefficient of such copper into/through autocatalytic Au is being determined.

If one expects to wire bond to pads over polymer "soft substrates," be they MCMs or Cu/LoK devices, then one must design the system (polymer/metallization structures) with that objective in mind; otherwise, the wire-bond/device yield and/or device reliability may be unacceptable and redesign costly! Wire bonding in microelectronics is entering a new area in which understanding the materials/metallurgical structures is at least as important as understanding the wire bonding process.

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REFERENCES

[1] T. A. Tran, L. Yong, B. Williams, S. Chen, and A. Chen, "Fine-pitch probing and wirebonding and reliability of aluminum capped copper bond pads," in *Proc. HDI Conf.*, Denver, CO, Apr. 25–28, 2000, pp. 390–395.

[2] L. Mercado, R. Radke, M. Ruston, T. Tran, B. Willias, L. Yong, A. Chen, and S. Chen, "Fine pitch probing and wire bonding and reliability of multi-layer copper interconnect structures," in *Proc. 2000 IMAPS Symp.*, Boston, MA, Sept. 20–22, 2000, pp. 727–732.

[3] G. G. Harman, *Wire Bonding in Microelectronics, Materials, Processes Reliability, and Yield*, Second ed. New York: McGraw Hill, 1997, See Chapter 10 for more references.

[4] R. W. Cheung and M.-R. Lin, "Advanced copper interconnect system that is compatible with existing IC wire bonding technology," U.S. Patent 5 785 236, issued July 28, 1998.

[5] P. M. Hall and J. M. Morabito, "Diffusion problems in microelectronics packaging," *Thin Solid Films*, vol. 53, pp. 175–182, 1978.

[6] T. Inoue *et al.*, "Stable noncyanide electroless gold plating which is applicable to manufacturing of fine pattern printed wiring boards," in *Proc. 45th Electron. Comp. Technol. Conf.*, Las Vegas, NV, May 21–24, 1995, pp. 1059–1067.

[7] P. M. Hall, N. T. Panousis, and P. R. Menzel, "Strength of gold-plated copper leads on thin film circuits under accelerated aging," *IEEE Trans. Parts, Hybrids, Packag.*, vol. PHP-11, pp. 202–205, Sept. 1975.

[8] R. Manepalli, F. Stepniak, S. Allen, and P. Kohl, "Silver metallization for advanced interconnects," *IEEE Trans. Adv. Packag.*, vol. 22, pp. 4–8, Feb. 1999.

[9] G. B. Alers *et al.*, "Trade-off between reliability and post CMP defects during recrystallization anneal for copper damascene interconnects," in *Proc. 39th Annual IRPS Conf.*, Orlando, FL, 2001, pp. 350–354.

[10] C.-C. Lee *et al.*, "Back-end assembly solution to bare copper bond pad wafers," in *Proc. 2001 Int. Symp. Microelectron. (IMAPS) Conf.*, Baltimore, MD, Oct. 9–11, 2001, pp. 511–514.

[11] M. Saran *et al.*, "Elimination of bond-pad damage through structural reinforcement of intermetal dielectrics," in *Proc. 36th Annu. IRPS Conf.*, Mar. 31–Apr. 2, 1998, pp. 225–231.

[12] Y. Ohtomo, "Multi-Gb/s CMOS LSI design and requirements for LSI packages," in *Proc. 5th VLSI Packag. Workshop Jpn.*, Kyoto, Japan, Dec. 4–6, 2000, pp. 6–9.

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