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Stacked nanoscale Josephson junction arrays for high-performance voltage standards*

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Abstract

Superconducting Josephson voltage standard systems have replaced electrochemical cell (battery-like) artifact standards for voltage metrology because quantum-based systems produce precise and accurate voltages independent of any material parameters. The performance of such systems has improved over the years as a result of advances in microelectronic fabrication. A new generation of voltage standard systems has new capabilities, such as stable and programmable dc voltages, ac voltages, and arbitrary waveform synthesis. However, even better performance of these new systems can be achieved through the development of nanoscale fabrication techniques and subnanometer control of junction barrier thicknesses. We are developing densely packed Josephson junction arrays for advanced voltage standard systems because performance will dramatically improve with high-density series arrays of junctions when the junction spacing becomes less than 100 nm. We describe the present state of our programmable and arbitrary waveform synthesizer systems and we present our

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latest nanoscale fabrication results using $MoSi_2$ as a normal-metal junction barrier. Preliminary results suggest that we should be able to achieve a 40 nm junction spacing.

I. Introduction

Over the past 30 years, Josephson voltage standard systems have advanced as a result of improvements in microelectronic fabrication as well as by clever physics and engineering ideas (see reviews by Kautz,[1] Niemeyer,[2] Hamilton[3], and Benz[4]). We are currently developing two microtechnology-based voltage standard systems: the Programmable Josephson Voltage Standard and the Josephson Arbitrary Waveform Synthesizer. The programmable system is fully automated and provides stable programmable dc voltages from −1 V to +1 V. The synthesizer is the first quantum-based ac voltage standard source. It uses perfectly quantized Josephson pulses to generate arbitrary waveforms with low harmonic distortion and stable, calculable rms voltages. Both systems are presently limited to output voltages less than 10 V as a result of frequency requirements and the limits of junction fabrication technology. We hope to achieve higher practical voltages through development of nanoscale junction technology, in which 13,000 junctions are closely spaced at 50 nm to 100 nm intervals and require subnanometer dimensional control of their barriers. Such high-density junction arrays also have smaller transmission-line inductance per junction, which will allow operation of the ac voltage standard at higher frequencies, namely hundreds of kilohertz to megahertz frequencies. Both the programmable system and the waveform synthesizer are being developed for metrology applications to calibrate and evaluate high-performance dc, audio and rf electronic instruments, such as spectrum analyzers, digital-to-analog and analog-to-digital converters, and power meters. This is important for continuing the high quality of calibrations for present and future electrical metrology standards for the Department of Defense. In collaboration with Northrop Grumman researchers we are also applying this technology to high-performance digital radar, where perfect Josephson quantization

is essential for creating stable, low spur-free-dynamic-range and low-phase-noise arbitrary waveforms. Such waveforms enable the detection of slow, small targets in the presence of a large background signal. Our technology also would allow multiple waveforms to be simultaneously transmitted for multiple functions, including communications. Most recently it has been used as a quantized voltage noise source for a novel electronic-based Johnson noise thermometry system.[5]

The basis for all these Josephson voltage standard systems is the superconducting Josephson junction.[6] When driven with a sinusoidal frequency f, a Josephson junction has a voltage-current characteristic with constant-voltage regions given by $V_n = nhf/2e$, where n is an integer and $h/2e$ is the ratio of Planck's constant to twice the elementary charge. These values of V_n are directly proportional to the frequency through fundamental constants only so that the constant-voltage step values are not dependent upon any environmental or material parameters. Since frequency can be accurately and stably controlled to parts in 10^{12}, a Josephson junction can convert frequency into accurate voltages. This is the reason that the Josephson effect is used for voltage metrology and why conventional Josephson voltage standard systems are the best representation of the volt for calibrations in numerous military, commercial and national standards laboratories throughout the world. We will now describe the new voltage standard systems that are under development.

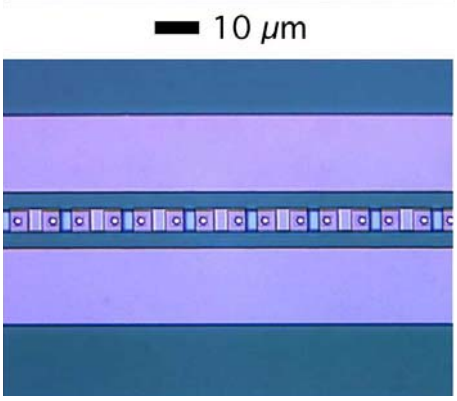

Fig. 1. Nb-PdAu-Nb 2 μm × 2 μm SNS junctions. Minimum feature sizes are 1 μm diameter via holes in the insulating layer that allow superconducting wiring to connect adjacent junctions. The SNS junctions are distributed in series along the 6 μm-wide center conductor of a coplanar waveguide.

II. Programmable Voltage Standard

In 1995, Hamilton et al. [7] suggested a quantum-based ac voltage standard using a Josephson digital-to-analog converter. By dividing a large array into a binary sequence of independently biased smaller arrays, it was hoped that the circuit would be capable of rapidly selecting stable arbitrary dc voltages as well as ac waveforms with a calculable rms voltage. This required the development of highly damped Josephson junctions with non-hysteretic voltage-current characteristics, which are quite different from the hysteretic junctions used in the conventional voltage standard system. Such junctions have constant-voltage steps that are single-valued, so that individual constant-voltage steps can be chosen using predetermined bias currents. This idea for a new voltage standard renewed our interest in developing uniform intrinsically shunted junctions for array applications, specifically in superconductor-normal metal-superconductor (SNS) junctions. Expectations were not high with regard to junction uniformity since critical current density is exponentially dependent upon the barrier thickness, and sputter-deposited metal films are not as uniform as thermally grown oxides. Nevertheless, moderately thick 30 nm to 40 nm barriers of PdAu provided sufficient uniformity with appropriate junction characteristics.[8,9]

However, to maintain junction critical currents less than 10 mA, the high current densities (2 mA/μm^2 to 4 mA/μm^2) require small junction areas (1 μm^2 to 4 μm^2, see Fig. 1). Fortunately, large critical currents yield correspondingly larger current ranges for the constant-voltage steps. This improves operating margins for the circuits and allows for dramatically improved noise immunity compared to that of hysteretic junctions in conventional standards, which have critical currents of only ~100 μA and a 10 μA operating current. The present 1 V programmable voltage standard system uses a chip shown in Fig. 2 with 32 768 Nb-PdAu-Nb junctions.[10] The 2 μm × 2 μm junctions have critical currents of I_c~8 mA and normal-state resistances R~3 mΩ. The smallest features in the circuit are 1 μm diameter vias for wiring contacts to each junction, as shown in Fig. 1.

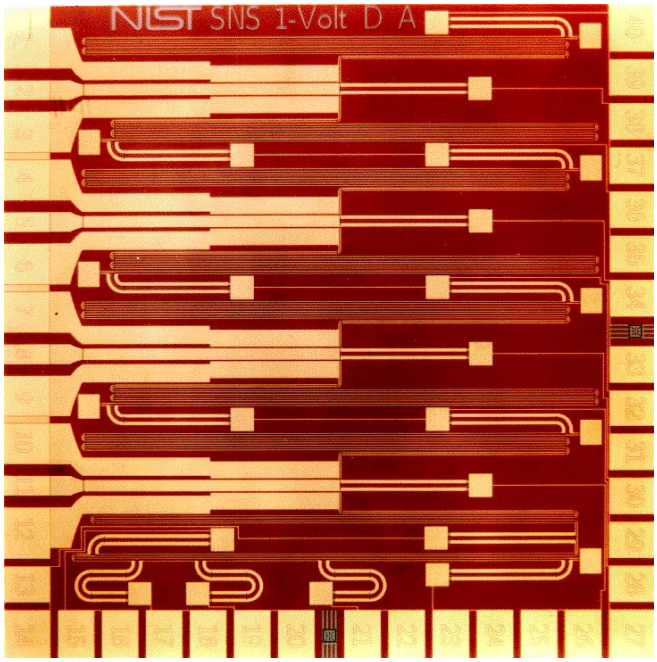

Fig. 2. 1 cm × cm NIST 1 V programmable voltage standard chip. Microwaves are launched onto the chip on the four coplanar waveguide lines on the left side. The pads along the bottom and right sides are for dc bias lines to each array. There are 8 arrays of 4096 junctions each. The bottom array is divided into a binary sequence of 2048, 1024, 512, 256 and two arrays of 128 junctions.

One of the remaining challenges is to create a programmable standard capable of generating large voltages, such as the 10 V conventional standard. Generating large voltages requires maximizing both the microwave frequency and the number of junctions. Operating margins, on the other hand, depend on both the junction uniformity and the uniformity of the microwave power applied to all junctions. Series arrays of junctions are typically distributed along a microstrip transmission line or a coplanar waveguide. Such distributed arrays are used for many of our designs. For example, the 1 V programmable chip uses arrays of 4096 junctions in each of eight parallel 50 Ω coplanar waveguides.

However the number of series junctions cannot be arbitrarily increased to increase the output voltage in a distributed array. Because the junctions are dissipative, the number of junctions that can be placed in a transmission line with fixed impedance is limited by the microwave attenuation that can be tolerated for an acceptable reduction in operating margins. For an array of N junctions with resistance

R per junction, the total rf-voltage drop across the array due to junction dissipation is approximately 1-exp(-*NR/2Z*), where Z = 50 Ω is the transmission line impedance.[11, 12] To prevent standing wave reflections that would further degrade the microwave uniformity, the transmission line must also be properly terminated The optimum performance for a distributed array for our 16 GHz microwave drive frequency uses a 4096-junction array of 3 mΩ junctions. Unfortunately, 88 % of the power is dissipated in the termination resistor. If we demand the same operating margins by always (1) choosing the same ratio $\alpha = NR/2Z$, (2) matching the I_cR product to the frequency (times $h/2e$), and (3) maximizing the junction critical current to 10 mA, then the number of junctions that can be placed in the transmission line decreases with increasing frequency, $N = 4e\alpha ZI_c/hf$. Thus, increasing the drive frequency cannot independently achieve larger output voltages for distributed arrays, although it may improve circuit yield by reducing the number of junctions.

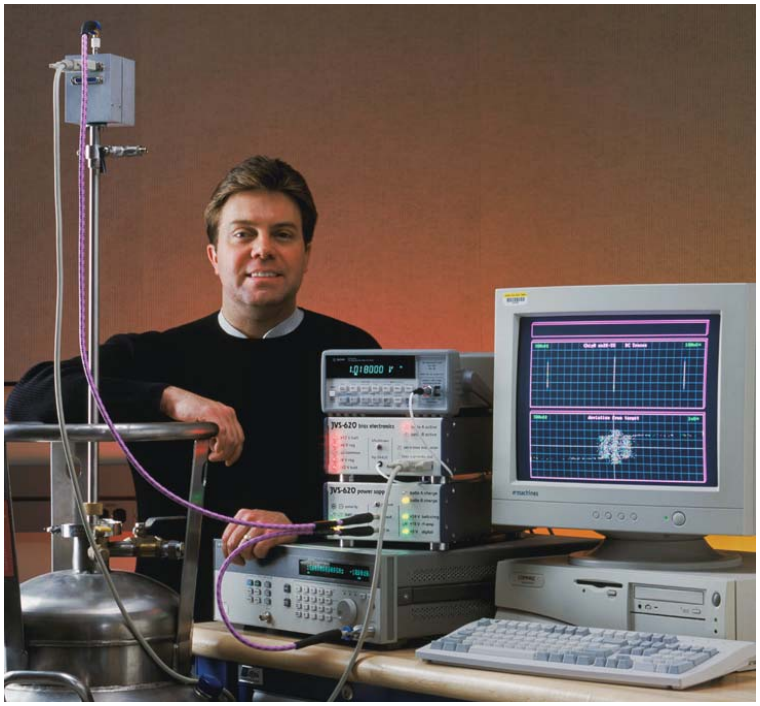

Fig. 3. Programmable voltage standard system. The low-thermal probe is in the Dewar at left. The electronics in the middle (from top to bottom) include a digital voltmeter, dc bias electronics, computer, and microwave source. The system is fully automated.

Since dissipation limits the number of junctions in a transmission line, multiple arrays are generally used to increase the total output voltage. Through the use of fixed-frequency microwave elements, such as quarter-wave taps and impedance transformers, the microwave power can be applied in *parallel* to smaller arrays in these circuits, while these smaller arrays can all be connected in *series* to create one large array with a high total output voltage. It is critical that the dc bias taps that connect to the arrays shall behave as a high impedance at the sine-wave frequency and as a superconducting short for dc; otherwise standing waves develop in the transmission line, reducing the uniformity of microwave power and operating margins for the arrays. This technique is used in both conventional voltage standards at 75 GHz[1, 2, 3] and in the programmable voltage standards at 16 GHz.[8]

Although the binary-sequence design for programmable voltage standards has proven adequate for *fast* and stable *dc* voltages, it is not practical for generating *ac* waveforms.[13] Since the switching time of each bias current driver is limited to about 1 μs, there is a significant uncertainty in the average voltage during this time interval. Thus the binary programmable voltage standard system is primarily used for applications that require stable and programmable dc voltages such as watt-balance experiments[14,15] and fast-reversed dc-to-dc comparisons.[16,17]

III. Josephson Arbitrary Waveform Synthesizer

In order to create a quantum-based ac Josephson voltage standard, the Josephson arbitrary waveform synthesizer was developed to exploit again the perfect quantization of Josephson junctions.[18,19,20] However, instead of being concerned with the constant-voltage steps of a sinusoidally driven junction, we consider the Josephson junction as a device that generates perfectly quantized voltage pulses. The time-integrated area of every Josephson pulse is precisely equal to $h/2e$. Digital synthesis techniques and precise control of the timing of every pulse allows the generation of voltage waveforms with unprecedented accuracy and stability. Knowledge of the pulse pattern and clock frequency precisely determines the frequency and amplitude of a synthesized sine-wave, or any

combination of harmonic frequencies. Simulations and experiments have shown that voltage noise and timing jitter, intrinsic to all semiconductor-switched digital code generators, create harmonic distortion in a synthesized waveform. These code generators are used to drive a Josephson array. Fortunately, the perfect area quantization of Josephson pulses recovers the low harmonic distortion of the original digital code that was created assuming perfect voltage levels and perfect timing. Using this technique and others, [21, 22, 23, 24] we have increased the output voltage of pulse-driven arrays by two orders of magnitude over the past 6 years. Most recently we have demonstrated synthesized arbitrary waveforms in arrays of 4096 junctions with peak voltages of 242 mV, and have reduced undesirable distortion-induced harmonics to 93 dB below the fundamental (–93 dBc) as shown in Fig. 4.

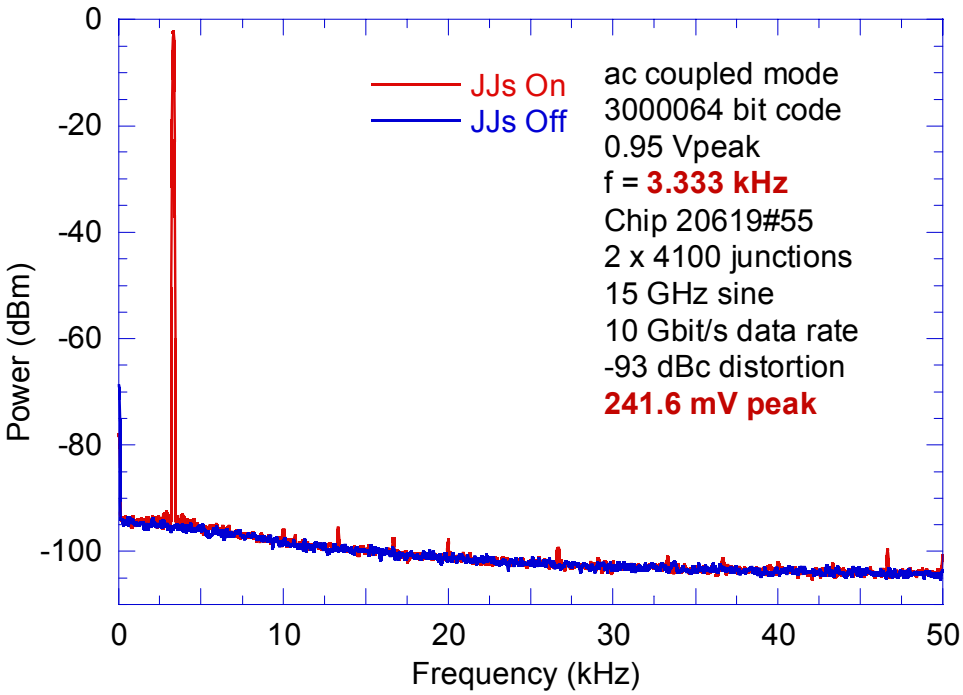

Fig. 4. Precision sine-wave synthesized by the Josephson arbitrary waveform synthesizer, showing a record 241.6 mV peak voltage with low harmonic distortion below –93 dBc (dB below the fundamental). To achieve this high voltage, two 4100-junction arrays are connected in series and biased with a 15 GHz microwave signal.

However, achieving practical voltages of 1 V to 10 V is even more difficult for waveform synthesis than for the programmable voltage standard. This is because the drive signal is broadband (dc to

15 GHz) and not single-frequency, as for the dc Josephson standards. Thus, quarter-wave filters and impedance transformers that control the single-frequency microwave signals for the dc systems cannot be used for the ac system. In order to achieve the record voltage shown in Fig. 4, improved filters and other techniques were used to combine in series the low-frequency signals from two arrays that are biased with two separate broadband waveforms. However, the best way to increase the output voltage for an array is the use of "lumped arrays" with nanoscale fabrication as described below.

IV. Lumped Arrays

In order to increase the output voltage for both programmable and ac voltage standards (which are limited by dissipation, broadband behavior, and in general, the physics of distributed arrays), we have begun developing nanoscale junctions for lumped arrays. [25, 26, 27] A lumped array is one in which all of the junctions are placed in the transmission line within a small fraction, say one-eighth to one-quarter, of the wavelength of the highest frequency of interest. Our goal is to make an array whose total impedance is equal to the 50 Ω transmission-line impedance. The output voltage would then be increased by about a factor of 8 for each array relative to current designs. These arrays would also be very efficient since most of the broadband power would not be wasted in a termination resistor, as in distributed-array circuits. Using the same arguments we used previously to optimize distributed arrays, if the maximum drive frequency is twice the characteristic junction frequency, then the maximum output voltage is $V_{max} = 2ZI_c$. For a 50 Ω transmission line and 10 mA critical current, this yields a 1 V maximum output voltage for a single array. Using our standard programmable array layout with 8 arrays and including two additional arrays (for a total of 10 parallel arrays), this approach could increase the output voltage of the programmable voltage standard output voltage to 10 V. It would also enable a 2 V peak output voltage for the Josephson arbitrary waveform synthesizer when two arrays are biased with a typical two-channel 10 Gbit/second semiconductor digital code generator.

The challenge for lumped arrays is that the junctions must be very close together. The effective dielectric constant for a coplanar waveguide on Si is 6.4 at our microwave frequencies. A 15 GHz drive frequency then has a quarter wavelength of about 2 mm. A critical current-resistance product of 31 μV and a critical current of 10 mA implies a junction resistance of 3.1 mΩ. Thus, a 50 Ω array would then require 16 100 series junctions spaced about 120 nm apart on the coplanar wavequide. This is a significant challenge, since the smallest SNS arrays fabricated using our present process have a junction spacing of 7 μm. These lumped array junctions will require nanoscale dimensions and subnanometer control to achieve sufficient uniformity.

The primary approach that we are now pursuing for making lumped arrays is a stacked-junction fabrication concept shown in Fig. 5. In this method, multiple barriers are deposited alternately with superconducting layers to create stacks of two-dimensional junctions. The lumped array in this geometry would have 320 stacks of 50 junctions each. The stacks would be 2 μm to 4 μm on each side and spaced 6 μm apart. Significant challenges of this approach will be to ensure that these 6 μm tall stacks have vertical sidewalls and to achieve a thick planarized insulator to create a smooth wiring layer.

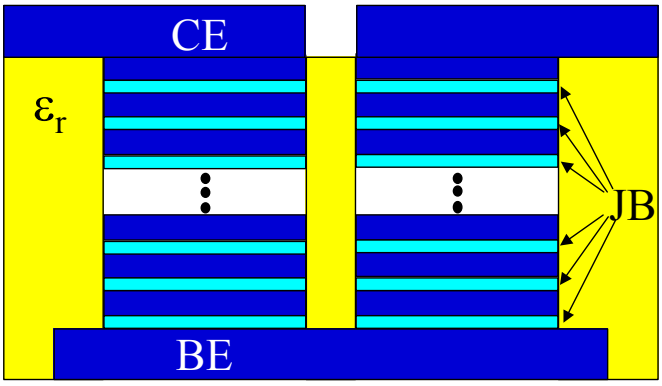

Fig. 5. Stacked SNS junction fabrication concept for lumped arrays. Counter electrode (CE), base electrode (BE), and other Nb superconductor between barriers are in blue. The junction barriers (JB) are in light blue. The insulating dielectric (ε_r) is yellow.

V. $MoSi_2$-Nb Stacked Junction Results

Recently, we have made significant progress toward stacked lumped arrays using $MoSi_2$ for the normal junction barrier.[27] Devices are fabricated starting with a Nb base electrode film followed by *in-situ* consecutive depositions of $MoSi_2$-Nb multilayers. The films are all dc sputtered and the thicknesses are controlled with subnanometer precision using computer-controlled shutters. To define the junction areas and create vertical sidewalls, the superconducting and normal barriers are etched together by reactive ion etching in a mixture of SF_6 and O_2. Sharp vertical etch profiles, together with uniform thickness of the deposited barrier, are essential to achieving uniform junction characteristics in a stacked geometry.

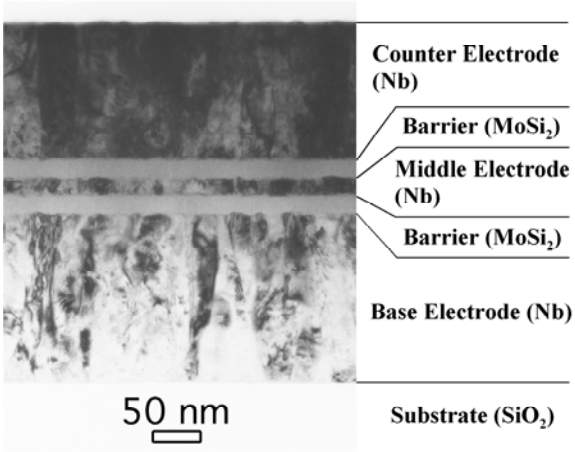

Fig. 6. Cross-sectional TEM image of a five layer Nb-$MoSi_2$-Nb-$MoSi_2$-Nb film. Each of the $MoSi_2$ barriers is 23 nm thick and the thickness of the middle Nb electrode is 20 nm.

Figure 6 shows a cross-sectional transmission electron microscope (TEM) image of a Nb-$MoSi_2$-Nb-$MoSi_2$-Nb pentalayer used to fabricate two-junction stacks. The interfaces are between the Nb and $MoSi_2$ films are flat and sharp, with only slight meandering at a length scale of 5 nm. Each of the $MoSi_2$ barriers is 23 nm thick and the thickness of the middle Nb electrode (ME) is 20 nm. These smooth interfaces and uniform thicknesses are critical to achieving good uniformity and reproducibility. This image shows that we can make uniform thin films of both Nb and $MoSi_2$, which is essential for making large multilayer stacks.

In order to increase junction density, we need to stack as many of these junctions as possible on top of each other. The number of junctions in a stack may ultimately be limited by the vertical dimension of the stack; thus it is important to keep the stacking unit as thin as possible. However, because the barrier is fixed by the designed characteristic voltage I_cR_n, the only parameter to minimize is the intermediate thickness of the Nb superconducting layers. In order to study this, we focused primarily on two-junction stacks and varied the thickness of the middle electrode between the normal barriers. If the thickness of a superconducting film is reduced below the superconducting coherence length ξ_s, the superconducting order parameter will be suppressed.

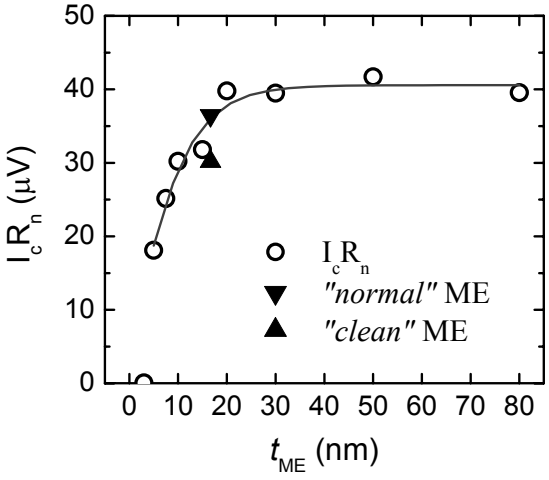

Fig. 7. Characteristic voltage I_cR vs. middle electrode thickness t_{ME} in two junction stacks at 4 K. The junction characteristic voltage is suppressed below a ME thickness of 20 nm. The line is drawn only as a guide to the eye.

A series of two-junction stacks were fabricated, all with barrier thicknesses of 23 nm. Each double-barrier stack behaves as two series-connected Josephson junctions, each having $I_cR \sim 39$ μV. When the middle electrode thickness t_{ME} is reduced, I_cR begins to be suppressed when $t_{ME} \sim 20$ nm, as shown in Fig. 7. In junctions with thinner ME's, the suppression of I_cR appears as a reduction in I_c, while R remains about the same because the barrier thickness and the junction geometry are the same for all

samples. This strongly suggests that the reduction in I_cR is due to suppression of the order parameter in the middle niobium electrode.

We also investigated the arrays of stacked junctions to ascertain the uniformity of the arrays and their behavior with taller stacks. Figure 8 shows current-voltage characteristics of two series-coupled arrays of 4100 triple-junction stacks (24,600 total series junctions) with 50 nm thick ME's. The microwave power was adjusted at each frequency to maximize the current range of the n=1 constant-voltage step. The current range over which the voltage remains constant is a measure of both the junction uniformity in the array as well as microwave losses due to dissipation in the array and out the bias taps.[11, 23] Flat steps were found for all three frequencies. With a 20 GHz microwave bias the circuit shows a flat step above 1 V (as expected) with a current range larger than 1 mA (see inset to Fig. 8). The rounding due at the edges of the steps is primarily due to microwave power dissipation by the junctions because there are a large number of junctions in each of these two arrays. Arrays with fewer junctions or shorter stacks show significantly less rounding and larger current ranges for the flat steps.

Similar uniform arrays were found with 20 nm thick ME's. Since the step voltages are correct for the total number of junctions and the current range of the steps are similar to those measured for arrays with thicker MEs, we conclude that the stacked junctions with 20 nm ME function exactly the same, both with and without microwaves, as stacked junctions with thicker ME. Using 20 nm ME thicknesses, 5-junction stacks would be possible using our existing process.

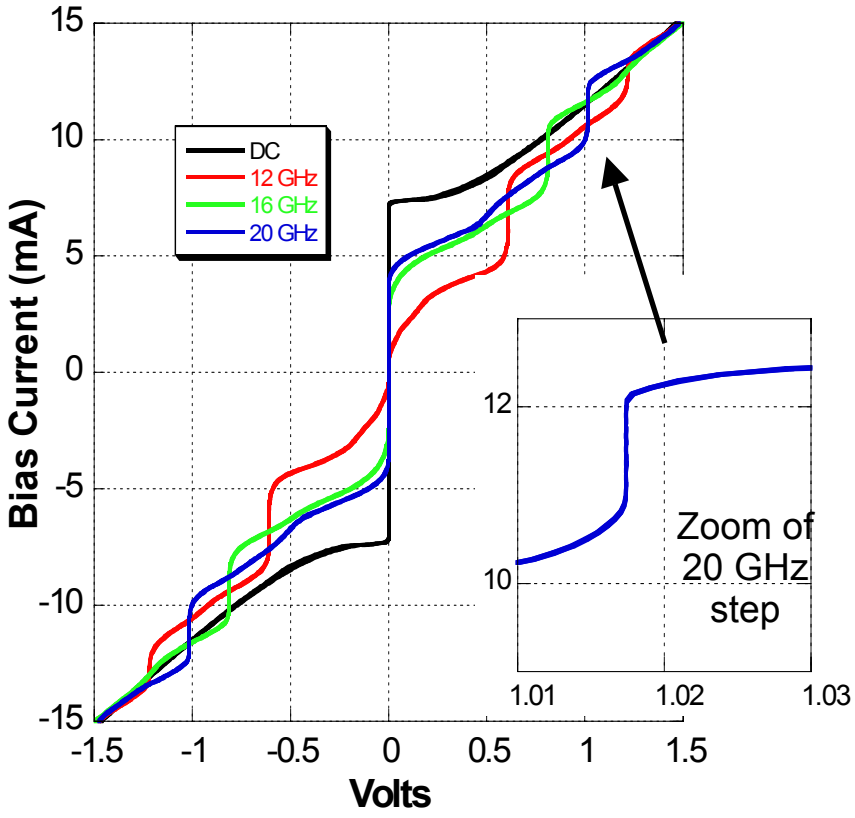

Fig. 8. Current-voltage characteristics of two series-connected 4100 triple-barrier junction arrays (24,600 total series junctions) with 50 nm ME's biased at different microwave frequencies. Inset shows the n=1 Shapiro step with a step height >1 mA for a 20 GHz microwave bias. The MoSi2 barrier etch is sufficiently uniform to have flat microwave steps from 12 to 20 GHz on two series-connected triple-barrier junction arrays with a total of 24,600 junctions.

Even for a ME thickness of 5 nm, we have measured flat Shapiro steps at the correct voltage for a stacked array. Flat steps appeared, even though I_cR is suppressed by more than 50% from the large ME value. This shows that, although suppression of the order parameter reduces I_cR for thin ME's, the junctions in the stacked array remain sufficiently uniform with a dramatically suppressed order parameter that they still have good microwave characteristics.

V. Conclusion

We have described the operation and performance of the programmable voltage standard and the Josephson arbitrary waveform synthesizer. We discussed the limitations of distributed arrays and

proposed the use of lumped arrays of Josephson junctions as a way to increase the output voltage and improve the performance of voltage standard systems. We described the stacked junction fabrication method and presented our latest results on $MoSi_2$-barrier stacked junctions. We showed that the middle Nb electrode sandwiched between two normal barriers can be reduced down to 20 nm before the electrical properties of the junction are changed. From these results we anticipate that we should be able to make stacks with up to 5 consecutive barriers that will allow us to make higher-voltage lumped arrays for the Josephson arbitrary waveform synthesizer and the programmable dc voltage standards. Significant further nanoscale fabrication development, including planarization and deep reactive ion etching for tall stacks, will be necessary to achieve our goal of 50 junction-tall stacks and lumped 50 Ω arrays.

Acknowledgments

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