Effects of interlayer electrode thickness in Nb/$(MoSi_2/Nb)_N$ stacked Josephson junctions

Yonuk Chong,[a] P. D. Dresselhaus, and S. P. Benz
National Institute of Standards and Technology, Boulder, Colorado 80305

J. E. Bonevich
National Institute of Standards and Technology, Gaithersburg, Maryland 20899

(Received 22 November 2002; accepted 12 February 2003)

Dense, vertically stacked Josephson junction arrays are being developed for voltage metrology applications. We present measurements of the uniformity and reproducibility of Nb/$(MoSi_2/Nb)_N$ vertically stacked junctions that clarify the superconducting properties of the middle Nb superconducting electrode. Middle electrode thicknesses down to 20 nm have shown minimal suppression of the superconducting order parameter as measured through the critical current density. Even with a middle electrode thickness of 5 nm, excellent junction uniformity has been observed as demonstrated by the measurement of large Shapiro steps when the arrays are biased with microwaves. We also discuss the role of the superconducting coherence length in these arrays of high-density junctions. [DOI: 10.1063/1.1566797]

Superconductor–normal–superconductor (SNS) Josephson junctions have been successfully used in programmable voltage standards[1–3] and in the Josephson arbitrary wave form synthesizer.[4,5] Series arrays of junctions are required to increase the output voltage to practical levels. A major goal of the National Institute of Standards and Technology (NIST) voltage standard research is to increase the linear junction density in these arrays. Arrays of higher density lead to both higher output voltages in programmable systems and better broadband frequency characteristics for ac voltage standards.[6] The method that has demonstrated the highest junction densities, while maintaining good uniformity and reproducibility, is the vertically stacked junction geometry.[7–9] Recently, it has been shown that $MoSi_2$ provides a stable, reproducible, normal-metal barrier for stacked junctions.[7] This reproducibility enables precise targeting of the critical-current density (J_c) for specific applications, and the high resistivity of $MoSi_2$ allows larger-sized junctions at a given characteristic voltage, $V_c = I_c R_n$, where I_c is the critical current and R_n is the normal resistance.

In order to increase junction density, we need to stack as many junctions as possible on top of each other. The number of junctions in a stack may ultimately be limited by the vertical dimension of the stack; thus it is important to keep the stacking unit as thin as possible. Because the barrier thickness is fixed by the designed V_c, the only parameter to minimize for a given barrier material is the intermediate thickness of the superconducting layers. In this letter, we investigate the properties of two-junction stacks by varying the thickness of the middle electrode (ME) between the normal-metal barriers.

Figure 1 shows the V_c versus $MoSi_2$ barrier thickness at 4 K. These data were summarized from the measured characteristics of arrays of single junctions and a few arrays of two- and three-junction stacks with intermediate-electrode thicknesses greater than 50 nm. The data were collected from more than 10 different runs over a period of 6 months. Figure 1 shows that the value of V_c depends only on the barrier thickness and not on any other process variable. It also shows excellent run-to-run reproducibility of the characteristic voltage.

The on-chip uniformity of the critical current can be inferred from the sharpness of the dc current–voltage characteristics of a series array of junctions and the current range of the microwave-induced Shapiro steps.[7] The normal coherence length ξ_n of the barrier is estimated to be 3.5 ± 0.1 nm, and the characteristic voltage has an expected dependence on barrier thickness d, of $V_c(d) = (4 mV)(d/\xi_n)\exp[-d/\xi_n]$.[10] The prefactor is about 5.5 times larger than that for PdAu junctions, whereas the normal–metal coherence length is shorter.[11] This excellent reproducibility, accuracy in targeting V_c, and on-chip uniformity enabled us to perform detailed studies of the middle electrode in two-junction stacks.

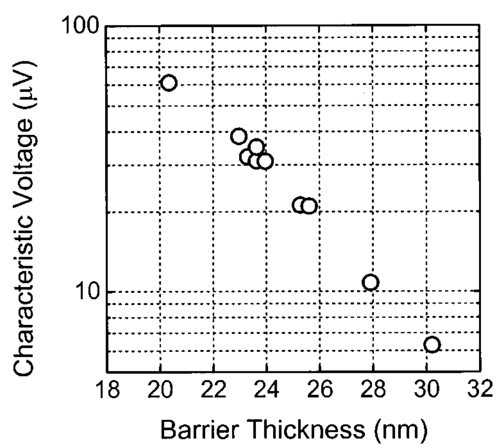

FIG. 1. Characteristic voltage ($V_c = I_c R_n$) at 4 K for a range of $MoSi_2$ barrier thicknesses. The data are from arrays of single junctions and a few arrays of two- and three-junction stacks with electrode thicknesses greater than 50 nm.

[a]Electronic mail: yonuk@boulder.nist.gov

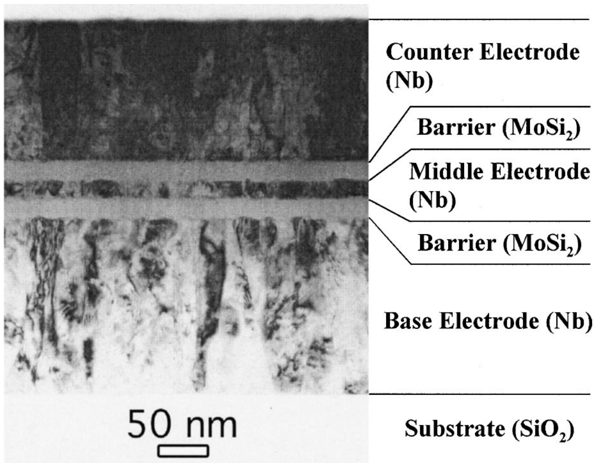

FIG. 2. Cross-sectional TEM image of a five layer Nb/$(MoSi_2/Nb)_2$ film. Each of the barriers is 23 nm thick and the middle electrode thickness is 20 nm.

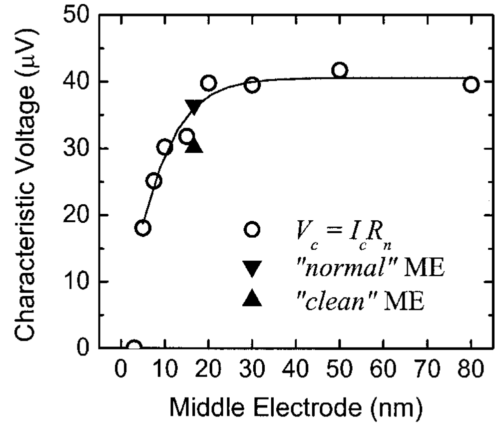

FIG. 3. Characteristic voltage $V_c = I_c R_n$ vs middle electrode (ME) thickness t_{ME} in two-junction stacks at 4 K. At ME thicknesses of less than 20 nm, the characteristic junction voltage is suppressed. The line is drawn only as a guide for the eyes. The "normal" ME was prepared with the usual process, and the "clean" ME was prepared immediately after depositing 10 Nb films in sequence.

Devices were fabricated starting with a Nb/$MoSi_2$ multilayer deposited *in situ* by dc magnetron sputtering. The $MoSi_2$ film resistivity is 650 $\mu\Omega$ cm at room temperature and increases by ~30% when cooled to 4 K. No superconducting transition was observed for temperatures down to 50 mK. To define the junction areas, superconducting electrodes and normal barriers were etched together by reactive ion etching in a SF_6 and O_2 mixture. Sharp vertical etch profiles, together with uniform thickness of the deposited barrier, are essential to achieving uniform junction characteristics in a stacked geometry.[7]

Figure 2 shows a cross-sectional transmission electron microscope (TEM) image of a Nb/$MoSi_2$ multilayer used to fabricate the junction stacks. The interfaces are flat and sharp, with only slight meandering at a length scale of 5 nm. The Nb film is highly textured in the [011] direction,[12] whereas the $MoSi_2$ films are amorphous. These smooth interfaces and uniform thicknesses are the main reasons why we can achieve good uniformity and reproducibility for V_c.

A series of two-junction stacks were fabricated, all with barrier thicknesses of 23 nm. Each double-barrier stack functions as two series-connected Josephson junctions, each having $V_c \sim 39\ \mu V$. As the ME thickness t_{ME} is reduced, V_c begins to become suppressed when $t_{ME} \sim 20$ nm, as shown in Fig. 3. In junctions with thinner MEs, the suppression of V_c appears as a reduction in I_c, while R_n remains constant because the barrier thickness and the junction geometry are the same for all samples. This strongly suggests that the reduction in V_c is due to order-parameter suppression in the middle niobium electrode.

In order to make the ME as thin as possible, it is desirable to have a dirty middle electrode with a short coherence length.[13] In order to qualitatively see the difference between dirty and clean Nb films, we intentionally prepared two multilayers with "normal" and "clean" middle electrodes. The normal ME was prepared with the usual process, but with a slightly shorter Nb presputter step; the clean ME was prepared immediately after depositing 10 Nb films in sequence, after which we expect that the residual gases are more effectively gettered than for the normal ME multilayer. The results are shown in Fig. 3 by triangles. With the ME fixed at 17 nm, the normal ME sample approximately follows the same trend as our previous data, while the clean ME sample has a V_c that is reduced by an amount that is significantly larger than our run-to-run variation. In addition, if the film order is factored into the previous data for thin ME samples, the films deposited at the end of a long deposition sequence tend to have lower V_c values than the usual trend (e.g., the data at 15 nm). This implies that our ordinary process produces "moderately dirty" Nb films with a comparatively short coherence length. These data confirm our expectation that cleaner Nb films will cause further suppression of V_c for the same ME thickness.

There are several effects that can cause this suppression of V_c for a thin ME. If the thickness of a superconducting film is reduced below the superconducting coherence length ξ_s, the superconducting order parameter will be suppressed.[14] The superconducting order parameter may also be suppressed in the ME due to the proximity to the normal metal. It is expected that if, due to the proximity effect, significant suppression of the superconducting order parameter occurs on the superconducting side of the S/N interface, then size effects will become important as the ME thickness becomes less than $2\xi_s$ (ξ_s from each interface).[15] From Fig. 3, we assume that the critical minimum ME thickness is 20 nm, the minimum thickness at which nonsuppressed V_c is observed. If this critical thickness is $2\xi_s$, we can estimate that ξ_s is about 10 nm in our Nb films, which is a value typical of those reported in the literature for thin Nb films.[16] However, from $H_{c2}(T)$ measurements, the measured coherence length of our Nb film at 4 K was 17.5 ± 0.5 nm.[17] Since the suppression parameter given by Kupriyanov and Lukichev,[18] $\gamma = \rho_s \xi_s / \rho_n \xi_n$, is estimated to be ~0.03 for the Nb/$MoSi_2$ interface, the suppression of the order parameter in the ME caused by the proximity effect with the barriers on both sides is expected to be small. Hence the measured values of V_c decrease only when the ME is less than $\sim \xi_s$, because the suppression of the order parameter at the S/N interface is negligible on the superconducting side. Furthermore, the measured interface resistance is negligible in our junctions ($< 2 \times 10^{-10}\ \Omega\ cm^2$, extrapolated from R_n times the junc-

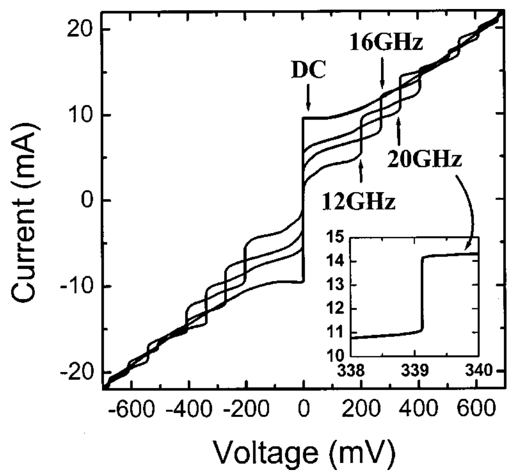

FIG. 4. Current–voltage characteristics of a 4100-stack double-barrier array (8200 series junctions) with 20 nm ME thickness biased at different microwave frequencies. These curves are qualitatively the same as those of thicker ME samples. The inset shows the $n=1$ Shapiro step with ~ 3 mA step height with a 20 GHz microwave bias.

tion area versus barrier thickness), so this high S/N interfacial transparency will not cause discontinuity of the order parameter. This insensitivity to interface properties also partially explains and contributes to the excellent run-to-run reproducibility of the $MoSi_2$-barrier junctions.

Figure 4 shows current–voltage characteristics of an array of 4100 double-junction stacks (8200 total series junctions) with a 20 nm thick ME. The microwave power was adjusted at each frequency to maximize the range of current of the $n=1$ constant-voltage step. The current range of these steps is a measure of the junction uniformity in the array as well as microwave losses due to dissipation in the array.[5,19] With a 20 GHz microwave bias the array shows a flat Shapiro step over a current range of 3 mA. Since the step voltages are correct for the total number of junctions, and the current range of the steps is similar to those measured for arrays with thicker MEs, we conclude that the stacked junctions with 20 nm ME function exactly the same, both with and without microwaves, as stacked junctions with thicker ME.[7]

Even for a ME thickness of 5 nm, we have measured flat Shapiro steps at the correct voltage for a 2000 junction stacked array. Flat steps appeared even though V_c is suppressed by more than 50% from the large ME value. This shows that, although suppression of the order parameter reduces V_c for thin MEs, the junctions in the stacked array remain sufficiently uniform to have good microwave characteristics.

$MoSi_2$-barrier stacked junctions are promising for integrated nonhysteretic Josephson device applications. Since $MoSi_2$ can be dry etched with Nb, multijunction stacks can be made with good uniformity. We successfully demonstrated a stacked Josephson junction array with a 20 nm ME thickness without a reduction in characteristic voltage or a change in microwave response. Our results suggest that this critical ME thickness is on the order of the superconducting coherence length ξ_s, and that by making the Nb film moderately dirty and reducing ξ_s we will be able to fabricate multiple stacked junctions with superconducting interlayer thicknesses on the order of ξ_s. Our results may be related to some of the observations in NbN/TiN_x stacked junctions.[8,20] Following these results, we anticipate that we will be able to make stacks with up to five consecutive barriers with our existing process in which the total stack thickness is limited by the vertical etch process.

The authors thank S. Ruggiero for valuable discussions, R. Goldfarb and T. Stauffer for $H_{c2}(T)$ measurements, and C. Burroughs for measurement systems. This research was supported in part by Office of Naval Research Contract Nos. N00014-00-F-0154, 01-F-011, and 02-F-0004.

[1] S. P. Benz, C. A. Hamilton, C. J. Burroughs, T. E. Harvey, and L. A. Christian, Appl. Phys. Lett. **71**, 1866 (1997).
[2] R. Pöppel, D. Hagedorn, T. Weimann, F.-I. Buchholz, and J. Niemeyer, Supercond. Sci. Technol. **13**, 148 (2000).
[3] H. Yamamori, M. Itoh, H. Sasaki, A. Shoji, S. P. Benz, and P. D. Dresselhaus, Supercond. Sci. Technol. **14**, 1048 (2001).
[4] S. P. Benz, C. J. Burroughs, and P. D. Dresselhaus, IEEE Trans. Appl. Supercond. **11**, 612 (2001).
[5] S. P. Benz, C. J. Burroughs, and P. D. Dresselhaus, Appl. Phys. Lett. **77**, 1014 (2000).
[6] S. P. Benz, P. D. Dresselhaus, and C. J. Burroughs, IEEE Trans. Instrum. Meas. **50**, 1513 (2001).
[7] P. D. Dresselhaus, Y. Chong, J. H. Platenberg, and S. P. Benz, IEEE Trans. Appl. Supercond. (to be published).
[8] H. Yamamori, M. Ishizaki, M. Itoh, and A. Shoji, Appl. Phys. Lett. **80**, 1415 (2002).
[9] A. M. Klushin and H. Kohlstedt, J. Appl. Phys. **77**, 441 (1995).
[10] H. Sachse, R. Pöpel, T. Weimann, F. Müller, G. Hein, and J. Niemeyer, *Applied Superconductivity*, Inst. Phys. Conf. Ser. No. 158 (Institute of Physics, Bristol, 1997), pp. 555–558.
[11] S. P. Benz, Appl. Phys. Lett. **67**, 2714 (1995).
[12] T. Imamura and S. Hasuo, Appl. Phys. Lett. **58**, 645 (1991).
[13] In the dirty limit ($\xi_0 > l$), the coherence length is given by $\xi \sim \sqrt{\xi_0 l}$, where ξ_0 is the superconducting coherence length in the clean limit, and l is the normal-state electron mean free path. The zero-temperature coherence length of niobium in the clean limit is known to be 38 nm; see, for example, B. W. Maxfield and W. L. McLean, Phys. Rev. **139**, A1515 (1965).
[14] L. H. Greene, A. C. Abeyta, I. V. Roshchin, I. K. Robinson, J. F. Dorsten, T. A. Tanzer, and P. W. Bohn, in *Spectroscopic Studies of Superconductors*, edited by I. Bozovic and D. van der Marel, Proc. SPIE **2696**, 215 (1996).
[15] P. G. de Gennes, *Superconductivity of Metals and Alloys* (Benjamin, New York, 1966).
[16] S. T. Ruggiero, T. W. Barbee, Jr., and M. R. Beasley, Phys. Rev. B **26**, 4894 (1982).
[17] E. Helfand and N. R. Werthamer, Phys. Rev. **147**, 288 (1966).
[18] M. Yu. Kupriyanov and V. F. Lukichev, Sov. Phys. JETP **67**, 1163 (1988).
[19] S. P. Benz and C. J. Burroughs, IEEE Trans. Appl. Supercond. **7**, 2434 (1997).
[20] M. Ishizaki, H. Yamamori, A. Shoji, S. P. Benz, and P. D. Dresselhaus, IEEE Trans. Appl. Supercond. (to be published).