Negative Bias Temperature Instability of Deep Sub-Micron *p*-MOSFETs Under Pulsed Bias Stress

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Abstract --- Negative bias temperature instability (NBTI) and Positive bias temperature instability (PBTI) of p-MOSFETs with 2.4 nm thick oxide films were studied. The ΔVth interface trap generation of p-MOSFET at DC and AC bias stresses with frequency up to 500 KHz were measured. Additional tests were also conducted under unipolar and bipolar bias stresses with varied stress on and off times. The ΔVth and interface trap generation of p-MOSFET were observed to be significantly reduced for pulsed bias repetition frequencies greater than 10 KHz. However, ΔVth of PBTI was almost independent of the bias stress frequency. These results suggested that there are different mechanisms for NBTI and PBTI phenomena, and the reliability specifications of NBTI could possibly be relaxed under certain pulsed operation conditions.

Keywords --- **Negative bias temperature instability, frequency dependence, *p*-MOSFET**

I. INTRODUCTION

Negative Bias Temperature Instability (NBTI) has become a serious reliability problem in deep sub-micron *p*-MOSFETs as device dimensions are continually scaled down, [1, 2, 3]. It has been reported that the threshold voltage shift (ΔV_{th}) of *p*-MOSFETS due to NBTI degradation becomes the limit of device lifetime with ultrathin oxides [4]. NBTI-enhanced hot carrier effect in *p*-MOSFETs was also reported [5]. Several models have been proposed for the mechanism of NBTI.

A. Hole trapping model

The hole trapping model is based on avalanche hole injection measurements on unstressed MOS capacitors and the NBTI tests [6, 7, 8]. This model proposes that the negative midgap voltage shift, which is believed to be a measure of the change of positive oxide charge without the contribution from interface states, is due to the filling of intrinsic hole traps. All the positive charge generated by preceding negative bias stress can be removed by the positive bias stress. But the exact mechanism for hole injection into the oxide is still unknown.

B. Thermally assisted electron tunneling model

The thermally assisted electron tunneling model was established by Breed [9, 10]. According to this model, the neutral or positive centers, which cause the charge trapping, are located near the interface in the oxide. Under negative bias stress, the centers are excited. The electrons in the excited states then tunnel into empty states of the conduction band of the silicon. This process is a thermally assisted tunneling process.

C. Electrochemical reaction model

Several authors [1, 11, 12, 13] proposed the electrochemical reaction model, which has been accepted by many researchers in recent years. This model explains the NBTI effect in terms of electrochemical reactions. Fig. 1 shows the schematic diagram of this model.

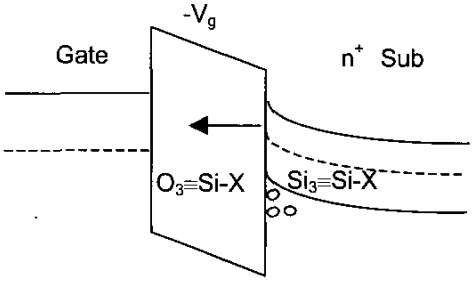

Fig. 1 The schematic diagram of electrochemical reaction model

Basically, there are two reactions in this model.

$$Si_3 \equiv Si - X + A \Leftrightarrow Si_3 \equiv Si^* + B$$

$$O_3 \equiv Si - X + C + p^+ \Leftrightarrow O_3 \equiv Si^+ + B$$

$$B_{\text{int}erface} \Leftrightarrow B_{bulk} \quad \text{(Diffusion)}$$

Si_3≡Si-X is a trivalent silicon, a defect near the interface. X, A, B, and C are unknown neutral species. Si_3≡Si^* is a neutral trivalent silicon backboned by three other silicon atoms, functioning as an interface trap near the interface. O_3≡Si^+ is a positively charged species, serving as a positive charge in the oxide.

The first reaction accounts for the interface trap generation. The trivalent silicon reacts with A and produces the interface trap and B. There are different definitions for A and B. Some suggest A as a hydrogen ion and B a hydrogen atom. But there are also some suggestions in different ways. The second reaction is for the fixed oxide charge generation reaction. There are a number of suggestions for the C species as well. The diffusion of the product B would produce the phenomenon of NBTI. There are also some other variant electrochemical reaction models, which explain the NBTI effect with

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one electrochemical reaction. It is clear that regardless of mechanism, holes certainly play an important role in the NBTI effect.

Most of the NBTI studies dealt with DC stress conditions [1-9]. In this work, we studied the NBTI and Positive BTI (PBTI) of p-MOSFETs under pulsed bias stress conditions, since most of the signals in digital CMOS circuits are AC signals.

II. EXPERIMENTAL TECHNIQUES AND EVALUATION METHODS

Surface channel p-MOS transistors with a 2.4 nm thick gate oxide from a standard CMOS 0.16 um technology are used in this study. The channel lengths are 0.12 um and 0.18 um. Constant bias stresses were conducted with DC, unipolar pulsed, and bipolar voltage sources with source, drain, and substrate of the p-MOSFET grounded as shown in Fig. 2.

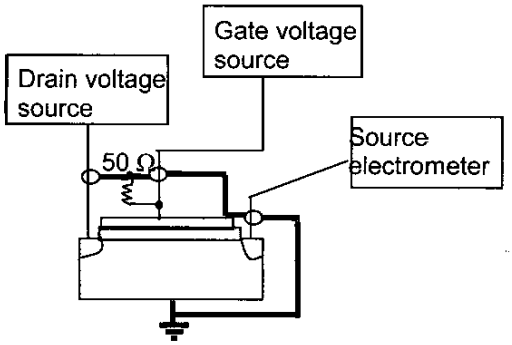

Fig. 2. The experimental set up for NBTI study.

The stress was periodically interrupted, and the drain current was measured with the gate voltage swept. The voltage waveforms were applied and monitored by an oscilloscope. Three kinds of waveforms were used to study NBTI in this work. Those waveforms are shown in Fig. 3.

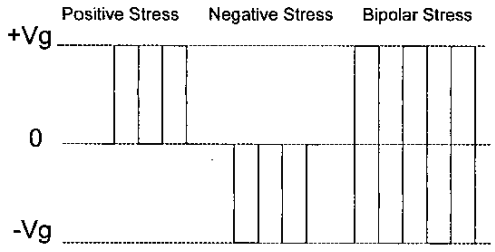

Fig. 3 The waveforms of stress voltages, V_g=3V.

From the drain current vs. gate voltage plots, the threshold voltage could be extracted using the linear extrapolation method in the linear region [14]. The threshold voltage shift was defined as:

$$\Delta V_{th}(i) = V_{th}(i) - V_{th}(0).$$

$V_{th}(i)$ is the i^{th} threshold voltage, and $V_{th}(0)$ is the initial threshold voltage.

The charge pumping method is an efficient way to evaluate the interface trap generation [15]. The interface trap generation was extracted from the I_{cpmax} using the equation:

$$D_{it} = \frac{\log_{10} e}{2qkTA} \times \frac{\Delta Q_{it}}{\Delta \log f}$$

$$Q_{it} = \frac{I_{cp}}{f}.$$

A is the gate area of the MOSFET; f is the pulse frequency to the gate; I_{cp} is the charge pumping current; and q, k, and T have their conventional meanings.

Since D_{it} is proportional to ΔI_{cpmax}, ΔI_{cpmax} reflects the change of the interface trap density.

III. EXPERIMENTAL RESULTS AND DISCUSSIONS

A. Threshold voltage shift

The frequency dependence of the NBTI phenomenon was evaluated. The ΔV_{th} at DC and AC bias stresses with pulse repetition frequencies up to 500 KHz were measured. Fig. 4a shows the ΔV_{th} under negative unipolar voltage stress for different frequencies.

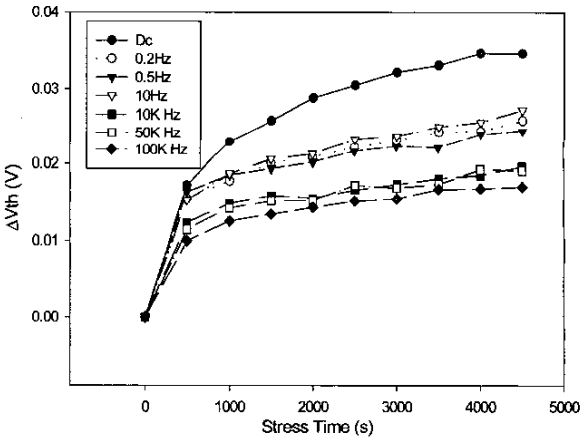

Fig. 4 (a). ΔV_{th} vs. stress time, under negative unipolar voltage stresses with different frequencies, V_{stress}=-3.0V, T=150 °C.

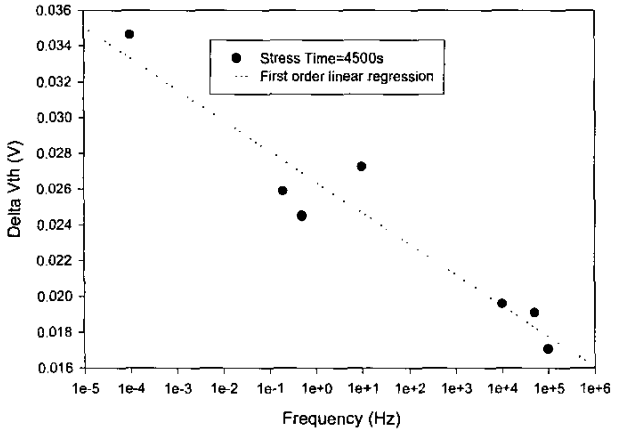

Fig. 4 (b). ΔV_{th} vs. frequency, under negative unipolar bias stresses, V_{stress}=-3.0V, T=150 °C.

Figs. 4 (a, b) suggested that under the NBTI stress condition, ΔV_{th} exhibits significant frequency dependence. It is clear that ΔV_{th} increases as the frequency decreases and approaches a DC condition. It has been suggested that ΔV_{th} is an indicator of the fixed oxide charge in SiO_2. These data indicate that there are less net positive charges in the silicon dioxide under higher frequency bias conditions. During the stress off time, some of the charges can be detrapped or neutralized.

Saturation (drive) current (Ion) is an important factor in determining the speed of CMOS circuits. Fig. 5 shows the degradation of ion vs. stress time curves under negative unipolar bias stresses with repetition frequencies from 0 KHz to 100KHz.

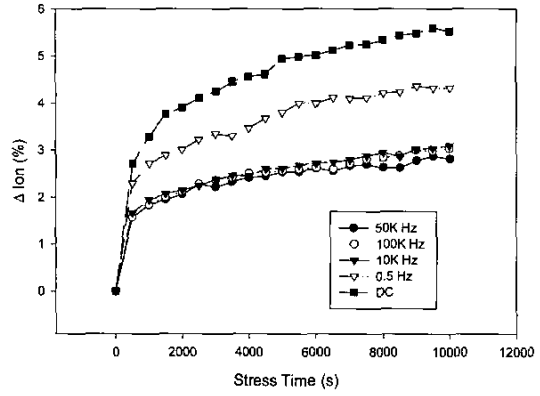

Fig. 5. ΔIon vs. stress time, under different unipolar bias stress. Vg=Vd=-1.5V, T=150 °C.

It is clear that the degradation of saturation current also exhibits a similar frequency dependence as threshold voltage shift under the negative bias stress conditions.

It has been reported that different from NBTI, which includes both interface state generation and positive charge formation, the PBTI only results in interface state generation, and the final saturation level is fixed by the number of defects in the device [16]. However, there are also some other models, which proposed a mechanism that is ionic in nature and due to protons [14]. Similar to the NBTI, we evaluated the frequency dependence of the PBTI. Fig. 6 shows ΔV_{th} under positive unipolar voltage stress for different frequencies. The ΔV_{th} shows almost no change with different frequencies. Thus, the PBTI doesn't exhibit a frequency dependence in our study, which may confirm the idea that there are different mechanisms for NBTI and PBTI.

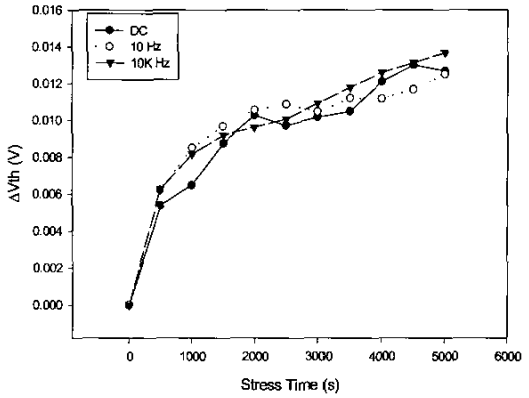

Fig. 6. Delta Vth vs. stress time, under positive unipolar voltage stresses with different frequencies, V_{stress}=3.0V, T=150 °C.

It has been reported that the positive bias stress could remove the positive charge in oxide generated by previous negative bias stress [6]. However, in our experiment, we did not observe this kind of recovery effect. On the other hand, the bipolar stress even worsened the ΔV_{th} caused by preceding negative bias stress. Fig. 7 compares the ΔV_{th} under positive unipolar, negative unipolar, and bipolar pulsed bias voltage stresses with a repetition frequency 10 KHz. Note that the ΔV_{th} under bipolar stress is even larger than the sum of negative and positive bias stresses. Thus, bipolar stress does not result in less defect generation, which was observed in TDDB (Time Dependent Dielectric Breakdown) studies [17].

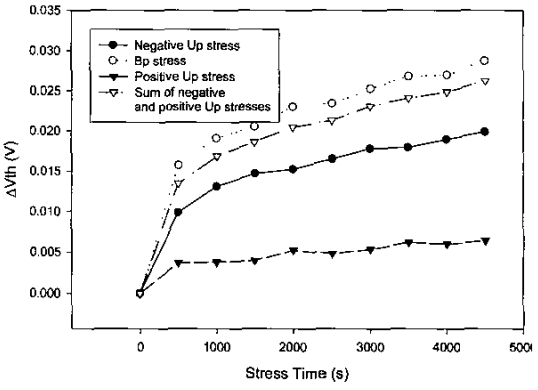

Fig. 7. Comparison of ΔV_{th} under different bias stress conditions with a 10KHz repetition frequency.

B. Interface trap generation

As the size of devices shrink, the interface trap generation due to NBTI becomes more serious [12]. It has shown that the interface trap generation and the fixed oxide charge generation has a one by one or at least a linear relationship. Based on this idea, we

evaluated the frequency dependence of interface trap generation with AC negative bias stress using the standard charge pumping method.

Fig. 8 shows ΔI_{cpmax} change under negative bias stress for *p*-MOSFETs with a standard charge pumping method. It is clear the interface trap generation is less under pulsed negative bias stress than negative DC stress. However, there is not much difference for positive bias stress. This is similar to the threshold voltage shift situation. But this is not sufficient to confirm the linear relation between the ΔV_{th} and interface trap generation.

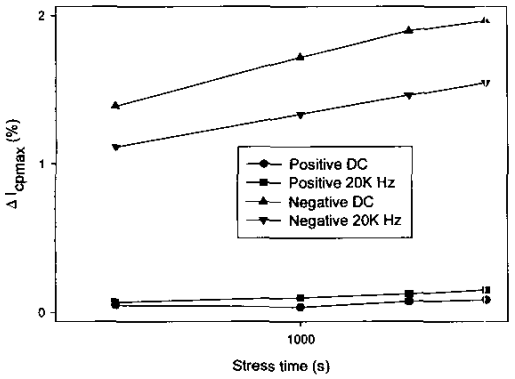

Fig. 8. ΔI_{cpmax} change under negative bias stress for *p*-NBTI with standard charge pumping method.

C. Time constants

As we discussed before, the ΔV_{th} and interface trap generation for p-NBTI under NBTI condition exhibit a similar frequency dependence. Figs. 9(a) and (b) show ΔV_{th} under negative unipolar voltage stress with varying stress on and off times.

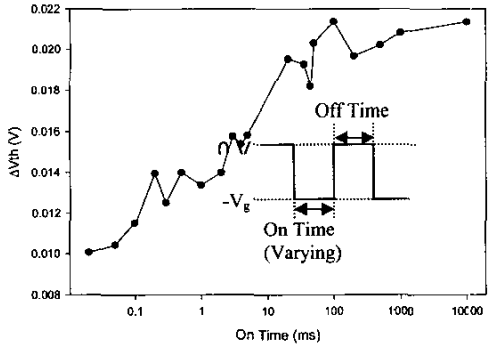

Fig. 9 (a). ΔVth under negative unipolar stress with constant off time and different on time, Vstress=-3.0 V, T=150 °C.

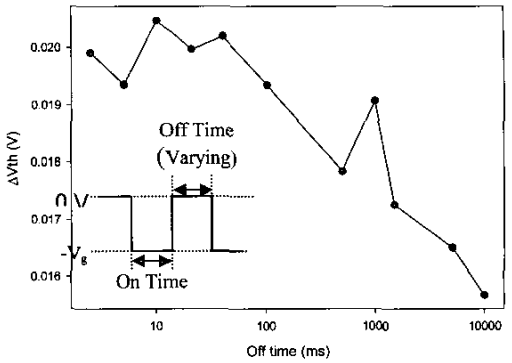

Fig. 9(b). ΔV_{th} under negative unipolar stress with constant on time and different off time, Vstress=-3.0 V, T=150 °C.

According to the Figs. 9(a) and (b), there are similar time constants in the whole process, which are on the order of 100 ms in our study. This also confirms from another aspect that there is a strong frequency dependence for the NBTI phenomenon.

The exact mechanism for this frequency dependence is still unknown. If the electrochemical reaction model is true, the product B, which diffuses away to the gate and oxide interface from the Si and SiO_2 interface, would diffuse back during the stress off time. During another test the ΔV_{th} only reduced about 30 % when we let the stress off time be as long as 24 hours. This may indicate that only part of B can diffuse back. If the hole trapping model is valid, then the trapped holes could be detrapped or neutralized during the stress off time. Then, this process is electric field dependent. More work is needed with different test temperatures and electric fields to confirm the models and the exact species involved in the process.

IV. CONCLUSIONS

The threshold voltage shift and interface generation of NBTI in sub-micron *p*-MOSFET were studied. A significant frequency dependence was observed for NBTI stress conditions. However, there is almost no frequency dependence for PBTI stress conditions. This may also suggest different mechanisms for the NBTI and PBTI phenomenon. In addition to the frequency dependence, certain time constants related to NBTI were observed.

Different from the reported effect of positive bias stress, which removed the positive oxide charge generated by the proceeding negative bias stress, the following positive stresses made the NBTI worse, as shown by the bipolar stress experiment.

Even though the exact mechanism of the NBTI effect is still unknown, the frequency dependence of NBTI is obvious. Possibly, part of the fixed oxide charge and interface traps are removed or neutralized during the stress off time. This may lead to the reduced NBTI phenomenon, which may allow NBTI reliability specifications to be relaxed.

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6. QUESTIONS AND ANSWERS

Q: What is the usage of the 50 Ω resistor in the experimental set up?
A: The waveforms in our study were square waves. We need this resistor to keep the shape of the waveform.

Q: Did you use dual gate devices?
A: Yes, the p-MOSFET we used in this study had p-polygate.

Q: So, there was NBTI phenomenon in both p-MOSFET and n-MOSFET?
A: Yes, we did observe the NBTI phenomenon in n-MOSFET.

Q: Have you done TDDB test on these devices?
A: No, we didn't.