4 K Cryocooler Implementation of a DC Programmable Voltage Standard

Charles J. Burroughs, Robert J. Webber, Paul D. Dresselhaus, and Samuel P. Benz

***Abstract*—NIST and HYPRES, Inc. have been collaborating to develop a 1 Volt DC programmable Josephson voltage standard (PJVS) that operates on a closed-cycle refrigerator. The goal of this work is to construct a platform that will allow the chip to work at 4 K without liquid helium, thereby making the system more convenient and eliminating the need for users to handle liquid cryogens. In our existing PJVS systems, the Josephson chip temperature is the only parameter that is not computer controlled. The addition of a cryocooler will allow automated warming and cooling of the Josephson device and enable an intrinsic voltage standard system in which every control function is automated, and the only required user input is the desired output voltage. The cryocooler package is designed to allow PJVS chips to be easily interchanged between the cryocooler and liquid helium cryoprobes.**

***Index Terms*—Cryocooler, dc voltage, Josephson voltage standard, SNS Josephson junctions.**

I. Introduction

PROGRAMMABLE Josephson voltage standard (PJVS) systems offer several advantages over conventional Josephson voltage standard (JVS) technology for certain applications. In particular, PJVS systems provide intrinsic voltage stability, higher noise immunity (50 times greater), comprehensive automation, and rapid programmability. The PJVS chip consists of 13 arrays of SNS (superconductor/normal-metal/superconductor) Josephson junctions, and operates at a temperature of 4 K. The voltage across each junction is given by the equation $V = f/K_j$, where f is the applied microwave frequency (16 GHz), and K_j is the Josephson constant 483 597.9 GHz/V. The chip contains a total of 32 768 Josephson junctions connected in series, so the total output voltage range is ± 1.1 V. The complete chip design and principles of operation have been previously described [1], [2].

These PJVS devices are integrated into fully automated systems [3] that operate as a 9-bit (including sign) precision D/A (digital-to-analog) converter where the output voltage at every level is known with Josephson accuracy. The system computer measures all chip operating parameters, and then performs automated measurements 24 hours a day (usually as an integrated instrument in a larger measurement system) while controlling all periodic local system functions. In order to have a completely turnkey system, the only remaining tasks are to automate the cooling of the chip and eliminate the liquid helium which requires monthly user intervention. The final development phase for these systems is to install the PJVS chip in a new cryostat utilizing a cryogen-free, closed-cycle refrigerator (CCR) at 4 K. The present cryostat design is an extension of the 4 K cryocooled 10 V conventional JVS that HYPRES has previously developed and demonstrated [4]. A complementary effort into implement a NbN-based programmable voltage standard chip on a 10 K cryocooler is being pursued through a collaboration between AIST and NIST [5].

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II. CCR Cryostat Design

Nb-based PJVS chips from NIST have never before been operated on a cryocooler, so one key feature of the new cryostat is that it uses the same method of electrical connection to the chip as our existing liquid helium cryoprobes. This direct compatibility allows a chip to be repeatedly installed, measured, and removed using either apparatus, thus allowing us to evaluate any differences in performance between the two measurement systems. The chip is permanently mounted on a small copper block that both systems use to hold and align the chip to the electrical connections. In the cryocooled package, the copper block also performs the function of extracting the heat generated by the chip. Both the cryopackage and the cryoprobes use electrical connections made using a BeCu (beryllium-copper) printed-circuit board with gold-plated spring-finger contacts.

Fig. 1 shows the completed cryopackage mounted on the 4 K stage of the CCR. The CCR employs a two-stage refrigerator utilizing the Gifford-McMahon cooling cycle with 5 W of cooling power at the first stage (60 K), and nominally 250 mW of cooling at the second stage (4 K) [6]. Magnetic shielding is provided by two cylindrical mu-metal shields that completely surround the chip package except for 4 copper posts that extend through the shields to provide the thermal link to the 4 K stage. Electrical connections to the chip consist of 30 copper dc bias wires (each 0.127 mm in diameter, and nominally 1 Ω or less), and one 2.2 mm diameter semi-rigid coaxial cable (stainless-steel outer-conductor, BeCu inner-conductor, 3 dB insertion loss) that delivers the 16 GHz microwave drive. The coax connects to a 50 Ω coplanar waveguide on the fingerboard so that all electrical connections (dc and microwave) are made to the front side of the chip via the fingerboard. The chip and its permanent back-side copper block are bolted to the copper base-plate of the cryopackage. Below we describe a number of key requirements for the cryopackage design.

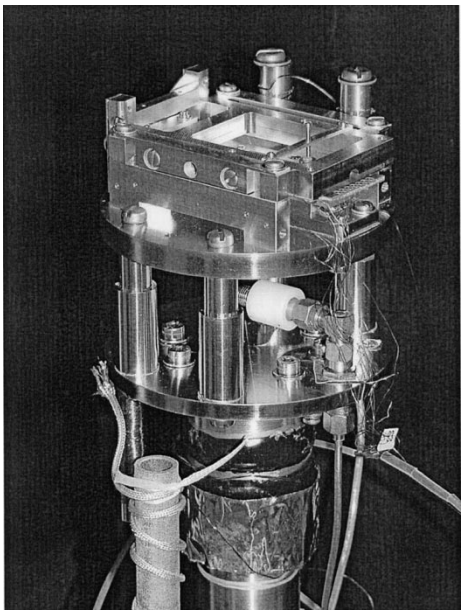

Fig. 1. Photograph of the cryopackage attached to the 4 K second stage of the CCR. The two magnetic shield cans are not shown.

TABLE I
CALCULATED HEAT LOADS TO THE 4 K SECOND STAGE

Static Unpowered Contributions	Joule Heating Contributions	Heat Load (mW)
dc wiring conduction		44.4
Coaxial cable conduction		10
60 K shield radiation		4.6
Room temp radiation through shield holes		10
	dc bias currents (dissipation on-chip)	15
	dc bias currents (wire dissipation)	0.7
	rf-power dissipation in coaxial cable	9
	rf power dissipation on-chip	15
		108.7 mW *TOTAL*

Calculations of the various heat loads to the 4 K second stage. The total estimated heat load is 108.7 mW, consisting of 69 mW of static unpowered contributions and 39.7 mW of joule heating when the chip is actively biased.

A. Chip Temperature

In order for the chip to operate at the correct 4 K temperature, we must ensure that the total required cooling power does not exceed the cooling capacity of the second stage. It is also important that the thermal conductance from the chip to the second stage is sufficient to remove the on-chip heat effectively. For this particular chip, there are two primary heat sources: (1) static contributions from the thermal conduction of the electrical connections to the chip, which include the 30 dc wires and the semi-rigid coaxial line, and (2) on-chip power dissipation of approximately 30 mW, about half of which occurs from microwave power dissipation in the 50 Ω termination resistors, and the other half from the array dc bias current. Quantitative estimates of the total heat load to the 4 K second stage are summarized in Table I. The total heat load of 108.7 mW is well within the 250 mW specification for the cryocooler.

B. Chip Alignment

One of the most important considerations in this cryopackage design is the precision mechanical alignment required for the 16 GHz microwave launches. The microwave input to the chip consists of 4 coplanar waveguides that connect to 4 matching coplanar waveguides on the fingerboard. Optimum performance of the Josephson chip is achieved when the relative alignment between the on-chip waveguides and fingerboard waveguides is better than ± 0.025 mm. Much of the mechanical configuration of the cryopackage was dictated by this constraint. This alignment requirement was satisfied by placing several 0.35 mm holes in the fingerboard directly over the on-chip coplanar waveguide launches. The hole size was chosen to match specific features on the chip so that aligning the chip within ± 0.010 mm is relatively easy when using this visual alignment scheme.

The obvious challenge with this visual method is that it is performed when the cryopackage and chip are at room temperature, and the alignment must be maintained when the cryostat is cooled to 4 K. The apparatus must behave in such a way that even though all of the pieces experience different amounts of thermal contraction, the overall alignment of the chip to the fingerboard remains fixed. This was accomplished by supporting the fingerboard at only 2 points using the mechanical configuration shown in Fig. 2. The first support is directly above the chip, where the fingerboard connects to a thin (0.25 mm) flexible BeCu plate. This X–Y flex-plate allows movement in the z-axis, but no movement in the X–Y plane. Alignment is maintained because the thermal contraction of different components in the cryopackage occurs without moving the center-point of the X–Y flex-plate with respect to the chip. A spring presses down on the center-point from above and applies a controlled amount of force to bring the fingerboard in contact with the chip. This scheme provides excellent alignment and insensitivity to thermal contraction in the X, Y, and Z dimensions. However, another support is required to eliminate torque on the fingerboard caused by the coaxial cable or by the assembly process.

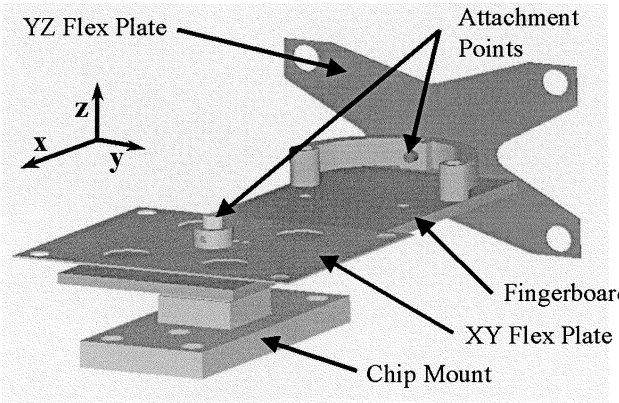

Fig. 2. Diagram of the chip-to-fingerboard alignment mechanism for the PJVS cryopackage. The attachment point on the X–Y flex plate is designed not to move when the cryopackage is cooled to 4 K, even though all of the mechanical components experience different amounts of thermal contraction.

TABLE II
MEASURED THERMOMETER TEMPERATURES

Thermometer Location	Mean Temperature (K)	Temperature Oscillation (K)
Base Plate	3.84	± 0.08
Chip Mount	4.01	± 0.04

Measurements of thermometers at various locations in the CCR cryostat for the system at thermal equilibrium. The temperature oscillation occurs approximately once per second each time the CCR performs one cooling cycle. The unexpected result that the chip mount temperature is oscillating less than the base-plate appears to be real, and is probably caused by thermal resistance between the copper chip mount and the copper base plate.

Such rotational movement could misalign or even break the chip, so a Y–Z flex-plate has been added to secure the far end of the fingerboard to prevent movement in the Y and Z directions, but still allow thermal expansion along the X axis.

Tests of this alignment scheme indicate that once the chip has been aligned and all the parts are clamped into position, the cryopackage can be repeatedly cooled and the alignment of the chip to the fingerboard remains the same each time it is measured at room temperature. Of course, at 4 K the only way to confirm that the alignment has not changed is to measure the operating parameters for the entire PJVS chip. At this time, preliminary measurements of individual arrays suggest that the alignment method is working properly. Some additional features of the alignment mechanism that are not visible in Fig. 2 are, (1) adjustment screws and reaction springs that allow the alignment to be conveniently adjusted under a microscope, and (2) a chip nest that is attached to the fingerboard which acts as a "bump stop" to prevent excessive x or y movement of the fingerboard which could damage the chip.

III. EXPERIMENTAL MEASUREMENTS

The first tests of the complete CCR cryostat were to verify its ability to cool the Josephson chip to the correct operating temperature of 4.0 K to 4.2 K. We used two independent methods to determine the temperature of the Josephson device and the degree to which its temperature oscillates as the cryocooler cycles (approximately once every second). First, there are temperature sensors built into the system at key locations: one on the copper chip mount, one on the base-plate that holds the chip-mount assembly, and one on the 4 K second stage of the CCR. The temperatures of the first two of these sensors were measured when the system was at thermal equilibrium, and are listed in Table II. These values remain approximately the same with and without the microwave and dc bias currents to the array.

The second method of determining the chip temperature is to observe the critical current of a known segment of the SNS Josephson array. These Nb/PdAu/Nb junctions have a critical current that depends strongly on temperature, and our experimental measurements and theoretical estimates for this temperature dependence give roughly 11 mA/K near 4 K. The critical current for a 2048 junction array segment was measured to be $I_c = 17.6$ mA in liquid helium (4.0 K at our altitude). When this same device is measured in the CCR cryostat, the mean critical current is $I_c = 19$ mA which indicates that the chip

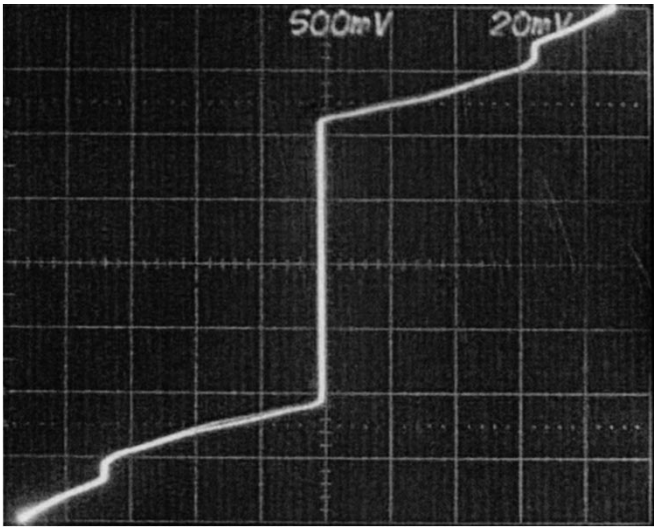

Fig. 3. The measured I–V characteristic of an individual segment of the 1 Volt programmable Josephson chip operating on the CCR. This segment containing 2048 junctions produces the step at 67 mV with 10 mW of microwave power at 16 GHz. The horizontal scale is 20 mV/div, and the vertical scale corresponds to 5 mA/div (due to the 100 Ω sense resistor). The small offset and gain error visible is due to the oscilloscope.

temperature on the CCR is approximately 3.92 K (*i.e.* 4.0 K $-(19.0–17.6)$ mA/11 mA/K). Furthermore, the measured oscillation of the critical current due to the cycling CCR is roughly ±0.3 mA, which corresponds to a temperature fluctuation every cycle of about ±0.03°K using the same method.

Both of these methods have uncertainties that limit their accuracy for the absolute temperature to a few tenths of a kelvin, so the two methods agree within their uncertainty. The uncertainty for the values of the temperature oscillations are much smaller (0.02 K or less for both methods) because they are relative measurements. These results confirm that the CCR cryostat is able to hold the Josephson device at the correct operating temperature with an oscillation of less than ±0.05°K. This performance meets the essential conditions required for operation of the PJVS chip on the cryocooler. Another fundamental requirement that seems to be working well is the magnetic shielding. The chip has been cooled a number of times, and there has been no evidence of trapped magnetic flux in the PJVS chip due to ambient magnetic fields or the magnetic components in the regenerator near the 4 K second stage of the CCR.

We also have preliminary data that demonstrates operation of the chip under both microwave and dc bias. The same 2048-junction array segment (the second largest array on the chip) was driven with microwaves at 16 GHz with an estimated power of 10 mW delivered to the chip at 4 K. Figs. 3 and 4 show the current-voltage $(I$–$V)$ curve of this array segment with a constant voltage step in its I–V curve at the correct voltage, 67 mV. The shape of this I–V characteristic is approximately the same as that measured in liquid helium at the same power level, and it demonstrates that the CCR and cryopackage are performing as required. The applied power was limited by the microwave generator, and we expect that when the microwave power is increased with an amplifier, the larger cells of the Josephson array will also exhibit flat steps allowing the entire device to be operated at the full ±1.1 V output range.

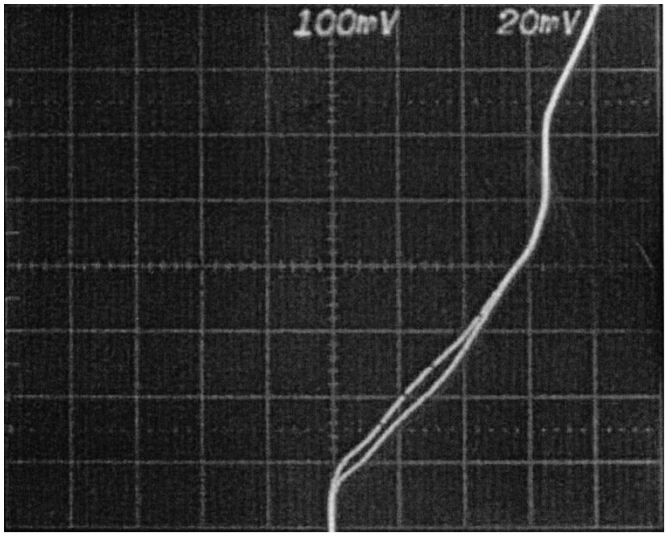

Fig. 4. Photograph showing 5 × higher vertical resolution of the same I–V curve shown in Fig. 3. The step at 67 mV is flat over a current range of approximately 1 mA. The horizontal axis is 20 mV/div, and the vertical axis is 1 mA/div.

IV. Conclusion

A new CCR cryostat and cryopackage that accommodates 1 Volt PJVS chips has been designed, built, and tested. The system has successfully met the key design requirements, which include a removable and quickly interchangeable chip-mounting configuration, adjustable precision chip alignment, cooling of the chips to the correct 4 K operating temperature with oscillations on the order of ± 0.05 K, and magnetic shielding to prevent trapping of magnetic flux in the Josephson junctions. Preliminary voltage measurements on an individual array segment of a PJVS chip show a flat step at 67 mV over a current range of 1 mA. It is expected that increasing the applied microwave power will result in larger current ranges and also increased output voltages when the largest array segments can be shown to have flat voltage steps. Also, chips with critical currents closer to the nominal value of 10 mA will have larger steps even with the low microwave power used for measurements in this paper.

From these results, we conclude that there are no fundamental technical barriers to prevent the operation of a complete PJVS system using this CCR cryostat and removable chip package. Due to their stability, noise immunity, and high degree of automation, PJVS systems are becoming integral components in applications such as mechanical/electrical watt-balance experiments [7], [8], evaluation of thermal voltage converters [9], metrology triangle experiments [10]. Integrating this Josephson technology with cryocoolers will allow us to provide more convenient and fully automated systems in the future, and it will also allow them to be used in locations where liquid cryogens are unavailable or inconvenient.

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