a-Axis $YBa_2Cu_3O_{7-\delta}$ /Au Interface Conductance-Voltage Characteristics

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***Abstract*—Conductance-voltage characteristics of interfaces between a-axis $YBa_2Cu_3O_{7-\delta}$ (YBCO) thin films and gold are presented. When the gold counter electrode is deposited *in-situ*, the junctions have a specific interface resistivity in the 10^{-9} Ω-cm^2 range, about an order of magnitude lower than nominal *in-situ*, c-axis YBCO/noble-metal junctions. As with nominal c-axis YBCO/noble-metal junctions, there is clear evidence at T = 4 K for a peak in the conductance at low bias. In addition, a dip in the the middle of the broad peak structure was resolved. It appears to be a feature unique to the a-axis YBCO/Au interface.**

I. Introduction

Low-resistance contacts to high-temperature superconductor (HTS) thin films are desirable for HTS electronics. Gold (Au), silver (Ag) and other noble metals have been used for this purpose, due to their low oxygen affinity [1]. Depending on the nature of the processes, the contact material may be deposited either *in situ* or *ex situ*. Due to the significant mismatch in electron density of states between YBCO and noble metals, there is a boundary resistance characteristic of the interface, even under ideal interface conditions. Because of its sensitivity to structural defects, the YBCO/noble metal interface is far from ideal, generally characterized by a non-ohmic, bias-dependent interface resistance. The value of this resistance at zero-bias, multiplied by the contact area and expressed in units of Ω–cm^2, gives the specific interface resistivity ρ_c.

We have done extensive measurements of interface resistance for a variety of thin-film HTS/noble metal systems [2-5]. Our major findings are the following: (1) For c-axis YBCO/Ag interfaces, the lowest ρ_c was obtained with *in-situ* processing and was in the low 10^{-8} Ω×cm^2 range[5]; (2) For ex-situ contacts, ρ_c generally is in the range of 10^{-4} Ω–cm^2 or higher, which can be reduced to the 10^{-7} Ω–cm^2 range by annealing in oxygen; (3) The conductance-voltage characteristics of the interface conduction have, in general, a parabolic shape at high bias, indicative of tunneling processes; and (4) A zero-bias conductance peak (ZBCP) is usually observed.

In this paper we report our results on YBCO/noble metal interfaces fabricated from a-axis YBCO films and *in-situ* deposited Au. Due to their longer coherence length in the perpendicular direction, a-axis YBCO films offer the potential for fabricating vertical HTS Josephson junctions. With these high quality a-axis YBCO films we address two questions: (1) Given the strong anisotropy in transport properties of YBCO thin films, what is the achievable interface conductance in the *in-situ* a-axis YBCO/Au system? and (2) Does the ZBCP exist in this system as well as in the c-axis YBCO systems?

II. Experiments

The a-axis YBCO films with an *in-situ* Au cap layer are grown at the University of Maryland. The details of film growth and microstructural characterization have been reported previously [6]. The films are made by standard multitarget pulsed laser deposition. Briefly, we start by depositing a $PrBa_2Cu_3O_{7-x}$ (PBCO) layer, 40 nm thick, on an (100) oriented $LaSrGaO_4$ substrate, at a substrate temperature of 660°C. The PBCO layer serves as a seed layer for the subsequent a-axis growth of YBCO. The substrate temperature is raised to 800 °C by the end of the PBCO deposition, at which point we switch to the YBCO target. Our typical YBCO thickness is 250 nm. Following YBCO deposition, a 200 nm thick Au layer is deposited, at about 200 °C, to complete the *in-situ* a-axis YBCO/Au structure. The films are patterned at the NIST Boulder Laboratory using photolithographic processes similar to those reported in [2] and [5]. In particular,

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it is necessary to carry out a frame etch before depositing the MgO insulating layer in order to eliminate the spreading resistance of the in-situ Au layer, as was emphasized in [5]. We report results obtained on two similarly prepared films, whose superconducting properties are given in Table I.

Our measurement circuit is designed to simultaneously record the I-V curve of a junction and its first derivative. The derivative was taken using a lock-in technique. Due to the low interface resistance encountered in these devices, a resolution of 5 $\mu\Omega$ is required to reveal structures in the conductance-voltage characteristics. This is achieved by properly matching impedances using low-noise preamplifiers and, sometimes, by averaging data over a number of scans.

TABLE I

T_c AND J_c OF THE a-AXIS YBCO FILMS STUDIED

Sample	T_{c0} (K)	ΔT_c (K) (10%-90%)	J_c (77 K, // b-axis) ($\times 10^6$ A/cm^2)
Z1355	84.8	0.8	0.23
Z1429	85.9	0.6	0.48

III. Results

A. *Specific Contact Resistivity*

For a uniform interface, ρ_c is independent of the contact area and gives a measure of the quality of the interface. Figure 1 displays ρ_c vs. the width of four square junctions on each of the two chips listed in Table I. First, they are all in the range of 10^{-9} Ω–cm2, which is about 10 times smaller than the value of ρ_c of *in-situ* c-axis YBCO/Ag(or Au) contacts. Second, an approximately linear dependence of ρ_c on the junction width, L, is discernible. We argue that this dependence is a consequence of the finite sheet resistance of the metal (Au) counterelectrode. Our contact geometry is designed to minimize this effect. Nevertheless, the width W of the metal contact is slightly larger than the junction size to ensure proper alignment. This causes current to enter the junction not only through the front edge but through the side edges as well [7]. Consequently there is a contribution from the sheet resistance. Assume that the lateral extension of currents near the sides of the junction is d; this additional resistance is approximately $R_s(d/L)$, where R_s is the sheet resistance. Then the relation $\rho_c=\rho_{c0}+R_s(d/L)$ exists between the intrinsic interface resistivity ρ_{c0} and the measured resisativity, ρ_c.

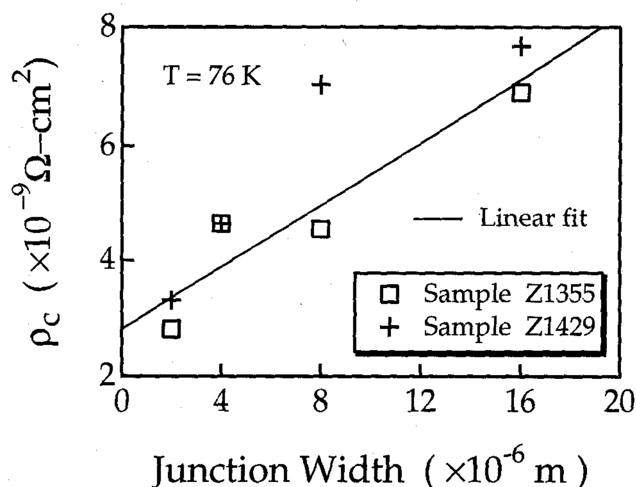


Fig. 1. Specific contact resistivity vs. junction width. There are four square junctions with sides from 2 µm to 16 µm on each chip. The linear dependence is due to the finite sheet resistance of the Au counterelectrode.

Physically d may be limited either by the difference in W and L: d ~ (W–L)/2, or by the quantity $(\rho_{c0}/R_s)^{1/2}$, whichever is larger[7]. Assuming for simplicity that d is the same for all four junctions, we do a linear fit to the data in Fig. 1. From its extrapolation and slope, and from the measured Au sheet resistance of 0.027 Ω per square (at 76K), we obtain ρ_{c0} = 2.8×10^{-9} Ω–cm^2, and d ~1.0 µm. While for our 2 µm junction (W–L)/2 is indeed only about 1 µm, for larger junctions d will certainly be limited by the quantity $(\rho_{c0}/R_s)^{1/2}$, which at 77 K is about 3.3 µm. Thus the fit is rather crude. However, we conclude from this exercise that, independent of the detailed assumptions used in the fit, the value of ρ_c obtained from the 2 µm junction is closer to the true interface resistivity.

B. *Conductance Structures at Zero-Bias*

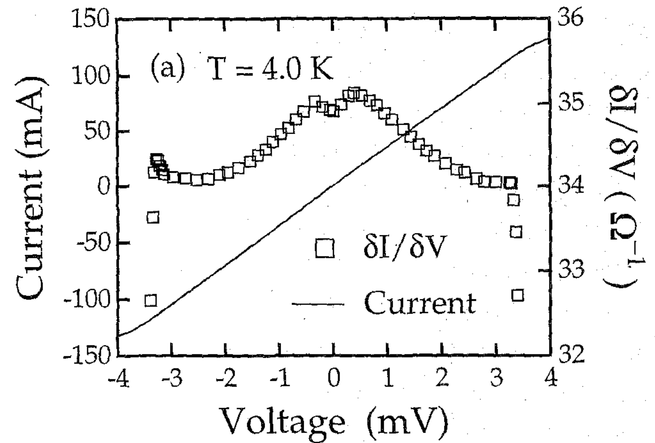
Figure 2(a) shows the voltage dependence of current, on the left axis, and dynamic conductance G = dI/dV, on the right axis, of a 4 µm × 4 µm junction on sample Z1429, measured at T = 4 K. The I-V characteristics are almost ohmic for bias current up to about 120 mA, at which point there is a significant increase in resistance. Concomitantly there is a precipitous drop in dI/dV. Given the thickness of the film and the base electrode width, we infer that at 120 mA the base electrode current density had just exceeded the J_c of our a-axis film (we determined J_c by measuring a test structure on the

same chip). When the base electrode was driven normal, its resistance quickly dominated over the junction interface resistance. Due to the smallness of the latter (about 30 mΩ at 4 K) the corresponding "threshold" voltage across the interface is about 3 mV. Therefore voltage range in which the intrinsic interface conductance behavior can be observed is quite limited. Nevertheless one cannot fail to notice the unusual structures exhibited in the dI/dV data, shown in more detail in Fig. 2(b).

Unlike the broad peak centered at about zero bias usually seen for c-axis YBCO/noble-metal interfaces, the conductance-voltage characteristic of our a-axis YBCO/Au contact splits into two peaks, one for each polarity of bias, almost symmetrically located with respect to the dip at zero bias. Although the overall shape of the conductance-voltage characteristic is reminiscent of the ZBCP previously reported for c-axis YBCO/noble-metal contacts, the dip in the middle is unique to the a-axis YBCO/Au interface. For the data in Fig.2 (b), the depth of the dip, as measured from the conductance minimum at zero bias to the anticipated maximum if the dip had not occurred, is 0.28 mΩ, that is, about 1% of the zero-bias resistance.

Also, as bias increases toward the J_c threshold voltage of 3 mV, the conductance starts to level off and even increase (cf. Fig. 2 (a)). We think that this behavior is not intrinsic to the interface conductance. Rather, it is a precursor of the superconducting-to-normal transition in the base electrode. In other words, the conductance may have continued to fall for bias beyond 3 mV had the base electrode remained superconducting, until the ZBCP is fully developed. Taking the conductance value at 3 mV bias, we found that [G(0)–G(3 mV)]/G(0) = 3.7%. All the ZBCP's observed in c-axis YBCO/noble-metal interfaces appear to be 3 mV to 5 mV wide and have peak-to-peak heights about 4% to 20% of the zero-bias conductanc; our data therefore seem to suggest that the broad peak structure in conductance is the same as those observed in c-axis YBCO interface systems.

For all the junctions whose interface resistance can be conveniently measured with our apparatus, we observed a broad peak with a dip in the middle. This characteristic thus appears to be generic to the a-axis YBCO/Au interface.



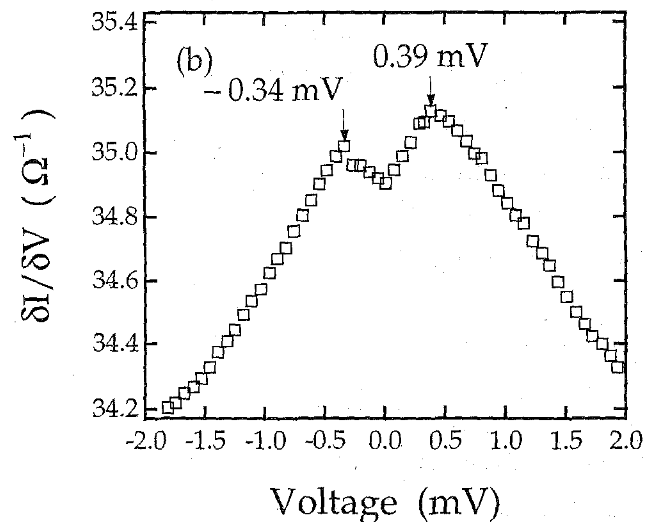


Fig. 2(a) Current and dI/dV vs. bias voltage of a 4 μm×4 μm junction measured at T = 4. 0 K. Intrinsic interface conductance behavior is limited to bias voltage less than 3 mV. (b) dI/dV data of panel (a) displayed on finer scale, showing an overall enhancement of dI/dV at small bias, with a pronounced dip at zero voltage.

C. Temperature Dependence

Figure 3 shows the temperature dependence of the zero-bias conductance of the device shown in Fig.2. Except for the region close to the T_c of the base electrode superconductor, the measured resistance is predominantly that of the interface. After an initial decrease at the superconducting transition, the resistance levels off at 65 K, then gradually increases as temperature decreased to about 35 K. At that point it starts decreasing significantly. After reaching a minimum at about 8 K , it departs from the trend and increases again. In a narrow temperature span from 8 K to 4 K the resistance increases by 0.11 mΩ. In comparison, the same amount is gained from the gradual increase between 65 K and 35K.

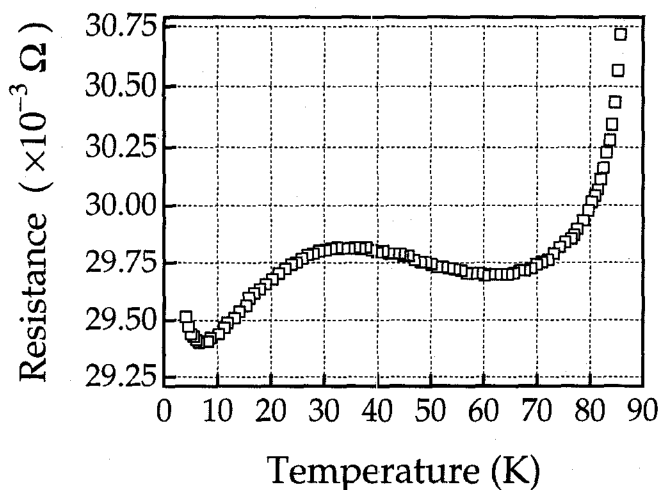


Fig. 3 Resistance at zero bias vs. temperature of the device shown in Fig.2, below the transition temperature of the base electrode.

Note that for the magnitude of the ac current used, the r.m.s. value of voltage across the junction is no greater than 6 μV, much smaller than the width of the dip in the conductance characteristic. Therefore we were measuring the true zero-bias conductance.

IV. Discussion

A. The Broad Conductance Peak at Zero-Bias

Due to the limit imposed by the critical current of the superconducting base electrode, as mentioned earlier, we are unable to measure the full range of the conductance peak. The available data, however, seem to suggest that the broad peak structure observed here is the same as the ZBCP in c-axis YBCO/noble-metal interfaces, which has been extensively studied by our group at NIST [2,3] and other groups [8, 9].

This observation also lends support to the idea that the nominally c-axis transport in YBCO is facilitated, and may even be dominated, by conduction along the a-b direction, due to anisotropic properties of the material and its particular growth mode [10].

B. The Dip in the Middle of the Conductance Peak

An intriguing feature is the dip in the middle of the more familiar broad conductance peak. As mentioned in section III B, the depth of the dip is about 0.28 mΩ. Now in the temperature dependence of the zero bias resistance shown in Fig. 3, if the trend between 30 K and 10 K continues to lower temperatures, the resistance at 4 K would have been about 0.25 mΩ lower than the actual value. This may suggest that the dip in the conductance at zero bias is correlated with the anomalous increase of the zero bias resistance for temperatures below 8 K. However, when we measured conductance-voltage characteristics at different temperatures, the dip structure persisted even for temperatures up to 30 K. Its origin remains elusive at present.

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