Critical Current Control and Microwave-Induced Characteristics of $(NbN/TiN_x)_n/NbN$ Stacked Junction Arrays

M. Ishizaki, H. Yamamori, A. Shoji, S. P. Benz, and P. D. Dresselhaus

***Abstract*—Stacked double and triple Josephson junctions with NbN electrodes and TiN_x barriers were fabricated for the next-generation 10 V programmable Josephson voltage standard. Because of difficulties in the growth of uniform junctions in a stack with a constant barrier thickness, a stack with carefully engineered thicknesses was grown that exhibited uniform junction properties. The junction arrays on these chips were biased with microwave power at 16 GHz resulting in constant-voltage steps consistent with the total number of junctions in the array, including the multiple junctions in the stacks. The steps had a current range greater than 1 mA at 4.2 K.**

***Index Terms*—Digital-to-analog converter, Josephson junction, sputtering, stacked junctions, voltage standard.**

I. Introduction

THE CONVENTIONAL voltage-standard system [1]–[3] used in the national standards institutions worldwide typically generates 10 V with an accuracy of 1 part in 10^9, operates at liquid helium temperature of 4.2 K, takes from seconds to a couple of minutes to achieve a stable output, and has constant-voltage step heights on the order of 0.01–0.1 mA. The step height is small in order to avoid chaotic behavior.

The next-generation voltage-standard system may have such properties as a) accurate voltages programmable up to 10 V, b) constant-voltage step heights of at least 1 mA, and c) the capability of operating with a compact cryocooler. In order to realize such a next-generation system, we have been developing NbN-based digital-to-analog (D/A) converters [4], [5] for programmable Josephson voltage standards [6]–[8]. In a previous paper [4], we reported successful operation of a 5-bit D/A converter composed of 4096 $NbN/TiN_x/NbN$ junctions at 10 K with a step height over 1 mA. We also recently succeeded in fabricating an 8-bit D/A converter composed of 32 768 $NbN/TiN_x/NbN$ junctions and operated it in a compact cryocooler [5]. The 8-bit D/A converter can generate programmed voltages up to 1 V. Demonstration of a 10 V programmable Josephson voltage standard has been reported that uses 69 120 $Nb/AlO_x/Al/AlO_x/Nb$ junctions [9]. We plan to develop a 10 V programmable voltage standard chip using $NbN/TiN_x/NbN$ junctions in a compact cryocooler system. However, the total number of junctions in the chip will reach 327 680 if the drive frequency is fixed at 16 GHz. The implementation of such a large scale integration requires a large chip area (>10 cm^2), and the required yield is a significant challenge for chip fabrication. One way to integrate a large number of junctions on a limited area is to stack junctions vertically. With this idea, we attempted to fabricate double-barrier junctions [10].

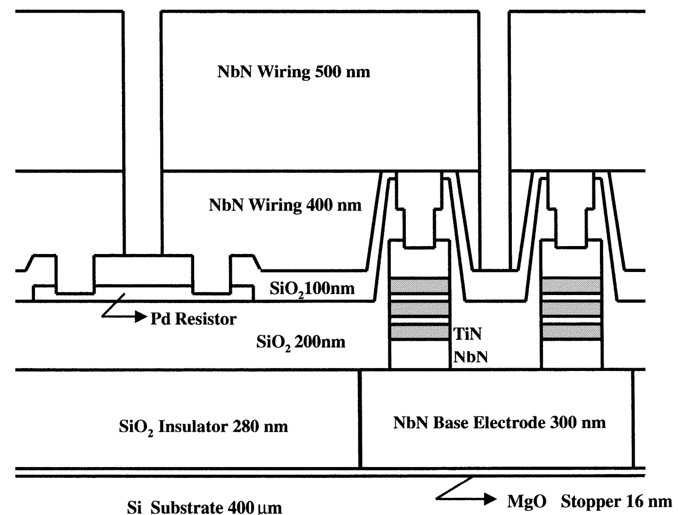

Fig. 1. A cross-sectional diagram showing the fabrication process of vertically stacked triple $(NbN/TiN_x)_3/NbN$ Josephson junctions.

In this paper we report the fabrication of stacked junctions with double and triple barriers. We present the current-voltage characteristics with and without microwave power. We describe the fabrication technique to obtain uniform critical currents with vertically stacked junctions.

II. Fabrication

Fig. 1 illustrates the cross-sectional schematic diagram of vertically stacked triple junctions. First, a MgO film of 16 nm was deposited on a 3-inch Si wafer as an etch stop, then a NbN film 320 nm thick was deposited by reactive rf sputtering. The NbN film was patterned by reactive ion etching. A SiO_2 film of 400 nm thickness was deposited by rf sputtering, and this layer was planarized by chemical mechanical polishing. Multilayers of $(NbN/TiN_x)_n/NbN$ were deposisted by reactive rf sputtering, with the thickness of the bottom and top NbN electrodes being 100 nm, the intermediate NbN electrode 10 or 20 nm, and the TiN barriers varied from 35 to 50 nm. The junction areas were defined by reactive-ion etching. An isulating layer of SiO_2 200

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M. Ishizaki, H. Yamamori, and A. Shoji are with the National Institute of Advanced Industrial Science and Technology, Umezono, Tsukuba 305-8568, Japan (e-mail: may.ishizaki@aist.go.jp).
S. P. Benz and P. D. Dresselhaus are with the National Institute of Standards and Technology, Boulder, CO 80305 USA.
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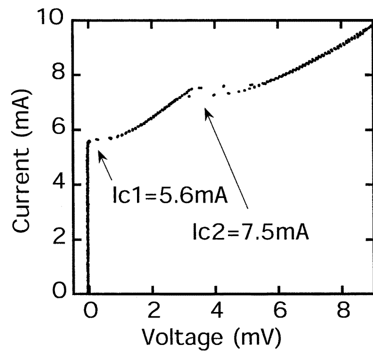

Fig. 2. Two distinct critical currents for the stacked-double-junctions that had the same barrier thickness. The thicknesses of the layers were 35 nm for the lower barrier, 10 nm for the intermediate electrode, and 35 nm for the upper barrier.

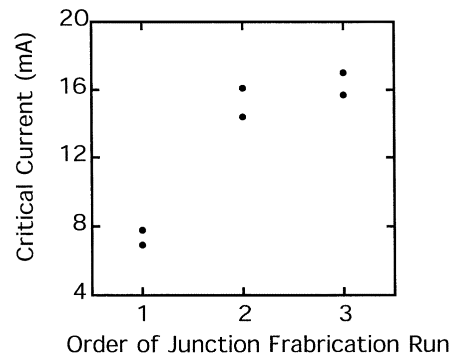

Fig. 3. Dependence of the critical current on the order of junction fabrication run in a sequence. The critical currents for both barriers in the stacked-double-junction arrays are plotted. Each wafer had the same combination of lower and upper barrier thicknesses of 35 nm and 38 nm.

nm thick was rf sputtered. Then a Pd film 50 nm thick was deposited. The Pd film was patterned by use of lift-off to define the termination resistors of the coplanar waveguide transmission lines. Again an insulating layer of SiO_2 100 nm thick was deposited by rf sputtering, and via holes to the junctions and to the resistors were made by reactive ion etching. Finally a NbN wiring film 400 nm thick was deposited by reactive rf sputtering, and planarized by chemical mechanical polishing. Then another NbN film 500 nm thick was deposited and patterned by reactive-ion etching to define the wiring layer.

III. Experiments and Discussion

In order to obtain large and clear constant-voltage steps, the normal-state resistance $R_{\rm n}$ in the stacked junctions should be uniform. As the $R_{\rm n}$ of each junction in the stack could not be detected separately, $R_{\rm n}$ was inferred from the measured critical current $I_{\rm c}$ by assuming a fixed $I_{\rm c}R_{\rm n}$ product for each barrier. This is reasonable because $R_{\rm n}$ depends linearly on the thickness of the barrier, whereas $I_{\rm c}$ depends inverse exponentially on thickness. The $I_{\rm c}R_{\rm n}$ product varies with the thickness of the barrier, but it could be assumed to be constant within the range of about 10% deviance in this report.

Fig. 2 shows two discrete critical currents in a stacked-double-junction array in which the deposition time for both the upper and lower barriers was the same. The deposition time for these TiN_x barriers corresponded to a thickness of 35 nm. This array had a critical current deviation δ of 29%, where δ for the multiple barrier stacked junctions is defined as the ratio of the largest difference between each $I_{\rm c}$ (maximum $I_{\rm c}$ minus minimum $I_{\rm c}$) divided by the average value of all $I_{\rm c}$s.

There are a number of possible causes to explain the different critical currents: 1) the surface condition of the NbN layer could have changed between the lower and upper barrier depositions, 2) the deposition rate could have changed, leading to different barrier thicknesses, or 3) the structure or composition of the TiN_x could be different for the upper and lower barriers. The third possible cause is most likely because, as we show below, the critical current of each barrier depends systematically on the order of its deposition. The deposition of junctions was carried out in such a way that a series of wafers was consecutively placed in a vacuum sputtering chamber in which

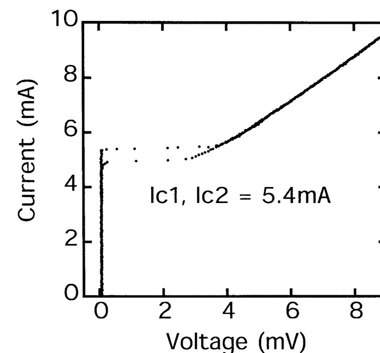

Fig. 4. Identical critical currents for the $I_{\rm c}$-controlled stacked-double-junctions. The thickness of the layers were 42 nm for the lower barrier, 20 nm for the intermediate electrode, and 45 nm for the upper barrier.

NbN electrodes and TiN_x barriers were successively deposited on each wafer. Then the wafer was taken out of the chamber and the next wafer was inserted, continuing the deposition sequence. When the first wafer was placed in the vacuum chamber, its temperature was at an ambient 15 to 25 °C. As the deposition progressed the temperature of the wafer and the substrate holder monotonically increased to a couple of hundred degrees centigrade. The substrate holder in the vacuum chamber has a large thermal capacity, so that when consecutive wafers were inserted they immediately equilibrated to the higher chamber temperature. The higher-temperature deposition may yield higher critical currents, although the mechanism is not yet clear. Nevertheless, as shown in Fig. 3, the critical current of consecutive barriers changes systematically with the order of deposition.

Fig. 3 shows the critical currents for the lower and upper junctions of three wafers in successive junction fabrication runs. The first wafer resulted in the lowest critical currents compared to the second and third wafers. Taking into consideration the systematic variation in critical current, the deposition time for the barriers was altered according to the deposition order.

Fig. 4 shows the current-voltage characteristic of a stacked-double-junction array with the barrier thicknesses tuned to match the critical currents. In this case the two critical currents coincided well with each other. Fig. 5 shows the current-voltage characteristic of a stacked triple 128 × 3-junction array also with the barrier thicknesses tuned to try to match the critical currents. This array had a critical-current deviation δ of

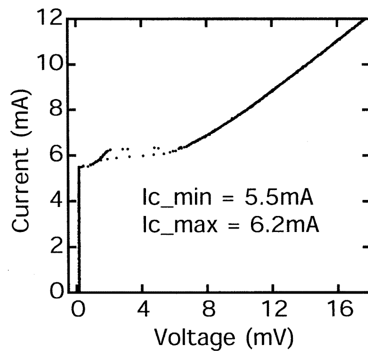

Fig. 5. Current-voltage characteristic of a stacked-triple-junction array.

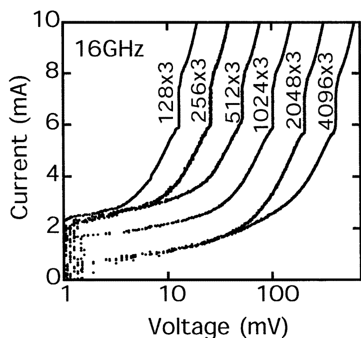

Fig. 6. Current-voltage characteristics of stacked-triple-junction arrays with 16 GHz microwave bias at 4.2 K. Numbers indicate the number of junctions in the array.

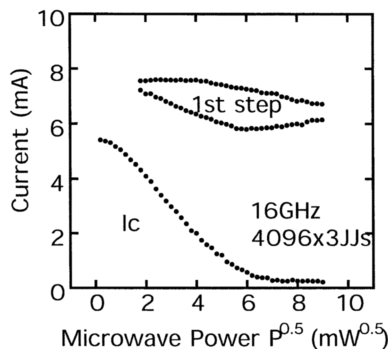

Fig. 7. Dependence of constant-voltage step heights on the microwave power for a 4096 × 3 stacked-triple-junction array at 4.2 K. The frequency of the applied microwave drive was 16 GHz and the power was measured at the generator output.

12%. The current-voltage characteristics of stacked-triple-junction arrays with 16 GHz applied microwave drive at 4.2 K are shown in Fig. 6. The junction arrays exhibited constant-voltage steps consistent with the total number of junctions in the array, including the multiple junctions in the stacks. Fig. 7 shows the constant-voltage step height dependency on the microwave power for the 4096 × 3 stacked triple-junction array from the same chip as in Fig. 6. The microwave power was measured at the output terminal of the microwave source. The maximum height of the first step was larger than 1 mA, which is sufficient for the programmable voltage standard application.

IV. Summary

Stacked double and triple NbN-electrode and TiN_x-barrier junction arrays were fabricated and their current-voltage characteristics were measured with and without microwave power. The critical current for different barriers varied depending on the position within the stack and the order during multi-wafer deposition. The critical currents in the barriers could be matched by adjusting the deposition time (thus the thickness) of the barriers in accordance with the measured systematic variation. Stacked-triple-junction arrays as large as 12 288 (4096 × 3) junctions displayed constant-voltage step heights larger than 1 mA at 4.2 K when biased with the 16 GHz microwave power. These results indicate that the SNS stacked-junction arrays can be used for the programmable voltage standard application.

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