Stacked SNS Josephson Junction Arrays for Quantum Voltage Standards

Paul D. Dresselhaus, Yonuk Chong, Jelle H. Plantenberg, and Samuel P. Benz

***Abstract*—NIST is using and developing superconductor-normal metal-superconductor (SNS) Josephson arrays for both programmable DC and AC voltage standards. Increasing the output voltage is difficult because the output voltage per junction is small; hence series arrays with large numbers of junctions are needed. The best way to generate higher voltages and achieve the best operating margins for the broadband drive signals is by densely packing the junctions into shorter arrays. NIST has been working on stacked SNS junctions to achieve this goal. By stacking junctions in the array, more junctions may be placed per length, while preserving a lumped microwave element. In this paper we introduce our results on stacked SNS junctions using $MoSi_2$ and Ti as barrier materials. These barriers were chosen because they can be reactive-ion etched (RIE) in contrast to our standard PdAu barriers, which must be wet etched. Using RIE, alternating layers of barrier material and Nb may be etched in a single step. We indirectly quantify the junction uniformity in the arrays by measuring the current range of the constant-voltage steps when the arrays are biased with a microwave drive.**

***Index Terms*—Digital-analog conversion, superconducting devices, superconducting films, thin film devices.**

I. Introduction

SUPERCONDUCTOR-normal-metal-superconductor (SNS) Josephson junctions have been used by NIST for programmable voltage standards because of their reproducibility, stable voltage steps, and noise immunity [1]. In addition, SNS junctions have enabled the development of an ac voltage standard system [2]. In order to increase the voltage and input drive bandwidth of these systems, it is desirable to pack junctions in series arrays as densely as possible. For programmable applications, increasing junction density offers higher voltage for a given microwave signal and chip size [3]. For ac waveform generation, the wavelength of the highest drive frequency influences the operating margins of the Josephson arrays, so that higher junction density leads to higher voltage for a given input drive bandwidth, or a larger operating bandwidth for the same voltage [4]. If the junction density is sufficiently high, lumped elements may be fabricated, easing the design of ac and dc voltage standard circuits. Higher junction packing density leads to higher voltage from a given series array, higher input bandwidth and operating margins (from increased standing wave frequency for a given number of junctions), and higher output bandwidth from reduced parasitic inductance per junction.

In order to increase the junction density, one may either pack junctions in-plane, or stack junctions perpendicular to the substrate. Uniformity is critical for voltage standard applications, and the uniformity of in-plane junctions is limited by the difficulty of controlling the barrier thickness in the in-plane directions. Such in-plane or in-line junctions are defined usually by removing materials in a bi-layer structure [5] or by modifying a thin superconducting film with ion implantation or damage [6]. Furthermore, because this approach is limited typically to thin films the junctions are usually one-dimensional, limiting the critical current and resistance values that can be simultaneously achieved. Ramp-type SNS junctions have been investigated, but their uniformity is limited because the barriers are not made in-situ with the Nb electrode [7].

The demonstrated uniformity of planar junctions has been excellent [8], [9], suggesting that stacked planar junctions would likely have better uniformity as well. Uniformity of planar and stacked junctions is determined primarily by barrier thickness, followed by the in-plane dimensions defined by lithography and etching. Uniform planar SNS junctions have been successful because the current density depends exponentially on the barrier thickness, which is well controlled and reproducible. The barrier thickness of the normal metal is defined typically by sputter deposition, which can easily be controlled to less than 1 nm. The first useful stacked SNS junctions were demonstrated with TiN_x barriers with NbN superconductors [3].

Stacked junctions have also been fabricated using superconductor-insulator-superconductor junctions [10], but because these junctions are hysteretic, they are not useful for ac voltage-standard applications. Superconductor-insulator-normal-metal-insulator-superconductor (SINIS) junctions have been successfully demonstrated for Josephson junction arrays for voltage-standard applications [11]. Their advantages include high $I_c R_N$ products and independently controlled critical current and resistance. However, this technique is not conducive to making stacked arrays because each barrier requires two separate time-consuming oxidation steps. High temperature superconductors have also been used to fabricate double-junction single-stacks using layer-by-layer growth, but no arrays were made [12]. This paper presents our best results to date at NIST on the development of stacked SNS junctions.

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Our standard process for SNS junctions uses a PdAu alloy barrier. The advantages of PdAu are the long-term electrical stability, moderate resistivity, and ease of deposition. The PdAu barrier is patterned with a wet acid etch because it does not etch in a fluorine plasma. This material and process are not suited for multiple barriers in a stacked configuration where junction uniformity is critical. Therefore, we have pursued other normal-metal materials. The choice of a normal-metal barrier was driven by the following considerations: the barrier material should be sputtered in-situ with the Nb films; the barrier must remain a normal metal well below the temperature of operation; the barrier must etch in a reactive-ion etcher (RIE) with a rate similar to that of niobium. Measurement and application considerations also dictate that the resistivity of the barrier be similar to or larger than that of PdAu (35 to 40 $\mu\Omega$-cm). Other researchers have explored TiN_x for SNS barriers [3]. In our research we have investigated normal metal barriers of TiN_x, Ti, and $MoSi_2$.

II. Fabrication

Devices were fabricated in a manner similar to our standard SNS process using PdAu junctions, except for the barrier deposition and patterning. First, a multilayer is grown by DC sputtering a 260 nm Nb base electrode, followed by an alternating series of barriers and inner Nb electrodes, ending with a final 160 nm Nb electrode on top. Details of the normal-metal barriers will be discussed later. The junctions are then etched in a single step, stopping at the top of the base electrode. RIE is used for the junction etch using a mixture of SF_6 and O_2, the exact mixture depending on the barrier material, but is gauged such that the barrier etch rate is approximately equal to the Nb etch rate. A dry etch was found to be the best way to fabricate the vertical side-walls needed to yield a uniform stack of junctions [13].

After the junctions are etched, the base electrode is patterned and etched using RIE in an SF_6 plasma without O_2. A 350 nm film of SiO_2 is then deposited on the wafer by plasma-enhanced chemical vapor deposition. During the oxide deposition, the wafer is rf-biased to ensure a smooth film, while the wafer temperature is maintained below 100°C by use of a back-side He-gas-cooled electrostatic chuck. Vias are made through the oxide to the top Nb layer of the stack. The stacks are interconnected with a reactive-ion-etched 600 nm wiring layer of Nb. Finally, a 160 nm layer of PdAu is lifted off to define the on-chip resistors and contact pads.

The critical issue for the fabrication of uniform arrays of stacked junctions is the vertical profile of the junction stack. Fig. 1 shows different profiles for two multi-layers containing two stacked Ti barriers that were etched with different plasma chemistries. Clearly, the stacked barriers in Fig. 1(b) have more nearly equal areas and their corresponding junctions will have more uniform electrical characteristics than the stack in Fig. 1(a). Both the partial flow of O_2 and the power were critical parameters used to optimize the profile. A minimum pressure of 2.7 Pa was always used to optimize the etch anisotropy. We found that optimizing the vertical profile of a test stack (Fig. 1) is adequate for optimizing the uniformity of an array of stacks.

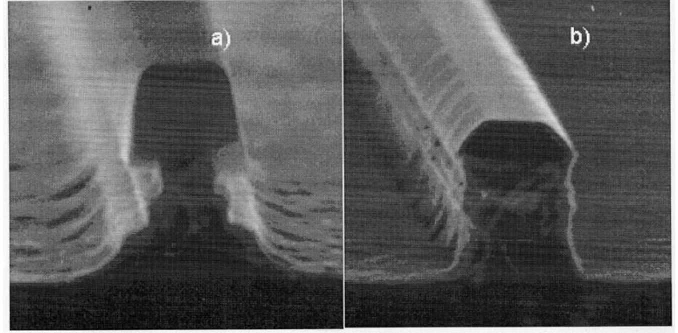

Fig. 1. Etch profiles of Ti barrier double stack. Stack (a) is etched with 50 sccm of SF_6, 13 sccm O_2, at 2.7 Pa, and 50 W of rf power. Stack (b) is etched with 50 sccm of SF_6, 15 sccm O_2, at 2.7 Pa, and 100 W of rf power. Etch conditions must be well characterized before vertical etches can be performed.

We investigated TiN_x barriers because the etch rate is very similar to that of Nb. Junctions with TiN_x barriers were fabricated using dc reactive sputtering, and varying the Ar and N partial pressures was used to change the nitrogen content in the film. Furthermore, vertical profiles were easily fabricated using pure SF_6 etches. However, measured uniformities were poor, and critical currents were often very large. Further studies found that the TiN_x barriers had rather high superconducting transition temperatures. Depending on the stoichiometry, the superconducting transition temperature could be varied between 2.4 K and 5.5 K [14]. For these transition temperatures, which are extremely close to the 4 K operating temperature, the coherence length is very long. In order to achieve reasonable uniformity of the electrical characteristics with TiN_x, either the barrier must be thick relative to these coherence lengths or the superconductivity must be suppressed with impurities. For these reasons, we have not continued investigation of the TiN_x barrier system.

We also investigated titanium barriers using dc sputtering. Titanium has the advantages that it has a low superconducting transition temperature and a moderate resistivity ($\sim$100 $\mu\Omega$-cm). However, its etch rate is slower than that of Nb in pure SF_6. By varying the etch conditions, vertical profiles were achieved using an SF_6:O_2 mixture at 50:15 sccm flow, a pressure of 2.7 Pa and 100 W rf power [13]. By means of this recipe, double-junction stacks were fabricated with sufficient uniformity to observe flat Shapiro steps over more than 1 mA current range with a 16 GHz microwave signal (see Fig. 2). Although we successfully fabricated multiple wafers of uniform Ti-barrier stacked arrays, we found that the run-to-run reproducibility was poor. Because Ti actively getters oxygen, the low temperature electrical properties depend strongly on the presence of residual gases in the chamber of our sputtering system.

Because of the poor reproducibility of Ti barrier junctions, alternative normal-metal barriers were investigated. The most promising multi-junction stacks were fabricated with molybdenum disilicide ($MoSi_2$) barriers by dc sputtering from a solid source target. Electrically, $MoSi_2$ is a normal metal with a resistivity about 10 times higher than that of PdAu ($\sim$500 $\mu\Omega$-cm at 4 K). The higher resistivity allows thinner barrier junctions of larger area for the same critical current (I_c) and normal-state resistance (R_N). As long as the film is passivated, $MoSi_2$ was found to have good long-term electrical stability. Similar to Ti, the etch rate in pure SF_6 is slower than that for Nb, but, vertical

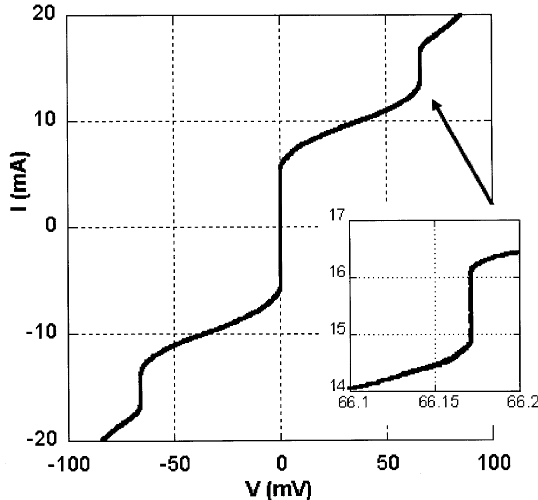

Fig. 2. Current–voltage plot of an array of 1000 double-junction stacks with 40 nm thick Ti barriers and an applied 16 GHz microwave signal. The inset shows that the constant-voltage step is flat over more than 1 mA and is at the proper voltage.

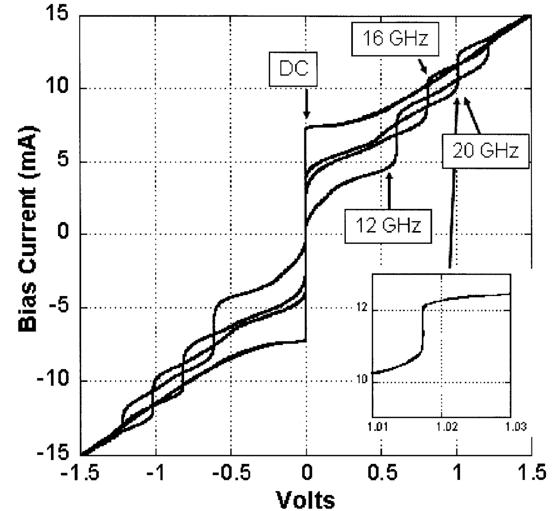

Fig. 3. Current–voltage characteristics of $MoSi_2$ triple-junction stacks in 2 series-connected arrays each having 4100 stacks. The stack thicknesses (from counter-electrode to base-electrode) are 180 nm, 24 nm, 50 nm, 24 nm, 50 nm, 24 nm, and 330 nm. The inset shows that the constant-voltage step above 1 V is flat over more than 1 mA for the 24 600 junction array.

profiles were achieved by adding O_2. In addition, no superconducting transition was found upon cooling the $MoSi_2$ films to 50 mK.

The current–voltage characteristics of two series-connected arrays of 4100 3-junction stacks (for a total of 24 600 series junctions) are shown in Fig. 3. In order to properly bias the arrays, the microwave drive is applied in parallel to the two arrays, but the dc current is applied in series. Different drive frequencies were used to produce constant-voltage steps at different voltages. The Shapiro steps are flat for a range of at least 1 mA of bias current over the measured frequency range from 12 GHz to 20 GHz.

In addition to good uniformity, as demonstrated by the constant-voltage steps, $MoSi_2$ barriers also displayed excellent run-to-run reproducibility. Fig. 4 shows a plot of the characteristic voltage (I_cR_N) for all the fabrication runs with $MoSi_2$ barriers. This type of barrier control is critically important for the fabrication of stacks, and is similar to the run-to-run reproducibility of PdAu barriers.

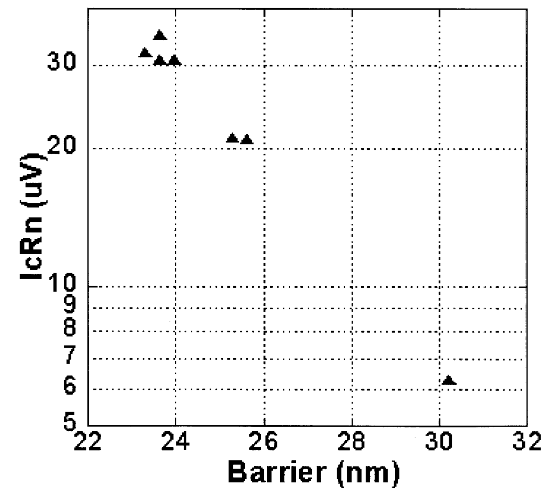

Fig. 4. Critical voltage (I_cR_N) of all wafers fabricated using $MoSi_2$ barriers. The barrier thickness is inferred from the deposition time and assumes a deposition rate of 19.7 nm/minute.

III. Measurements and Discussion

Barrier uniformity is the key to getting flat constant-voltage steps in an array of Josephson junctions. A single junction with a deviant critical current or resistance will produce a sloped voltage step when measured across the array. The use of in-line junctions for voltage standard applications generally suffers from nonuniform electrical characteristics because variations in the barrier length produce nonconstant voltage steps. Vertically stacked junctions have much higher barrier uniformity because thin films are routinely grown with thickness variations <1 nm. The challenge with vertical stacks then is to make every junction in the stack have the same area.

In order to measure the uniformity of a junction stack, the first step is to measure the vertical profile (e.g., Fig. 1) with a scanning electron microscope or some other high-resolution imaging tool. For this measurement, an elongated test structure is cleaved, and then the edge profile is imaged. The next step is to embed an array of stacked junctions in a coplanar transmission line and measure the current–voltage characteristics with and without microwaves. All of these electrical measurements were done at 4 K in a liquid-helium bath using a dip probe with a μ-metal can surrounding the chip.

Typical junctions have an I_cR_N product of $\sim$23 μV to operate between frequencies of 4 GHz to 20 GHz. Fig. 5 shows the microwave response of a double-junction array of 1000 elements over this frequency range. The broadband filters for this circuit are described in [2]. The range of frequency over which a flat step with large current margins may be achieved is important for applications to ac waveform generators [2], [8]. By making the physical length of the array short, resonances (corresponding to standing waves in the structure) are pushed out of band-the features observed around 9 and 11 GHz in Fig. 5 are most likely due to such a resonance. The decrease in bias range

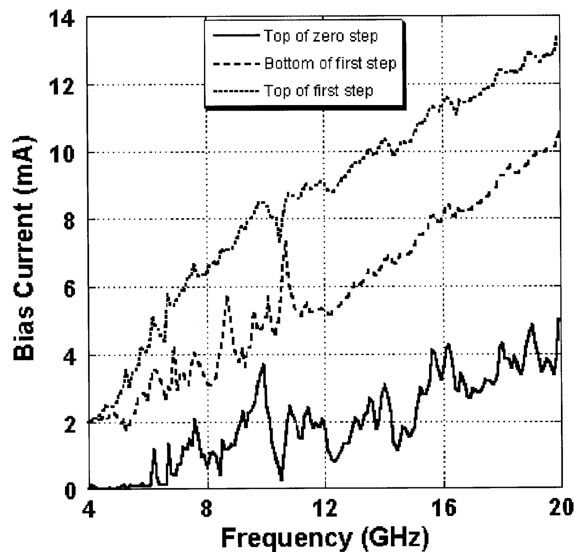

Fig. 5. Microwave response of a 1000-stack array of double junction stacks with $MoSi_2$ barriers. The lower trace corresponds to the top of the constant-voltage step at zero voltage, the middle trace corresponds to the lowest current value of the first step, and the top trace corresponds to the maximum current of the first constant-voltage step.

at low frequency is caused by the combined effects of nonuniformity and the dynamic response of the junctions when biased at frequencies far below the junction characteristic frequency. The use of such arrays in our ac voltage-standard system will allow higher-voltage operation without limitations due to resonances.

Our ultimate goal is to produce a 50 Ω lumped array with 10 mA critical current junctions and I_cR_N products between 20 and 40 μV. This will enable 0.5 to 1 V operating voltages for each array [4]. This is important for higher-voltage ac waveforms from the Josephson arbitrary waveform synthesizer as well as for higher-voltage (2 V to 10 V) programmable dc voltage standards with fewer arrays in parallel.

IV. Conclusion

A reliable method of fabricating uniform arrays of stacked Josephson junctions is presented. Using $MoSi_2$ as a barrier material, double and triple junction stacks were fabricated and measured. The microwave response shows that the junction stacks have excellent uniformity. The maximum number of barriers in a junction stack will be limited by vertical etching uniformity and heat dissipation. We are continuing our research to improve the vertical etch process and to increase the number of junctions in each stack. The results are promising for the implementation of junction stacks into ac and programmable dc voltage-standard circuits. Further work will attempt to implement stacked junctions in these circuits. We will also pursue other barrier materials that may have advantages over $MoSi_2$. For example, a material with an etch rate that matches that of Nb in a pure SF_6 etch would be advantageous.

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