Characteristics and Utilization of a New Class of Low On-Resistance MOS-Gated Power Device

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Abstract - A new class of MOS-gated power semiconductor devices Cool MOS™† has recently been introduced with a supreme conducting characteristic that overcomes the high on-state resistance limitations of high voltage power MOSFETs. From the application point of view, an immediate and very frequently asked question arises: this device behaves like a MOSFET or an insulated gate bipolar transistor (IGBT)? The goal of this paper is to compare and contrast the major similarities and differences between this device and the traditional MOSFET and IGBT. In this study, the new device is fully characterized for its (1) conduction characteristics, (2) switching voltage, current, and energy characteristics, (3) gate drive resistance effects, (4) output capacitance, and (5) reverse bias safe operating areas. Experimental results indicate that the conduction characteristics of the new device are similar to the MOSFET but with much smaller on-resistance for the same chip and package size. The switching characteristics of the Cool MOS are also similar to the MOSFET in that they have fast switching speeds and do not have a current tail at turn-off. However, the effect of the gate drive resistance on the turn-off voltage rate-of-rise (dv/dt) is more like an IGBT. In other words, a very large gate drive resistance is required to have a significant change on dv/dt, resulting in a large turn-off delay. Overall, the device was found to behave more like a power MOSFET than like an IGBT.

I. INTRODUCTION

In high frequency power conversions, the switching loss can be reduced or eliminated through soft-switching techniques [1], but the device voltage drop imposes an inherent loss that is not reducible through circuit design. The Cool MOS [2] – [4], being considered as a breakthrough device, was mainly developed to reduce the turn-on voltage drop or the on-resistance for high voltage applications. The basic principle applied to achieve the breakdown voltage is not through low doping concentration and thick epitaxial layer as it is for the power MOSFET, but through the insertion of vertical "p-strips" in the drift zone. The voltage blocking capability is thus established in both vertical and horizontal directions with a three-dimensional (3-D) structure [2]. This technique allows for a reduction in layer thickness while maintaining voltage blocking and an increase in doping concentration to reduce the on-resistance.

Although this new 3-D MOSFET device maintains high blocking voltage with low on-resistance, the question arises as to whether the added p-strip would alter the original characteristics of the traditional MOSFET. A series of tests are thus conducted to verify some important features:

(1) Conduction characteristic: With the added p-strip, the main question is whether a junction voltage drop is created at zero current or not. Other concerns exist regarding the on-resistance versus gate voltages and temperature. A positive temperature coefficient is desirable if parallel operation is needed.

(2) Switching voltage, current, and energy waveforms: The expectation for a MOS-gated device is that it should have a fast switching speed without a current tail, so that it can replace the insulated gate bipolar transistors (IGBTs) for high voltage applications. The main concern is whether the special structure in this new device affects the switching behavior and whether any differences from the characteristics of traditional MOSFETs and IGBTs affect circuit utilization.

(3) Gate drive resistance effects: Gate drive resistance effects are related to the gate capacitance characteristics. Traditional MOSFET and IGBT devices exhibit different characteristics in turn-off voltage rate-of-rise modulation by the gate drive resistance, or "active snubbing" [5]. Because the p-strip cell apparently redefines the gate input characteristics of this new device, the active snubbing possibility is questionable.

(4) Output capacitance: The output capacitance of a MOS device is typically a function of the output voltage. It was found that the variation of the output capacitance vs. voltage is very large and is nonlinear in a Cool MOS. For the sample 600 V device, the output capacitance decreases by two orders of magnitude when the drain-source voltage increases from 0 to 300 V. This wide range of capacitance variation can have significant impact on switching loss at light-load or no-load condition.

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(5) Reverse biased safe operating areas (RBSOA): The RBSOA test is to investigate high-voltage avalanche breakdown which is expected to be improved in the Cool MOS because it incorporates the "spacer" techniques used in the SIPMOS [2]. This feature is verified with the unique non-destructive unclamped RBSOA test system [6].

II. Structure of MOS-Gated Devices

To understand how the Cool MOS emerges as a new class of power devices, it is essential to differentiate its internal structure from other MOS devices. Fig. 1 illustrates how the Cool MOS is evolved from a conventional diffused MOSFET (D-MOS). In a conventional D-MOS, shown in Fig. 1(a), the breakdown voltage is obtained by reducing doping concentration and increasing thickness of the n^- epitaxial layer. This approach drastically increases the on-resistance for high voltage blocking requirements.

Fig. 1(b) shows the structure of an IGBT which deviates from D-MOS by replacing the n^+ substrate with a p^+ substrate to obtain high-voltage blocking capability while maintaining low on-resistance. This approach, however, introduces an inherent junction voltage drop during conduction.

The structure formed in Cool MOS can be considered as an extension of the p^+ body in a D-MOS to a vertical p-strip in the epitaxial layer, shown in Fig 1(c). With this p-strip, the high voltage blocking capability can be obtained in both vertical and horizontal directions while the junction voltage-drop can be avoided. Unlike the IGBT that has a PNP transistor dominating the device characteristic, the Cool MOS preserves much of original features of a conventional MOSFET.

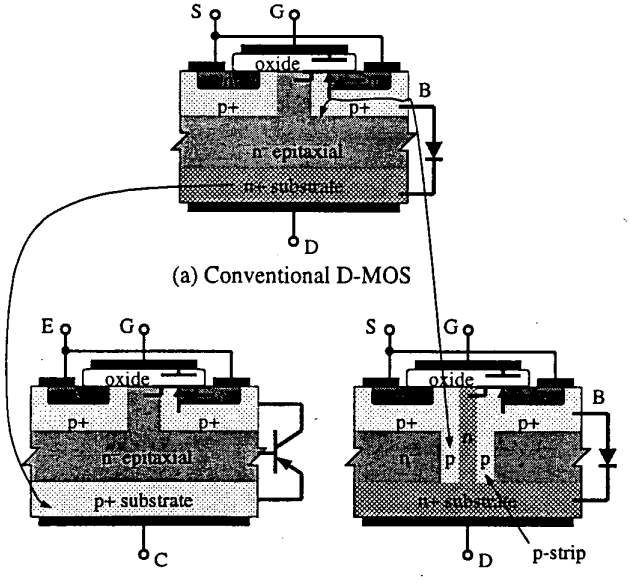


Fig. 1. Evolution of IGBT and Cool MOS from D-MOS.

III. Conduction Characteristics

The conduction characteristics were scanned at different gate voltages and different device temperatures using a Curve Tracer. As expected, the on-resistance of the Cool MOS is significantly lower than that of the same chip-size traditional MOSFET. Unlike the IGBT, this high voltage device does not have a junction voltage drop near the zero current condition.

Fig. 2 shows the measured conduction characteristics with different gate-source voltages, V_{GS}, at 25 °C. The horizontal axis variable, V_{DS}, represents the voltage across the drain and source, and the vertical axis variable, I_D, represents the drain current. The applied V_{GS} starts from 8 V with a 2-V increment. There is a clear transition between operating regions for V_{GS} between 8 V and 10 V. When V_{GS} exceeds 10 V, the device basically exhibits a linear resistive behavior within the 20 A device current range. For the current beyond 20 A range under non-continuously conducting condition, the voltage-current characteristics will be discussed in Section VII.

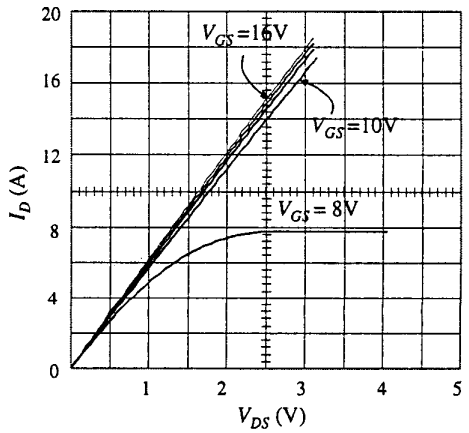


Fig. 2. Conduction characteristics at different gate drive voltages.

Using the slope of the conduction characteristics, the on-resistance is found to be 172 mΩ at V_{GS} = 15 V. The temperature effect on the on-resistance was measured with more frequent pulses to increase the case temperature. The measured resistance was about 258 mΩ at 75 °C case temperature. This positive temperature coefficient would allow paralleling of devices in steady state.

IV. Switching Characteristics

The turn-on and turn-off are the major concerns of a switching device. In high power inverter applications, however, the body-diode can hinder the use of MOSFETs because of its slow recovery characteristic. Thus, the switching characteristic evaluation includes three tests: (1) diode reverse recovery, (2) turn-on, and (3) turn-off. Fig. 3 shows the test setup for these three tests.

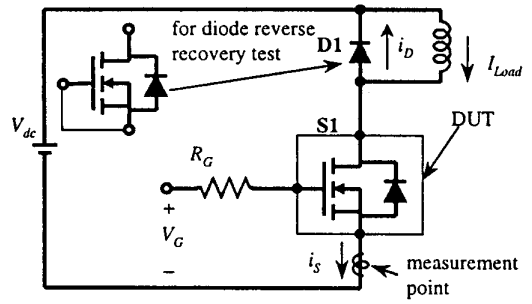


Fig. 3. Test setup for switching characteristics.

A. Reverse Recovery Characteristic of Body Diode

In Fig. 3, S1 is the device under test (DUT), and D1 is an ultra fast recovery diode for free wheeling. When testing the reverse recovery characteristic of the body diode, D1 is replaced with a Cool MOS with gate-source shorted and becomes the DUT. Fig. 4 shows the measured body diode current i_D and the voltage across drain and source V_{DS}. The reverse recovery characteristic is somewhat affected by the switching speed of the lower device S1. With R_G = 100 Ω for S1, the reverse recovery time t_{rr} is 410 ns, the reverse recovery energy E_{rr} is 520 μJ, and the peak reverse recovery current $I_{D\text{-}rr}$ is 2.15 times the load current I_{Load}. For lower R_G values, t_{rr} and E_{rr} are reduced, but the $-I_{D\text{-}rr}/I_{Load}$ ratio is increased. The body diode exhibits "abrupt" recovery characteristic because the high impedance period, t_b, is found to be 85 ns and is much smaller than t_{rr}.

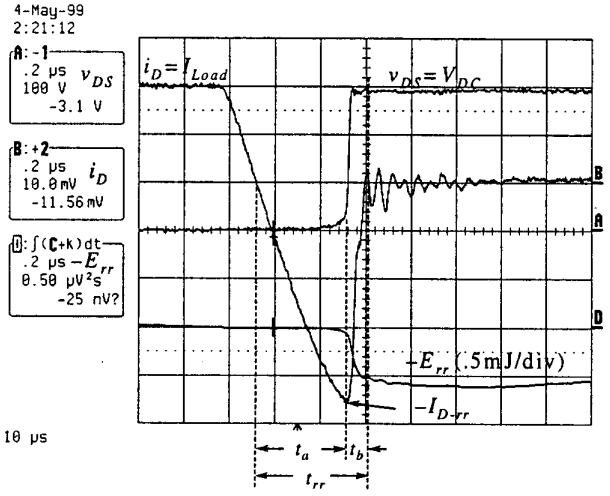


Fig. 4. Voltage and current waveforms of the device in the free-wheeling path.

Under the same load condition and test setup, the measurement was conducted for two other similar current-rated but lower voltage-rated conventional MOSFETs, IRFP360 and IRFP460. Table 1 compares the measurement results of the reverse recovery characteristic. Cool MOS shows slightly longer t_{rr}, same $I_{D\text{-}rr}$, but much less E_{rr}, as compared to those of conventional MOSFETs.

TABLE I
COMPARISON OF BODY DIODE CHARACTERISTICS

Device	R_G (Ω)	t_{rr} (ns)	$-I_{D\text{-}rr}/I_{Load}$ (pu)	E_{rr} (μJ)
CoolMOS	47	500	2.6	310
	100	600	2.15	520
IRFP360	47	320	2.7	500
	100	400	2.1	1000
IRFP460	47	400	2.7	500
	100	450	2.15	980

B. Turn-on Characteristic

The diode peak reverse current can be considered as the peak turn-on current of the low-side device, S1. Using an external ultra-fast recovery diode as the free-wheeling diode, the peak turn-on current of S1 is much reduced. Fig. 5 shows the measured turn-on voltage and current at a 300 V, 20 A condition. Similar to a conventional MOS turn-on device, the Cool MOS turn-on process can be explained as follows:

- t_0: Gate drive input logic signal sends turn-on command. The gate drive output voltage starts charging the gate-source capacitance.
- t_1: Gate-source voltage exceeds the threshold voltage, current i_S starts rising, and i_D starts reducing
- t_2: Current i_S exceeds the load current, i_D = 0. Circuit enters into diode reverse recovering period, and the gate drive voltage starts charging the Miller capacitance, i. e., the capacitance between gate and drain, C_{gd}.
- t_3: Diode is reverse blocking, current i_S reaches the peak because it is the sum of I_{Load} and $I_{D\text{-}rr}$.
- t_4: Current equals the load current, voltage drops to zero.

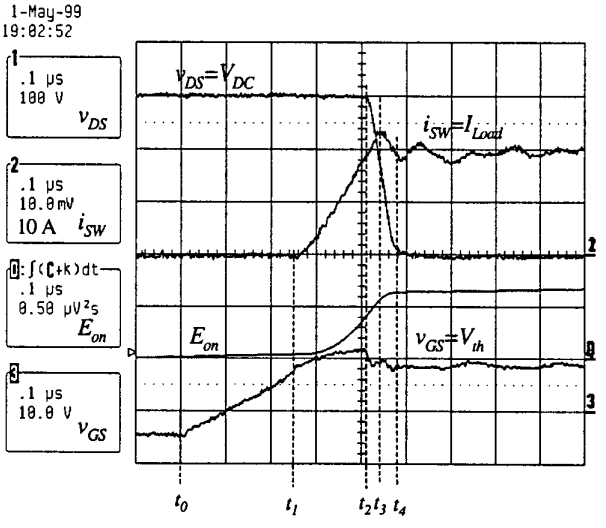


Fig. 5. Turn-on characteristic at 300V, 20A.

From the R_G = 100 Ω measurement results shown in Fig. 5, several key turn-on parameters can be obtained. These parameters include:

(1) the turn-on delay time $t_{d\text{-}on}$, measured from t_0 to t_1, is about 0.23 μs;
(2) the turn-on rise time t_r, measured from t_1 to t_2, is about 0.2 μs;
(3) the reverse recovery time t_{rr}, measured from t_2 to t_4, is about 80 ns;
(4) the turn-on energy E_{on}, obtained using the oscilloscopes integration function, is about 0.5 mJ.

It should be noted that the complete turn-on process actually extends beyond point t_4 to where the gate source capacitance is fully charged to the gate drive supply voltage.

C. Turn-off Characteristic

Fig. 6 shows the turn-off characteristics of the DUT. This figure indicates that this high voltage device does not exhibit a turn-off current tail characteristic of IGBTs. The turn-off process can be explained as follows.

t_5: Gate drive input logic signal sends turn-off command, and the gate drive output voltage decreases. The gate-source capacitance starts discharging.
t_6: Gate voltage drops below the threshold voltage, drain voltage starts rising. Current does not fall until v_{DS} exceeds the dc bus clamp voltage.
t_7: Current starts falling, but the source inductance slows down the drain current rate-of-fall and causes a gate-source voltage ringing.
t_8: Current falls to zero and the gate-source voltage continues discharging.

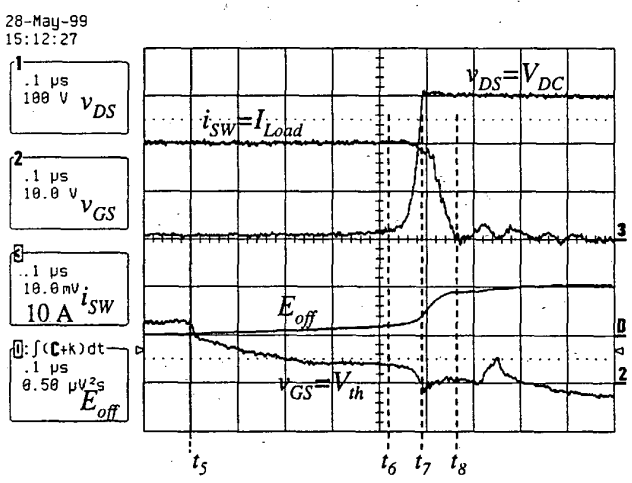


Fig. 6. Experimental Cool MOS turn-off waveforms (voltage, current and switching energies) at 300-V bus.

From the R_G =47 Ω, measurement results shown in Fig. 6, several key turn-off parameters can be obtained. These include:

(1) the turn-off delay time $t_{d\text{-}off}$, measured from t_5 to t_6, is about 0.42 μs;
(2) the turn-off fall time t_f, measured from t_7 to t_8 is about 70 ns,
(3) the turn-off energy E_{off}, obtained using the oscilloscopes integration function, is about 0.5 mJ.

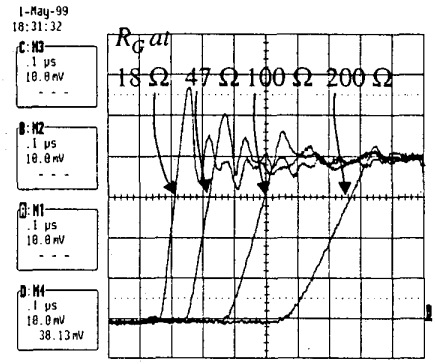
It should be noted that $t_{d\text{-}off}$ is a function of the gate resistance. As R_G becomes larger, $t_{d\text{-}off}$ becomes longer.

V. Gate Drive Resistance Effects

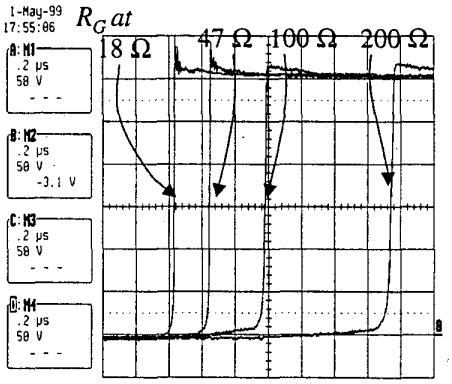
It is well known that for the IGBT and power MOSFET, the gate drive resistance, R_G, affects the turn-on delay and current rise time as well as the turn-off delay and voltage rise time. With the p-strip structure, the major change in the new device is that the gate-drain feedback capacitance is much smaller at high drain voltages than it is for the traditional MOSFET. This occurs because the gate-drain capacitance is determined by the space charge region capacitance at high voltages and the space charge region capacitance is reduced by the p-strips. Because the gate-drain capacitance is the series combination of the gate oxide capacitance and the drain-source space-charge region capacitance [2], the feedback capacitance is even more nonlinear than for the traditional power MOSFET and IGBT devices. This nonlinear feedback capacitance causes a ringing at the gate-source voltage during turn-off as can be seen in Fig. 6 where the gate voltage tends to oscillate from t_7 and up. Even with a tight circuit layout and a high R_G value (47 Ω), the ringing cannot be completely damped.

The nonlinear input characteristics lead to questions regarding the gate drive resistance effect on both turn-on and turn-off, especially the active snubbing for the turn-off dv/dt modulation. Fig. 7(a) shows the turn-on delay and current rise time variations due to the change of R_G, where R_G is varied from 18 Ω to 200 Ω. Similar to the traditional MOSFET and IGBT, the turn-on delay and current rise time are increased with the R_G value. Higher R_G values tend to slow down the turn-on speed and reduce the peak current caused by the diode reverse recovery. However, it also increases the turn-on losses.

Fig. 7(b) shows the turn-off delay and voltage rise time variations due to the change of R_G which is varied from 18 Ω to 200 Ω. It is interesting to see that the turn-off delay is significantly affected by the R_G value, but that the voltage rate-of-rise is not affected unless R_G is very large. Varying R_G at 18 Ω, 47 Ω, 100 Ω, and 200 Ω, the turn-off delay time was found to be 180 Ω, 400 Ω, 720 Ω, and 1450 ns, respectively. However, the turn-off dv/dt remains constant even with this wide variation in turn-off delay time. This characteristic is quite different from traditional MOSFETs but similar to IGBTs. The test results indicate that active snubbing is not possible with limited variation of R_G. It was suggested in [5] that adding a gate-to-drain feedback capacitor with a series feedback resistor would allow dv/dt modulation for IGBTs. For the new Cool MOS device, this active snubbing requirement is similar to that of the IGBT.



(a) Turn-on delay and current rise effects



(b) Turn-off delay and voltage rise effects

Fig. 7. Turn-on and turn-off delay due to gate resistance.

Table 2 compares the measurement results of switching loss and switching energy for Cool MOS, IRFP360, and IRFP460. Overall, the switching losses among these three devices are at a similar level, and are a function of gate resistance. In practical applications, R_G larger than 100 Ω may not be used in high frequency switching. They are tested mainly just to show the effects of R_G variation.

TABLE II
SWITCHING LOSS AND DELAY AS A FUNCTION OF GATE RESISTANCE

Device	R_g (Ω)	E_{on} (mJ)	$T_{d\text{-}on}$ (ns)	E_{off} (mJ)	$T_{d\text{-}off}$ (ns)
Cool MOS 20 A	18	0.375	100	0.48	180
	47	0.5	120	0.5	400
	100	0.65	230	0.6	720
	200	1.2	510	0.7	1,450
IRFP 360P 20A	18	0.4	65	0.4	230
	47	0.56	120	0.7	560
	100	0.85	240	1.45	1,100
	200	1.5	460	2.2	2,200
IRFP 460P 20A	18	0.45	60	0.45	270
	47	0.64	120	0.94	550
	100	1.01	230	1.6	1,200
	200	1.5	400	2.4	2,500

It should be noted that the turn-off energy of Cool MOS only varies slightly with a wide range of gate resistance, while the other two conventional MOSFETs show a significant turn-off energy variation with respect to the gate resistance variation.

VI. OUTPUT CAPACITANCE

In a conventional MOSFET, the output capacitance varies with the drain-source voltage, and the range of variation is approximately one order of magnitude. In a Cool MOS, however, the output capacitance exhibits a wide variation with respect to the drain-source voltage. For the sample 600 V device, the output capacitance decreases from 7000 to 60 pF, two orders of magnitude reduction, when the drain-source voltage increases from 0 to 300 V. This high initial capacitance along with wide range variation can have significant impact on switching loss in different applications.

Consider a half-bridge circuit with an inductive load, L, and a blocking capacitor, C_b, shown in Fig. 8. The devices were mounted on a small heat sink with forced-air cooling. A 250-ns dead time is provided to avoid shoot through. When the upper switch S1 is on, the load current, I_L, increases linearly, but the increasing rate is inverse-proportional to the load inductance, L. When S1 is turned off, its output capacitance C_{o1} needs to be charged to the dc bus voltage, and C_{o2} needs to be discharged from full voltage to zero. The energy that charges C_{o1} and discharges C_{o2} comes from I_L.

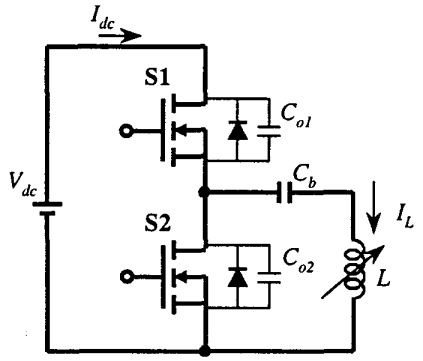


Fig. 8. Test circuit with varying load inductance.

If I_L is zero or very small, then these capacitances will be charged and discharged by turn-on of the opposite switch, rather than by the inductor current. In this case, the switching loss will be high. If I_L is sufficiently high to charge C_{o1} to the dc bus voltage, and to discharge C_{o2} to zero, then the load current will be diverted to the body diode of S2, and S2 can then be turned on at zero voltage, resulting in the minimum switching loss condition.

With a high initial output capacitance, the Cool MOS requires a high current, I_L, to naturally turn off the switch as compared to the conventional MOSFETs. The test condition is to have a fixed dc bus voltage V_{dc} = 300 V, and a switching frequency of 200 kHz. The load inductance values used for

these tests start from open circuit, and then are reduced from 404 μH to 70 μH so that the load current increases from zero to 2.68 A at the lowest inductance. The input dc power was obtained by $P_{dc} = V_{dc} I_{dc}$. This power contains both the device switching loss and resistive losses, i.e., $P_{dc} = P_{sw} + P_L$ where P_{sw} is the switching loss, and P_L includes all resistive losses in the load inductor and switch on-resistance.

Fig. 9 shows the experimental results. When the load circuit is open, $L = \infty$ and $I_L = 0$, the total loss P_{dc}, containing only the switching loss P_{sw}, is measured at 20 W and 5 W, respectively for the sampled Cool MOS (SPP20N60S5) and the conventional MOSFET (IRF840). The IRF840 is compared because it has a similar die size. With Cool MOS, the case temperature increases to 50°C without inductor connected. After the inductor is connected, the load current I_L is established, and the switching loss P_{sw} is reduced. At 1.6 A, P_{sw} drops to a minimum, and the loss contains only P_L. P_{dc} then becomes proportional to I_L^2. It can be seen from Fig. 9 that for the IRF840, I_L at 0.5 A is sufficient to reduce P_{sw} to zero, and for the SPP20N60S5, I_L needs to be increased to 1.6 A to eliminate P_{sw}.

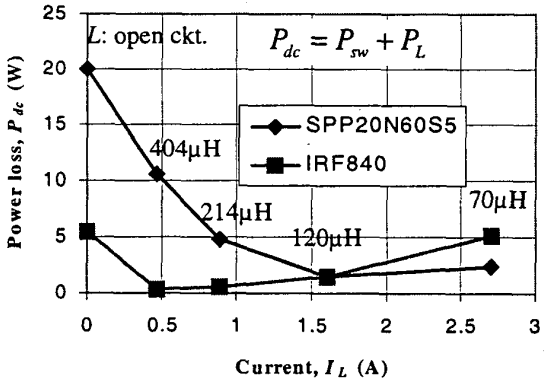


Fig. 9. Switching loss due to the effect of load current and output capacitance.

VII. Safe Operating Areas

In most hard-switching applications, the device needs to turn off high currents under inductive load conditions. If the voltage is clamped, most MOS-gated devices, including the IGBT, can withstand high turn-off currents with clamp voltages near the device rated voltage. However, for the unclamped inductive switching (UIS) condition, the voltage spike can easily cause avalanche failure and differences exist between device types. For example, power MOSFETs can withstand UIS conditions with the only restriction being in the amount of energy and thus avalanche time the device can withstand before failure. Power MOSFETs are typically rated for their UIS Energy capability. However, typical IGBTs do not have UIS Energy capability and fail a short time after the device begins to avalanche.

The question thus arises as to the clamped and unclamped switching failure for the new Cool MOS device type. In this study, the clamped and unclamped inductive switching failure is studied using an automated nondestructive RBSOA tester developed by National Institute of Standards and Technology (NIST) [6]. The tester detects the failure event and removes the current from the device within 30 ns, thus preventing the device from being destroyed. This enables the same device to be tested for multiple failure conditions and prevents damage to the test circuit as a result of the device failures.

Figure 10 shows both the clamped and unclamped RBSOA test results for a 20 A/600 V rated Cool MOS device. For the clamped condition, the device can safely turn-off for currents up to 60 A and clamp voltage up to 700 V. The test conditions are limited to 60 A because the device current saturates at 60 A due to an internal JFET effect for gate voltage above 14 V. Thus, the CoolMOS has a *square RBSOA*, that is, it can switch safely for the full current and voltage range of the devices.

For the unclamped inductive switching case, the device safely sustains the avalanche condition with a breakdown voltage of 765 V (127 % of the rated voltage) for currents up to 15 A (75 % of the rated current) Above this current level, the device fails and is destroyed for the unclamped inductive condition. Although this represents a substantial avalanche energy capability, it falls far short of today's energy rated power MOSFET.

For unclamped inductive switching, the full inductor energy is transferred to the device resulting in rapid heating of the silicon chip voltage blocking region. In our RBSOA test condition, the energy for 15 A current and the 400 μH inductor is $E = 0.5 \times L \times I^2 = 0.045$ J. Assuming that the chip area heating is uniform, the temperature rise during the RBSOA test can be calculated as $E/(C \cdot A \cdot W) = 23$ °C, where the chip area is $A = 0.25$ cm^2, the voltage blocking junction depth (punch-through thickness) is $W = 50$ μm, and the silicon heat capacity is $C = 0.002$ J/°C,. However, the intrinsic temperature where the device fails for a drift region dopant density of 2×10^{14} cm^{-3} is 225 °C. This temperature difference indicates that the Cool MOS energy withstand capability is far below its intrinsic capability.

The reduced avalanche energy capability is possibly caused by non-uniform heating of the silicon chip voltage blocking region due to internal parasitic bipolar current constriction mechanisms. Today, high energy rated power MOSFETs have eliminated this bipolar current constriction mechanism and can withstand avalanche energies that uniformly heat the voltage blocking region to the intrinsic temperature before failure. However, early generations of power MOSFETs had substantially reduced avalanche capabilities. Presently available IGBTs also have limited avalanche energy capability, but it has been shown that better designs have improved avalanche energy capability to near the uniform heating limit [7]. At the present time, it is not clear whether the avalanche energy of the Cool MOS can also be increased, or whether there is a fundamental current constriction mechanism that cannot be eliminated just like the case with bipolar power transistors.

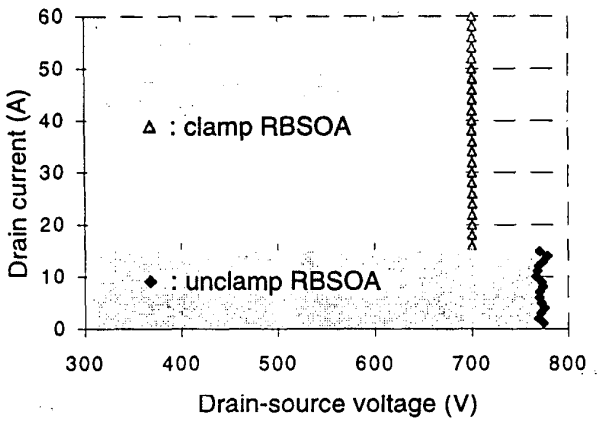


Figure 10. Clamped and unclamped RBSOA test results at 25°C.

VIII. Discussions and Conclusions

A new class of low on-resistance MOS-gated power devices has been characterized for both conduction and switching conditions. Its gate input characteristics and safe operating areas are also investigated for utilization concerns.

Experimental results indicate that the device conduction characteristics are similar to that of the power MOSFET but with a much lower on-resistance. Furthermore, unlike the IGBT, this new device does not exhibit junction voltage drop. For high power applications where paralleling is needed, the Cool MOS is found to be suitable because it has a positive temperature coefficient.

The switching characteristics of the new device are also similar to the MOSFET with fast switching speed and no tail current. However, for active snubbing using the gate drive resistance, the new device behaves like an IGBT, that is, its dv/dt is nearly constant for a wide range of gate drive resistance. The turn-off delay is proportional to the value of the gate drive resistance. However, the slope of the turn-off voltage rise varies only slightly when the gate drive resistance is increased to a very large value.

The Cool MOS exhibits excellent clamped RBSOA. Test results indicates that the device can sustain 300 percent of its rated current at a voltage 17 percent higher than its rated voltage, indicating that the device has a square RBSOA and very high pulse current switching capability.

For unclamped inductive switching, the sample device sustained an avalanche voltage 27 % higher than its rated voltage at about 75 % of its rated current. With a simple calculation of energy in unclamped RBSOA test, it was found that the Cool MOS energy withstand capability is far below its intrinsic capability. Such a low energy capability is possibly caused by non-uniform heating of the silicon chip in the voltage blocking region where an internal parasitic bipolar current constriction mechanisms exists. It remains to be seen whether the avalanche energy of the Cool MOS can be improved with better design or manufacturing just like the case with IGBTs, or whether there is a fundamental current constriction mechanism that cannot be eliminated just like the case with bipolar power transistors.

Overall, the device was found to behave more like a power MOSFET than an IGBT. The major similarity to the IGBT was in the active snubbing circuit utilization, where an external capacitance is required to reduce turn-off dv/dt in addition to the gate resistance.

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