An Active High-Voltage Divider with 20 μV/V Uncertainty

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***Abstract*—A voltage divider has been developed consisting of an external compressed-gas capacitor, a group of stable solid-dielectric capacitors, and special electronic circuitry. A developmental prototype divider has been constructed and test results obtained to verify the operating principle and accuracy target. The new critical items enabling the desired performance are the solid-dielectric capacitors in the low-voltage arm, approaching the short-term stability of gas-insulated capacitors, and the active circuit consisting of a feedback amplifier, complemented with a controlled source, which essentially removes the error contribution from the feedback amplifier.**

***Index Terms*—Compressed gas capacitor, electronic compensation, high-voltage divider.**

I. Introduction

A DEVELOPMENT was undertaken to produce an accurate and versatile voltage divider based on a compressed-gas high-voltage (hv) capacitor—a precision measurement component widely found in hv laboratories and test facilities but frequently underutilized in its potential applications. The specific goal was to design an instrument, which utilizes readily available components, to serve as an interface between the high-voltage capacitor and a precision multimeter or comparator for measuring 60 Hz high voltages with an accuracy typically available in laboratory-grade voltage transformers. The device could then be used as a laboratory standard for calibration of other voltage transformers and dividers. Advances in integrated circuits and introduction of stable ceramic-dielectric capacitors provided new tools for the realization of such a goal.

In a related earlier development [1], an active divider with polystyrene capacitors in the low-voltage arm and a feedback amplifier enhanced with a controlled source was built and used as a standard for calibration of test equipment to measure transformer losses. Ten years of successful use of that equipment and the stability of its components prompted the reexamination of this approach with a possibility of advancing its accuracy and versatility. In the present design the ratio stability is improved by using ceramic-dielectric capacitors with specified temperature dependence of $\pm 30 \times 10^{-6}$/K^{-1} or less. The input to the controlled source is obtained from the high-voltage capacitor in the divider without the use of a second hv capacitance element. The controlled source is designed to remain stable without adjustments during the operation.

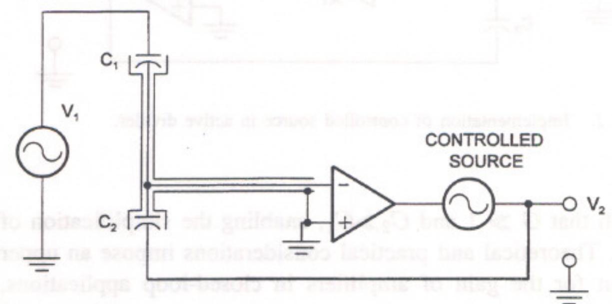

Fig. 1. Active divider with controlled source.

The actual instrument is a system consisting of the basic divider with a 12 V output, a 12 V inverter stage, and a 120 V output stage. This system provides considerable versatility in output voltage levels, polarity and divider ratios. Using 1000 pF and 100 pF hv capacitors and low-voltage capacitors of 0.1 μF to 2.0 μF, the available ratios of the basic divider range from 100/1 to 20 000/1 in steps of the multiples of 2, 5, 10, and their decade multiples. The output stage reduces all ratios and increases the output voltage by a factor of 10. The estimated uncertainty of the basic divider is within $\pm 20 \times 10^{-6}$, provided the divider is verified at low voltage during the test sequence. The use of both the inverter and output stages increases the uncertainty to within $\pm 30 \times 10^{-6}$. Tests on the system have validated the operating principle and the accuracy estimates.

II. Operating Principle

The evolution of the active circuits employed in this development is illustrated by the diagrams of Figs. 1 and 2. Conceptually, the active divider comprises a high voltage capacitor C_1 in series with a low voltage capacitor C_2 in the elementary operational amplifier circuit of Fig. 1 without the controlled source. This configuration ensures that the voltage of the junction point to ground is near zero yielding the voltage ratio

$$\begin{aligned}(V_2/V_1) &= -(C_1/C_2)[1 + (C_1 + C_2)/C_2 G]^{-1} \\ &\approx -(C_1/C_2)(1 - 1/G). \qquad (1)\end{aligned}$$

Here, G is the open-loop gain of the amplifier, and the typical component values encountered in this application are

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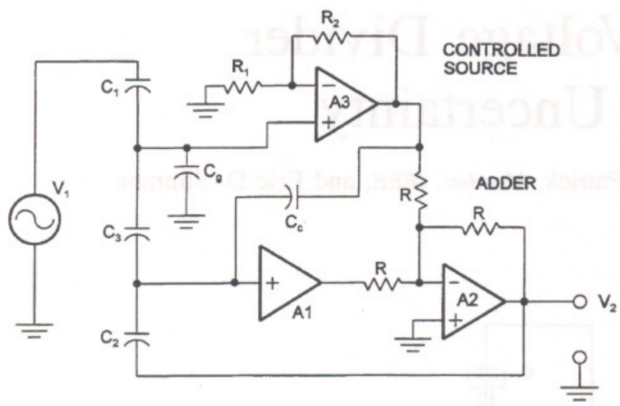

Fig. 2. Implementation of controlled source in active divider.

such that $G \gg 1$ and $C_2 \gg C_1$, enabling the simplification of (1). Theoretical and practical considerations impose an upper limit for the gain of amplifiers in closed-loop applications, which for typical general-purpose operational amplifiers at 60 Hz is 5000 to 10 000.

Numerous methods to overcome this limitation in precise measurements have been invented and utilized. For example, note the approaches described in [2], [3]. The method described in [1] uses the concept of a controlled voltage source, phase-locked to the input hv signal, that is inserted on an open-loop basis in the low-voltage arm of the divider to add to the amplifier output, as in the complete circuit of Fig. 1. If the voltage of this source is adjusted to the value $V_1(C_1/C_2)(1-d)$, where d is the small deviation from the desired exact value, the equation for the voltage ratio becomes

$$(V_2/V_1) \approx -(C_1/C_2)(1 - d/G). \tag{2}$$

It is relatively easy to obtain $d \leq 0.001$ and $G \geq 1000$ and a proportional difference between the ideal and actual ratios that is equal or smaller than 10^{-6}. The controlled source is implemented as an additional feedback amplifier and signal-adder circuits [1].

The previous circuit described in [1] requires two hv capacitors which are available in some capacitor structures as dual low voltage electrodes coupled to the same hv electrode. To accommodate most existing hv capacitors having a single low voltage electrode, an alternative was developed as shown in Fig. 2. A large-value, low-voltage capacitor, C_3, is inserted in series with C_1 to act as a voltage-sensing impedance for the controlled source. In such a circuit, the guard capacitance C_g to the junction of C_1, and C_3 becomes significant, causing the effective three-terminal capacitance, C_1', of the hv arm of the divider to become

$$C_1' \approx C_1[1 - (C_1 + C_g)/C_3]. \tag{3}$$

Neglecting the higher order terms in (3) is valid since typically C_1 has a value between 1000 pF and 100 pF, $C_g < 200$ pF, and $C_3 = 2\ \mu$F. The effective change in C_1 is less than 600×10^{-6} for a 1000 pF standard and less than 150×10^{-6} for a 100 pF standard. It can be treated either as a permanent augmentation to C_1 or removed with an additional compensating circuit. The simplest compensating circuit consists of a capacitor, C_c, having the value of $(C_1 + C_g)/(C_3/C_2)$ connected as shown in Fig. 2. Assuming such a compensation and adjusting the closed-loop gain of the amplifier A3 so that $(R_1 + R_2)/R_1 = C_3/C_2(1-d)$, we obtain the condition described by (2). In practice, the values for C_1' and the compensating capacitor, C_c, are determined by two direct measurements—of C_1 and C_1'. More complicated compensation, to maintain the junction between C_1 and C_3 at ground potential and thus remove the influence of C_3, is feasible.

The nominal output voltage of 12 V rms, rather than the more common 120 V for power equipment, was selected to essentially eliminate the voltage dependence of the capacitor C_2 in the low voltage arm. The 120 V output stage and the inverter are also constructed using similarly enhanced, but simpler, operational amplifier circuits with precision resistors as critical elements.

III. Construction Details

A. Basic Divider

The detailed circuit of the basic divider is shown in Fig. 3. The gain in the feedback loop is provided by the amplifier A1 which has local feedback—a double lag network—to stabilize the circuit at dc. A2 is the summing amplifier. The two amplifiers, A3 and A4, constitute the controlled source and provide the flexibility for coarse and fine gain and phase-angle control. Nominal gains of 1, 2, 5, 10, and 20 are available corresponding to C_2 values of 2, 1, 0.5, 0.2, and 0.1 μF. The output of A1 is monitored and reduced to zero by adjusting the gain of the controlled source. To accommodate five values of C_2, different sets of preadjusted variable-tap resistors ("trimpots"), designated R_1 in Fig. 3, are switched in as C_2 and the divider ratio are changed. The feedback impedances of A2 and A4 contain series RC circuits to stabilize the entire circuit at high frequencies.

B. Inverter and Output Stages

The inverting and output circuits are similar except for values of the analog computing resistances. The circuit of the output stage is shown in Fig. 4. Unlike in the previous circuit of Fig. 3, the function of the controlled source is combined with that of the adder. Fine adjustment of gain and phase angle of the controlled source is performed with the two variable-tap resistors. The closed loop gain (V_o/V_2) is equal to $-(R_2/R_1)(1 - d/G)$ and is analogous to that given in (2). The RC networks in the local feedback of A5 and A6 stabilize the feedback loop at high frequencies. Only the amplifier A6 needs to have the 120 V rms capability. In the inverter circuit the two 100 kΩ feedback resistors are replaced by 10 kΩ units and both amplifiers have 12 V rms capability.

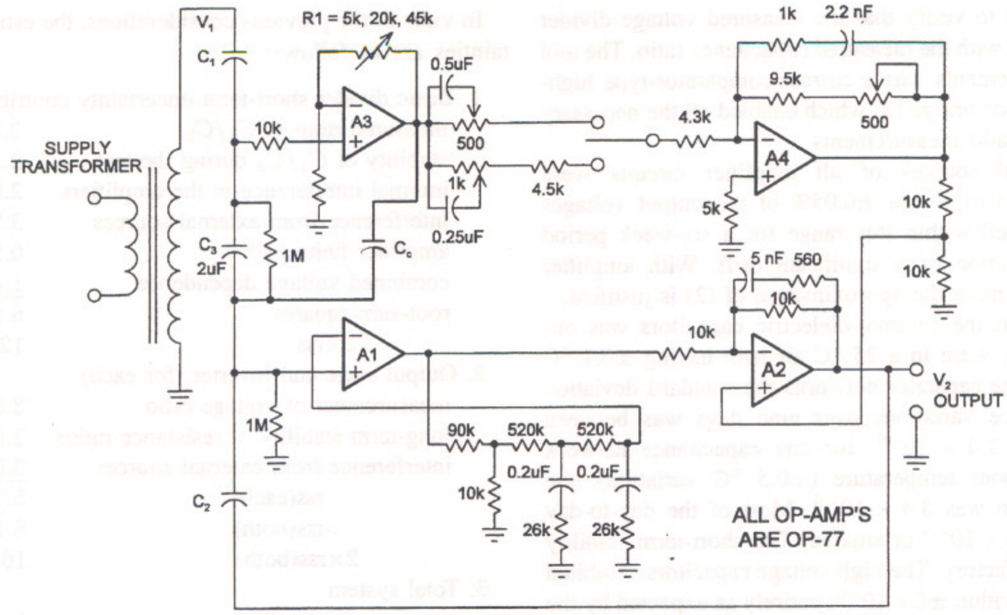

Fig. 3. Detailed circuit of basic divider.

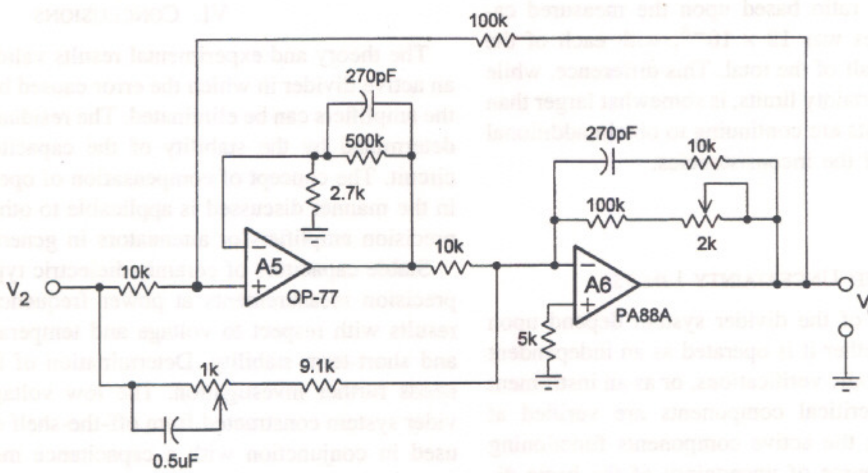

Fig. 4. Detailed circuit of output stage.

C. Low-Voltage Capacitor Networks

The basic components are 0.1 μF multilayer ceramic-dielectric capacitors designated by industry as "ultrastable COG"[1] type rated for peak voltage of 200 V and specified temperature dependence of $\pm 30 \times 10^{-6}/\mathrm{K}^{-1}$ or less. The criteria for this application were low temperature dependence and negligible voltage dependence, the latter being achieved by operating the capacitors below 10% of their rated voltage.

The ceramic dielectric capacitors and mica-dielectric trimming capacitors were connected in parallel to produce the required C_2 values for the capacitor in the low-voltage arm. Additionally, a capacitance-resistance-capacitance T-network for canceling the dissipation factor in the effective transfer capacitance was added to each network. The objective was to obtain the actual transfer capacitance value that is within $\pm 0.1\%$ of the nominal value and the dissipation factor that is within $\pm 10^{-6}$. The combined circuits are wired as four-terminal-pair networks.

IV. Summary of Tests and Results

Preliminary tests have been performed to verify that the system functions as predicted by the theory, to demonstrate that the error contribution by the active part of the circuit can be reduced to negligible portions, to establish the stability limits of the critical capacitors, especially those in the low

[1]Certain commercial materials are identified for completeness. In no case does this identification imply a recommendation by the National Institute of Standards and Technology, nor does it imply that the materials are the best available.

voltage arm, and to verify that the measured voltage divider ratio corresponds with the measured capacitance ratio. The tool for these measurements was a current-comparator-type high-voltage capacitance bridge [3] which enabled all the necessary impedance and ratio measurements.

The controlled sources of all amplifier circuits were orginally adjusted to within ±0.05% of the output voltages and have remained within this range for a six-week period without an indication of a significant drift. With amplifier gains of 1000 or more the approximation of (2) is justified.

The stability of the ceramic-dielectric capacitors was observed while they were in a 25 °C air bath having ±0.1 °C variation. for three capacitor networks the standard deviation of the capacitance variations over nine days was between 2.6×10^{-6} and 3.0×10^{-6}. for one capacitance network maintained at room temperature (±0.5 °C variation), the standard deviation was 3.4×10^{-6}. Most of the day-to-day variations were 2×10^{-6} or smaller. The short-term stability was entirely satisfactory. The high voltage capacitors exhibited small variations within $\pm 3 \times 10^{-6}$, entirely as expected by the variations in the room temperature.

The proportional difference between one measured voltage ratio of the combination of the basic divider and the output stage and the calculated ratio based upon the measured capacitances and resistances was 19×10^{-6}, with each of the stages contributing one half of the total. This difference, while within the estimated uncertainty limits, is somewhat larger than realistically expected. Tests are continuing to obtain additional data and resolve some of the inconsistencies.

V. Estimated Uncertainty Limits

The uncertainty limits of the divider system depend upon the operating mode—whether it is operated as an independent instrument with only periodic verifications, or as an instrument in which some of the critical components are verified at the time of its use. With the active components functioning properly, the principal source of uncertainty of the basic divider is associated with the knowledge of the two capacitance values.

Both low and high voltage capacitors exhibit excellent short-term stabilities in a laboratory space with moderate temperature control, e.g., ±0.5 °C. Experience has also shown that properly maintained high voltage capacitors do not have significant long-term variations. However, long-term data are not available for the ceramic-dielectric capacitors being utilized. Hence, any long- or short-term operation should include capacitance or ratio verifications at low voltage. At NIST this is done using the current-comparator-type of capacitance bridge. A dedicated calibrator—a resistive or transformer-type divider for 1000 V—is being investigated.

The inverter and the output stage are devices with fixed voltage ratios which depend on the ratio of two precision resistances. Initial determination of their resistance ratio is performed at ac and dc, but subsequent monitoring can be done at dc only. Long-term stability is predictable from the components being used.

In view of the previous considerations, the estimated uncertainties are as follows:

1. Basic divider short-term uncertainty contributions	
measured ratio of C_1/C_2	3.5×10^{-6}
stability of C_1/C_2 during the test	2.1
internal interference in the amplifiers	2.8
interference from external sources	3.5
amplifier finite gain	0.5
combined voltage dependence	1.4
root-sum-squares	6.2×10^{-6}
2×rss	12.4×10^{-6}
2. Output stage and inverter (for each)	
measurement of voltage ratio	3.5×10^{-6}
long-term stability of resistance ratios	2.8
interference from external sources	3.5
rss(each)	5.7×10^{-6}
rss(both)	8.1×10^{-6}
2×rss(both)	16.2×10^{-6}
3. Total system	
rss(all)	10.2×10^{-6}
2×rss(all)	20.4×10^{-6}

VI. Conclusions

The theory and experimental results validate the concept of an active divider in which the error caused by the finite gain of the amplifiers can be eliminated. The residual error is primarily determined by the stability of the capacitors in the divider circuit. The concept of compensation of operational amplifiers in the manner discussed is applicable to other devices such as precision amplifiers or attenuators in general.

Stable capacitors of ceramic-dielectric type were utilized in precision measurements at power frequencies with excellent results with respect to voltage and temperature dependences, and short-term stability. Determination of long-term stability needs further investigation. The low voltage part of the divider system constructed from off-the-shelf components, when used in conjunction with a capacitance meter or equivalent instrument, can broaden the uses of high voltage capacitors to precision ratio measurements in the $\pm 10^{-4}$ to $\pm 10^{-5}$ uncertainty range.

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