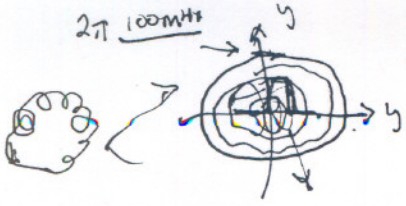
THAM 3-10



Phase Plane Compensation of the NIST Sampling Comparator System

J. P. Deyst and T. M. Souders
National Institute of Standards and Technology[1], Gaithersburg, MD

Abstract This paper describes a compensation method to improve the static and dynamic linearity of the response of an equivalent-time digitizer. The nonlinearity of the digitizer response is represented in a multidimensional lookup table as a function of digitizer state and appropriate parameters, such as the instantaneous signal value and slope. In operation, the lookup table is used to compensate for the nonlinearity of the digitizer response by subtracting the appropriate table value from each new sample taken of the input signal. A second lookup table can be added to compensate digitizer timebase nonlinearity. The digitizer being compensated is a sampling comparator system that produces noticeable distortion in signals such as high frequency sine waves. The performance of the compensated sampling comparator system will be presented, for a range of input test signals having a variety of trajectories in the phase plane.

Introduction

The U. S. National Institute of Standards and Technology developed a Sampling Comparator System[1] after demonstrating, along with other laboratories[2-4], that very high performance sampling of repetitive waveforms could be achieved with an analog latching comparator in a feedback arrangement. The Sampling Comparator System (SCS) is an equivalent-time digitizer consisting of a latching comparator in a successive approximation loop, as shown in figure 1. The comparator has high bandwidth (2.5 GHz) and features very fast settling response (0.2% in 2 ns) for accurate acquisition of fast step and pulse waveforms.

The main sources of nonlinearity in the SCS are the comparator circuit and the timebase. The comparator circuit is specially designed for high linearity[1], but it does have some low level dynamic nonlinearity as evidenced by harmonic distortion of high frequency sine wave signals. Timebase nonlinearity adds some additional nonharmonic distortion.

"Phase plane" compensation, properly implemented, should correct for much of the nonlinearity of the comparator circuit. Phase plane compensation (PPC) is the use of a multidimensional lookup table, which stores estimated linearity errors indexed by selected parameters of the signal. Rebold and Irons[5] originally developed PPC for correction of nonlinearities in high speed analog-to-digital converters(ADCs). Subsequent research has improved tailoring of PPC to ADC error sources[6], and made important algorithmic improvements[7]. Significant results include increases in ADC spurious-free dynamic range (SFDR) by 10 dB over bandwidths of 40 MHz[6] and 80 MHz[7]. Two areas that are key to good results are (i) selecting the appropriate table indices, and (ii) correctly estimating the linearity errors to be used in the lookup table.

PPC can be augmented to correct for timebase nonlinearity by the addition of a second lookup table that is indexed by the estimated slope of the signal and by relevant timebase parameters. Related techniques of characterization and correction of digitizer timebase nonlinearity have been extensively researched (e.g., [8-10] and their references).

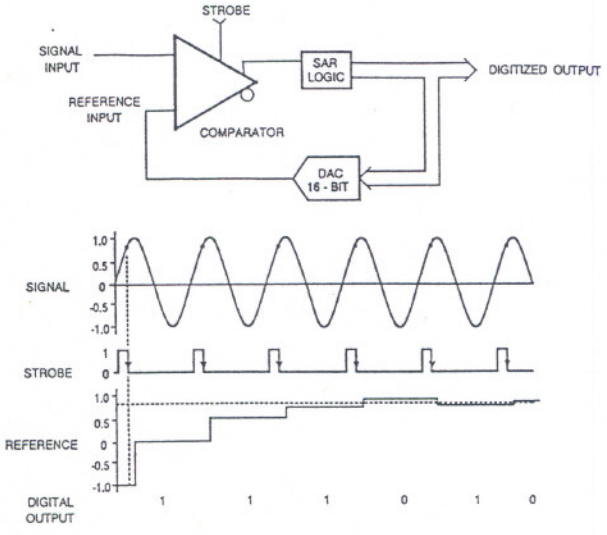


Figure 1: Diagram of the sampling comparator and successive approximation loop (above) and diagram of its search routine (below).

Sampling Comparator System

The SCS consists of a probe and a mainframe connected together by an umbilical cable. The probe houses the comparator, which is a custom-designed integrated circuit. The mainframe consists of the successive approximation logic, the reference digital-to-analog converter (DAC), and the system timebase and trigger, and is implemented with a commercially available waveform analyzer. The probe and umbilical arrangement permits the comparator to be connected directly to the source of the signal to be measured[1].

The method of successive approximation equivalent-time sampling is described in detail in [4]. The DAC resolution is 16 bits, and the timebase equivalent-time resolution is 10 ps.

A simplified diagram of the comparator circuit is shown in figure 2. It has an input range of ±2 V and features an innovative enabling technique that minimizes "thermal tail" settling errors. The comparator is implemented using commercial Si processing, with transistor f_Ts of up to 8.5 GHz. The dominant nonlinear error sources in the comparator have not yet been determined.

The effects of the comparator and timebase nonlinearities depend on the input signal amplitude and frequency and on the timebase length. For near-fullscale (3.9 Vpp) sine waves, with frequencies f_{in} lower than about 10 MHz, the timebase nonlinearity is the dominant error source. For example, typical measured signal-

[1]U. S. Department of Commerce, Technology Administration

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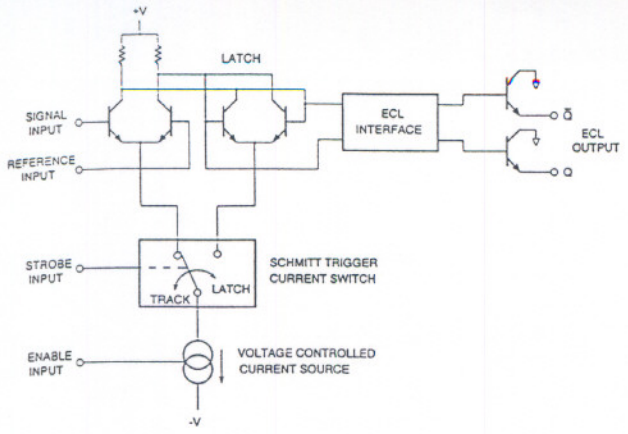

Figure 2: Simplified diagram of the comparator circuit.

to-noise ratios (SNRs) at f_{in} = 1 MHz are 71 dB for a 2 μs timebase versus 64 dB for a 10 μs timebase. Corresponding measured SFDR values are 83 dB and 68 dB, respectively. Harmonic distortion dominates at input frequencies greater than about 10 MHz and typical timebase settings. For 3.9 Vpp sinewaves, typical measured SNR values are 47 dB at f_{in}= 50 MHz and 36 dB at f_{in} = 100 MHz. Corresponding SFDR values are 47 dB and 37 dB, respectively.

Phase Plane Compensation

Contents of PPC lookup tables typically are stored in a defined set of locations in digital memory. The table indices are values derived from signal parameters such as the instantaneous signal value and slope at the sampling instant.

Prior to using PPC, the digitizer error estimates must be generated and entered into the lookup table. Error estimates are generated by stimulating the digitizer with a known calibration input, such as a sine wave, and acquiring records of the corresponding digitizer output samples. An estimate of the linear response part of the output is subtracted from each output record, leaving estimates of the linearity errors. Each error estimate is entered into the table location indexed by the values of the signal parameters at the moment the error occurred. The input signal has to be varied during table generation, in order to fill the space of the table reachable by the variety of signals expected during operation. Typically this is done by using a sinewave frequency equal to the maximum signal frequency expected during operation, and by decrementing the amplitude of the sine wave in many steps from fullscale to nearly zero[5]. For each amplitude a record of estimated errors is generated and stored in the table. Since multiple error estimates are entered into the bins during table generation, typically all the entries to each bin are averaged to make a final error estimate for that bin. Errors from timebase nonlinearity have to be corrected before the error estimates are entered into the table; alternatively, at each amplitude step sine waves could be acquired with various starting phases, so as to average out the unwanted contributions of timebase errors.

During PPC operation, the signal parameters are determined for each digitizer output sample, and the table is accessed for the corresponding error estimate that is then subtracted from the output sample to produce a corrected sample value.

Proper selection of table indices is key to successful implementation of PPC. Previous analysis suggests that the best signal parameters for use as indices for comparator nonlinearity are the present sample value and estimated slope[6]. Notably, it appears that the nonlinearity is not dominated by error sources that are difficult for PPC to compensate: thermal tails, metastability, and decode errors from thermometer code glitches[6].

Another key to successful implementation of PPC is the estimation, during generation of the table, of the linear response part of the digitizer output. If the estimation is incorrect, the wrong values are subtracted from the output, producing incorrect error estimates in the lookup table. For instance, the linear portion of the output is commonly estimated by the component of the output's Discrete Fourier Transform corresponding to the input frequency, or by the least-squares sine-fit: these are generally incorrect estimates[6,7]. Important recent work by Hummels et al[7] on error estimation has produced improved algorithms and higher distortion reductions over wide bandwidths.

Timebase nonlinearity can also be compensated by an additional lookup table indexed by the timebase setting, the position of a given sample in the timebase, and the estimated slope of the signal at the sampling instant. This table can be characterized with sine waves of various phases, with the results averaged so as to minimize the contribution of comparator errors to the estimates of timebase error[10]. In operation, an error estimate from this table is also subtracted from each digitizer sample.

If PPC reduces distortion significantly over a wide bandwidth, then the lookup table or tables are implicitly a good description or map of the digitizer's nonlinearity. Thus, PPC lookup tables could serve as a standard method of representing digitizer nonlinearity. Also, the digitizer's nonlinear error sources might be identified from patterns in the error estimates.

Implementation

Figure 3 shows the present implementation of phase-plane compensation for the SCS. The table generation input is a

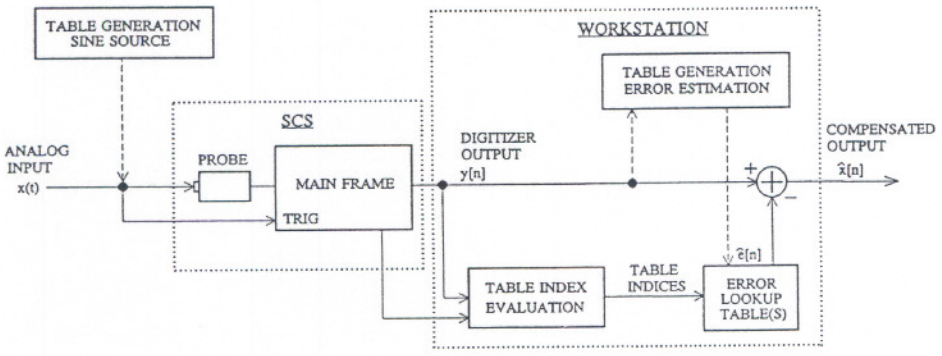

Figure 3: Diagram of the application of phase plane compensation to the Sampling Comparator System.

synthesized sinewave, filtered for high spectral purity. The compensation experiments are implemented using a computer workstation with digital signal processing software. Compensation in these experiments is carried out over bandwidths in the 100-200 MHz range. This range is less than the digitizer's maximum bandwidth of 2.5 GHz, but is sufficient to compensate many signals now typically measured, even including outputs caused by very fast step inputs (~2000V/μs). There are no known barriers to extending the compensation to higher bandwidths.

Results of the application of PPC to the SCS will be presented, for a range of test signals having a variety of trajectories in the lookup table space. The results of applying different methods of input estimation during table generation will also be presented, along with results of attempted identification of the dominant error sources.

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