

DIGITAL SOURCE FOR A NEW IMPEDANCE BRIDGE

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Abstract

A digitally-synthesized source has been designed to provide two sinewave outputs with an accurately known adjustable phase shift in the second channel for use with a proposed new impedance bridge.

Introduction

Recently a new design for an impedance bridge has been proposed for the calibration of inductance standards at NIST. The calibration requirement is for the measurement of the self-inductance of inductance standards in the range of 10 μ H to 10 H over the frequency range of 66 Hz to 20 kHz. (The frequency range is restricted for some inductances.) This new bridge is a modification of an earlier design proposed by Free, but this one uses two digitally synthesized sinewave sources (DSS) to eliminate one of the two inductive voltage dividers (IVD) of the original design [1].

As this bridge design (Fig. 1) has not been previously published, a limited description follows. The operating procedure requires two balances in sequence. The detector is first switched to A and the source magnitudes V_{REF} and V_{VAR} and the phase of V_{VAR} are adjusted to null the detector. Then, the detector is switched to B and the IVD and phase of V_{VAR} are adjusted to produce a second null. If the magnitudes of V_{REF} and V_{VAR} remain stable between the two balances the impedance Z is proportional to the IVD and phase settings and resistance standard R .

Source Requirements and Design

The requirements for the sources are therefore: good

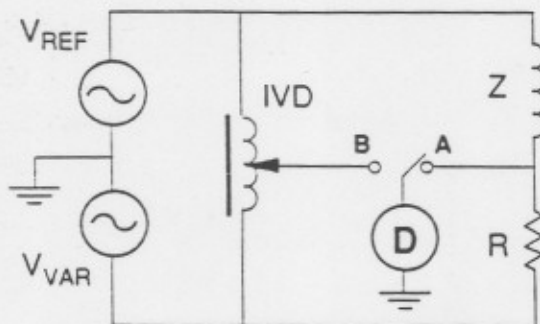


Fig. 1. Simplified diagram of the proposed impedance bridge.

short-term amplitude stability relative to each other, adjustable (but not necessarily calibrated) amplitudes, accurately adjustable phase change of V_{VAR} , and 200 mA output for driving low-impedance loads. The design of the source is simplified considerably because accuracy is required only for the change in phase of V_{VAR} between the two balances. However, a phase change accuracy of 10 μ rad at 1 kHz is typically needed to achieve 1 part-per-million (ppm) accuracy in the anticipated inductance measurements.

The design of the source exploits the ability of digitally synthesized sources to produce accurate changes in phase. Our source uses as a building block a design by one of the authors that was originally produced for a transportable ac voltage standard [2]. This new design (Fig. 2) uses three similar sources with additional circuitry to provide an adjustable phase angle between the two channels. Not shown in Fig. 2 is the bus network and circuitry used to control the frequency, phase angle, and magnitudes of the sources via the IEEE-488 bus.

The sinewave output of each DSS is produced by a digital counter, a sine table stored in read-only-memory (ROM), and two 16-bit multiplying digital-to-analog converters (DAC). A master dc reference is supplied to all three DSSs and a third 16-bit DAC in each DSS scales the reference input to the other DACs to adjust the ac amplitude. An adjustable clock incre-

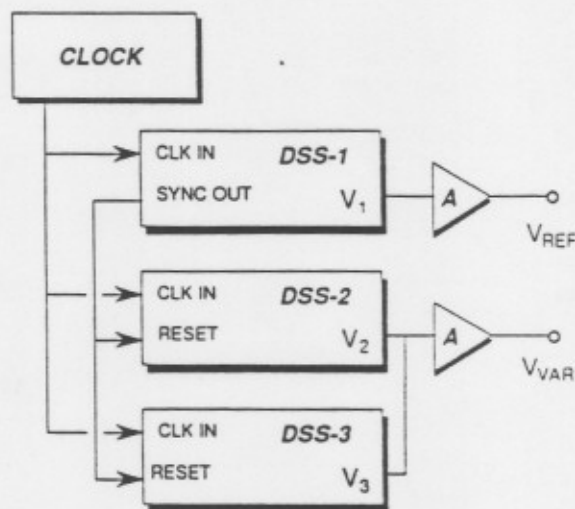


Fig. 2. Block diagram of the two channel phase-controllable source using three digitally synthesized sources.

ments the ROM address counter in each DSS, presenting successive sine values from the ROM to the DACs for conversion to an analog signal. Successive steps are routed to alternate DACs to deglitch the output voltage and to increase the maximum operating frequency. A buffer amplifier and filter (A in Fig. 2) boost the current capability to 200 mA and reduce the distortion due to sampling harmonics.

The phase angle between the two channels is varied by offsetting the ROM address counter in DSS-2 by an integral number of counts with respect to DSS-1. The phase resolution of this method is limited by the number of sine values generated per period (about 6 mrad for a 1024-step waveform). Additional resolution may be achieved by changing the contents of the ROM in DSS-2; however, this approach often produces small changes in the magnitude of V_2 which are not easily predicted. If the magnitude of V_2 changes between balances, it will lead to a proportional error in the impedance measurement. Therefore, the ROM values are fixed and a third source, DSS-3, has been combined with DSS-2 to provide additional phase resolution without changing the magnitude of V_2 .

DSS-3 is operated nearly in quadrature with DSS-2 and its amplitude is scaled to be a small fraction of DSS-2. The combined output can be expressed by,

$$V_{VAR} = V_2 \sin(\omega t + \phi) + V_3 \cos(\omega t + \phi + \zeta)$$

where ϕ and $\phi + \zeta$ are the phase angles of DSS-2 and DSS-3, respectively.

This reduces to the form,

$$V_{VAR} = V_0 \sin(\omega t + \phi).$$

Coarse adjustment of ϕ (and hence ϕ) is accomplished using the previously discussed counter offset method. Fine adjustment of ϕ (interpolation between coarse steps) is made by adjusting V_3 and ζ to obtain the desired ϕ while keeping $|V_{VAR}|$ constant. An inaccuracy in the magnitude of V_3 will produce an error in ϕ but this error is negligible if $|V_3| \ll |V_2|$ as is the case here.

Conclusions

A test-bed wire-wrapped version has been constructed and demonstrates stability and noise of 0.5 ppm (rms) over a one hour period. Complete results from a printed circuit version will be presented at the Conference.

References

- [1] G.M. Free, "A High Accuracy, Easy to Use, 100 Hz to 100 kHz Inductance Bridge," *CPEM 84 Digest*, 1984.
- [2] N.M. Oldham, P.S. Hetrick, X. Zeng, "A Calculable, Transportable Audio-Frequency AC Reference Standard," *IEEE Trans. Instrum. Meas.*, Vol. 38, No. 2, pp. 368-371, Apr. 1989.

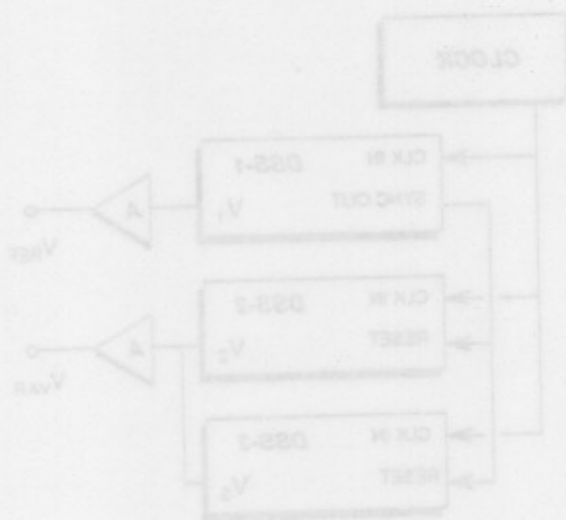


Fig. 2. Block diagram of the two channel phase-convertible source using three digitally synthesized sources.

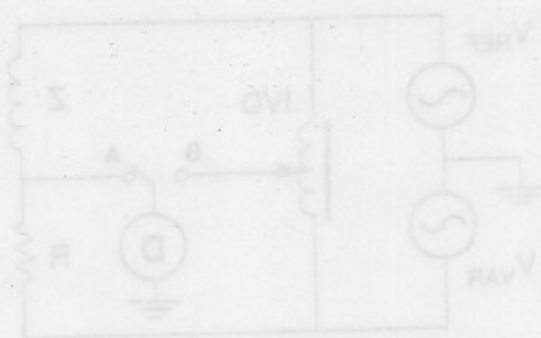


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