Thermal Component Models for Electrothermal Network Simulation

Allen R. Hefner, *Senior Member, IEEE*, and David L. Blackburn, *Fellow, IEEE*

***Abstract*—A procedure is given for developing thermal component models for electrothermal network simulation. In the new electrothermal network simulation methodology, the simulator solves for the temperature distribution within the semiconductor devices, packages, and heat sinks (thermal network) as well as the currents and voltages within the electrical network. The thermal network is represented as an interconnection of compact thermal component models so that the system designer can readily interchange different thermal components and examine different configurations of the thermal network. To facilitate electrothermal network design, the interconnection of the thermal component models is specified by the user in the same way that the interconnection of the electrical network components is specified. The thermal component models are also parameterized in terms of structural and material parameters so that the details of the heat transport physics are transparent to the user. Examples of electrothermal network simulations are given, and the temperature measurement methods used to validate the thermal component models are described.**

I. Introduction

NETWORK simulation programs such as the simulation program with integrated circuit emphasis (SPICE) have traditionally been used to simulate electronic circuits using detailed physics-based semiconductor device models. Although the semiconductor device models include temperature dependence in the traditional approach, the temperature used by the device models is chosen by the user and remains constant during the simulation. Recently, though, a new methodology has been developed for simulating the dynamic electrothermal behavior of electronic systems [1]. In the new methodology, the simulator solves for the temperature distribution within the semiconductor devices, packages, and heat sinks (thermal network) as well as the currents and voltages within the electrical network. The purpose of this paper is to describe the method for developing compact physics-based thermal component models for incorporation into thermal component libraries of advanced network simulation programs [2].

Temperature is a critical parameter in determining the electrical behavior of semiconductor devices. However, the effects of temperature are not adequately described using the traditional user-defined device temperature because the devices are often heated significantly by the power dissipated within the device (self-heating) and by the power dissipated in adjacent semiconductor devices (thermal coupling). Therefore, the device temperature depends upon the circuit operation and does not remain constant for dynamic operating conditions. The approach used in the new electrothermal network simulation methodology is to define the temperatures at various positions within the silicon chips, packages, and heat sinks (thermal network) as simulator system variables so that the dynamic temperature distribution within the thermal network is solved for by the simulator in the same way that the node voltages within the electrical network are solved.

The new methodology enables the designer to incorporate thermal management considerations into the design of electronic systems. For example, the designer can readily interchange semiconductor devices having similar electrical characteristics but with different chip areas and thus different thermal characteristics. The designer can also interchange thermal network components such as packages and heat sinks and can change the topology of the thermal components within the thermal network. For example, the behavior of a system including thermal coupling between adjacent electrical devices mounted on a single heat sink can be compared with the behavior of the same system but with the devices having separate heat sinks. However, the electrothermal simulation capability will become a more useful design tool when models are avaliable in simulator component libraries for all of the standard thermal components used for typical system designs.

The method used to develop electrothermal models for semiconductor devices was described in detail in [3]. In this paper, the techniques used to develop the thermal network component models for the silicon chip, packages, and heat sinks are described. The methods used to implement these models into the Saber[1] circuit simulator are also described. It is shown that these model development techniques can be used to develop libraries of thermal component models for network simulation programs. In addition, various methods used to measure the temperature within the thermal network to validate the thermal models are discussed. The electrothermal models and thermal network component models developed in this paper and in [3] are provided in the template libraries of Saber version 3.2 [2].

II. Electrothermal Simulation Methodology

Fig. 1 is a diagram of the electrothermal network simulation methodology indicating that the electrical and thermal networks are coupled through the electrothermal models for the semiconductor devices. The electrothermal models

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The authors are with the Semiconductor Electronics Division, National Institute of Standards and Technology, Gaithersburg, MD 20899 USA.

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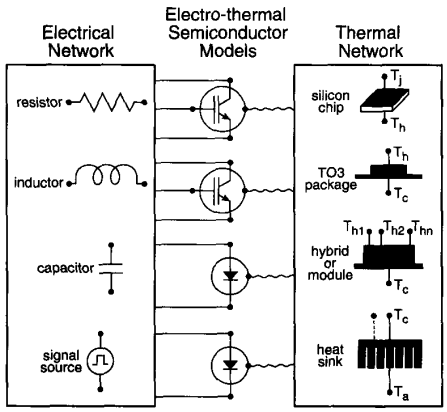
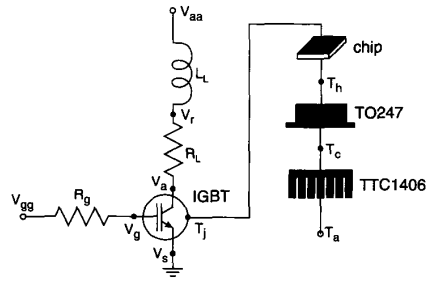


Fig. 1. Diagram indicating the interconnection of the electrical network with the thermal network through the electrothermal models for the semiconductor device, where the types of components within each network are indicated.

for the semiconductor devices (e.g., power insulated gate bipolar transistors (IGBT's) and power diodes in Fig. 1) have electrical terminals that are connected to the electrical network and a thermal terminal that is connected to the thermal network. The thermal network is represented as an interconnection of thermal components so that the system designer can readily interchange different thermal components and examine different configurations of the thermal network. The thermal network models for power modules and heat sinks contain multiple terminals and account for the thermal coupling between the adjacent semiconductor devices. To simplify the system design process, the thermal component models are represented in the same form as the electrical component models, and the details of the thermal component model physics are transparent to the user. However, the structural and physical parameters of the thermal models enable the user to provide the specific information necessary to perform accurate simulations.

As an example, Fig. 2(a) is a schematic of an electrothermal network, and Fig. 2(b) is the corresponding Saber simulator netlist using the IGBT electrothermal model [3] and the thermal component models of the silicon chip, the TO247 package, and the TTC1406 heat sink. The first column of the Saber netlist in Fig. 2(b) specifies the name of the template that contains the model equations for each component (left-hand side of the period) and the instance within the circuit (right-hand side of the period). The remaining columns on the left-hand side of the equals sign indicate the terminal connection points of the components within the network, where the electrothermal IGBT model is connected to both the electrical and thermal networks. The parameters used by the model templates to describe the specific components are listed on the right-hand side of the equals sign. For example, the chip area, chip thickness, and chip location on the package are changed from their default values. It is evident from Fig. 2 that the thermal network component models are interconnected to form the thermal network in the same way as the electrical components are interconnected to form the electrical network.

Because power semiconductor devices dissipate a considerable amount of heat, the electrothermal network simulation



(a)

```
#IGBT electro-thermal simulation

#Electronic network components
v.vaa          vaa  0          = 300
l.ll           vaa  vr         = 80u
r.rl           vr   va         = 30
r.rg           vgg  vg         = 10
pulsgen.1      vgg  0          = 20

#IGBT electro-thermal model
igbt_therm.1  va   vg   0  tj = tauhl_1=1.6,
                                kp_1=1.5

#Thermal network components
chip_therm.1      tj   th      = thick=0.05,
                                 a_chip=0.1
to247_therm.1     th   tc      = a_chip=0.1,
                                 ychedm=0.2
ttc1406_therm.1   tc   ta      = a_heat=0.4
t.ta              ta   0       = 300
```

(b)

Fig. 2. (a) Schematic and (b) netlist for an example electrothermal network using the IGBT electrothermal model and the thermal component models of the silicon chip, the TO247 package, and the TTC1406 heat sink.

methodology was developed first for power semiconductor devices and standard power device packages. However, the new methodology is applicable to all areas of electronics for which thermal management is important in the design of the overall system. Because the electrothermal semiconductor models reduce to the traditional constant-temperature semiconductor models by connecting the thermal terminal to a constant-temperature source, all of the traditional global-temperature-dependent models in circuit simulators can be replaced by the electrothermal semiconductor models. This will give the system designer the ability to specify a different operating temperature for each semiconductor device by connecting a different constant temperature source to each thermal terminal, and the ability to incorporate thermal management considerations at any point in the design process by connecting the thermal network to the thermal terminals of the appropriate semiconductor devices.

III. Electrothermal Semiconductor Models

This section briefly describes the development of dynamic electrothermal models for semiconductor devices. A more detailed description of electrothermal semiconductor model development and a complete description of the IGBT electrothermal model are given in [1] and [3].

Fig. 3 is a diagram of the structure of the electrothermal semiconductor device models indicating the interaction with the thermal and electrical networks through the elec-

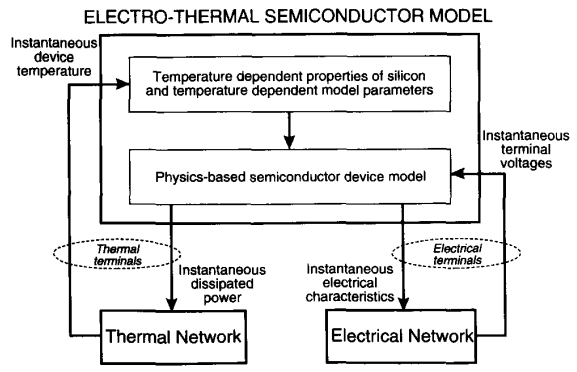


Fig. 3. Diagram of the structure of the electrothermal semiconductor device models indicating the interaction with the electrical and thermal networks.

trical and thermal terminals, respectively. The electrothermal semiconductor models use the instantaneous device temperature (temperature at the silicon chip surface T_j) to evaluate the temperature-dependent properties of silicon and the temperature-dependent model parameters. These temperature-dependent values are then used by the physics-based semiconductor device model to describe the instantaneous electrical characteristics and the instantaneous dissipated power. The dissipated power is calculated from the internal components of current because a portion of the electrical power delivered to the device terminals is dissipated as heat and the remainder charges the internal capacitances. The dissipated power calculated by the electrical model supplies heat to the surface of the silicon chip thermal model through the thermal terminal.

The electrothermal semiconductor models are implemented into the Saber circuit simulator by expressing the components of current flow between the electrical nodes and the components of power into thermal nodes in terms of the simulator system variables. Simulator system variables are the voltages across the electrical nodes, the temperatures across the thermal nodes, and additional system variables that are defined to solve implicit model equations. The simulator solves the system of electrothermal equations by iterating the system variables until the components of currents into each electrical node sum to zero (Kirchhoff's current law) and the components of power flow into each thermal node sum to zero (energy conservation). The thermal nodes have units of temperature (K) across the nodes and units of power (W) flowing through the nodes, whereas the through and across variables for electrical networks are current and voltage.

The temperature-dependent expressions for the physical properties of silicon and the expressions for the temperature-dependent model parameters indicated in Fig. 3 are defined in [3] for the IGBT model. The temperature-dependent properties of silicon are well known, and the temperature-dependent model parameters are obtained by using the extracted values of the model parameters versus temperature [3]. An accurate extraction sequence [4] is required to resolve the temperature dependence of the model parameters. The advantage of using a physics-based model for the semiconductor devices is that the well-known temperature-dependent properties of silicon can be used to describe the temperature dependence of the model, and only a few temperature-dependent model parameter expressions must be developed. Conversely, semiconductor models that rely heavily on empirical-based formulas require calibration of each of the empirical formula versus temperature.

IV. Thermal Network Component Models

In the new electrothermal network simulation methodology, the thermal network is represented as an interconnection of thermal component models where each component represents an indivisible building block used by the designer to form the thermal network (see Fig. 1). The goal of the new methodology is to produce accurate, computationally efficient, and easy-to-use thermal models (*compact models*) so that the designer can use them effectively in the design of large electrothermal networks. The component models should also be valid for the full range of applicable use conditions of the component, so that the designer need not be concerned with the limitations of the models. In the new methodology, a grid spacing that increases logarithmically with distance from the heat source is used to minimize the number of thermal nodes required to represent the temperature distribution for the full range of applicable power dissipation levels.

Fig. 4 is a diagram of the structure of the thermal component models, indicating that the thermal component models interact with the external thermal network through thermal terminals T_1, T_2, $\cdots$, T_n. The terminals of the thermal component can be connected to the thermal terminals of other thermal component models, to the thermal terminals of electrothermal models, or to thermal element models such as temperature sources. The thermal network models for power modules and heat sinks contain multiple terminals and account for the thermal coupling between the adjacent semiconductor devices (Fig. 1). To use the thermal component models, the designer needs only to specify the connection points of the thermal terminals within the thermal network and the structural and material parameters of the model. The user-defined structural and material parameters are used by the model to determine the heat diffusion equation discretization coefficients. The thermal models also provide an output list of internally calculated parameters, such as the thermal node positions, that are useful for interpreting the simulated temperature waveforms.

A. Modeling Methodology

The thermal network component modeling methodology is based on several innovations that result in accurate, computationally efficient, and easy-to-use thermal component models. In the new methodology, the temperatures at various positions within the silicon chips, the device packages, and the heat sinks are defined to be simulator system variables, so that the temperature distribution is solved for by the simulator in the same manner as the simulator solves for the node voltages of the electrical network. The equations describing the heat flow between the internal thermal nodes and the heat storage at the thermal nodes are obtained by discretizing the nonlinear heat diffusion equation. In the discretization

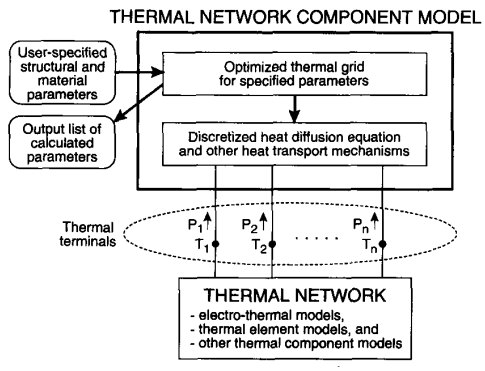


Fig. 4. Diagram of the structure of the thermal component models, indicating that the user only needs to specify the structural and material parameters of the models and the connection points of the thermal terminals, T_1, T_2, $\cdots$, T_n, within the network.

process, a grid spacing that increases logarithmically with distance from the heat source is used to maximize computation efficiency and to accurately represent the dynamic temperature distribution for the applicable range of heating rates. Finally, the thermal network is represented by an interconnection of thermal component models for the device silicon chips, device packages, and heat sinks, where the individual component models are parameterized in terms of structural information. Hence, the user needs only to specify the interconnection of the thermal components and the values of their structural parameters to represent thermal networks.

Traditionally, several other methods have been used for solving the heat diffusion equation to describe the temperature of semiconductor devices. These methods include 1) steady-state Fourier series solution [5], 2) convolution of the thermal step response with analytical power dissipation functions [6], 3) empirical extraction of thermal network element values from the measured thermal step response [7], 4) physics-based thermal resistance and thermal capacitance network element analysis [8], and 5) three-dimensional finite difference and finite element simulation [9]. However, each of these methods has limitations that prevent efficient dynamic electrothermal simulation. The first method is very efficient for three-dimensional steady-state thermal analysis, but is not applicable to dynamic thermal conditions. The second method is useful for analytical calculation of the dynamic temperature distribution from predetermined power dissipation functions, but is valid only for linear materials and would require the evaluation of a convolution integral by the circuit simulator, which is inefficient.

Methods 3) through 5) are numerically similar to the thermal network component modeling methodology used in this work in that they result in a finite number of state equations (coupled first-order ordinary differential equations) that are numerically integrated by the simulator to determine the evolution of the temperature distribution in terms of the instantaneous power dissipation. However, methods 3) through 5) do not result in compact models that are parameterized in terms of structural information and that are both accurate and computationally efficient. For example, the third method uses an assumed thermal network that may not have adequate precision to describe the nonquasistatic heating for high-power dissipation levels. The fourth method can be used to derive accurate thermal network models from structural and material information but requires the user to analyze each thermal resistance and thermal capacitance element of each component in the network. The fifth method is generally applicable to three-dimensional structures and nonlinear materials, but is computationally inefficient and requires the user to generate a structural model and an accurate element mesh.

B. Thermal Model Development

In the new methodology, the thermal network component models are derived from the heat diffusion equation using the component geometry, the nonlinear thermal properties of the materials, and other nonlinear heat transport mechanisms such as convection. The three-dimensional heat flow is accounted for using appropriate symmetry in the discretization of the heat equation for each region of the component. The silicon chip thermal model is based upon the one-dimensional rectangular coordinate heat diffusion equation and includes the nonlinear thermal conductivity of silicon. The package models describe the two-dimensional lateral heat spreading and the heat capacity of the periphery of the package. The heat sink models describe the heat spreading beneath the package-heat sink interface, the semicylindrical heat flow from the package toward the heat sink fins, and the nonlinear forced and natural convection heat transfer at the heat sink fins.

The three-dimensional heat diffusion equation for isotropic materials (thermal conductivity is independent of direction) can be written as:

$$\nabla \cdot (k(T)\nabla T) = \rho c \frac{\partial T}{\partial t} \tag{1a}$$

where the thermal conductivity for silicon is nonlinear and is given by [10]:

$$k(T) = 1.5486 \cdot (300/T)^{4/3}. \tag{1b}$$

The symbols used throughout the text are defined in the nomenclature section. For various symmetry conditions, this partial differential equation can be discretized into a finite number of first-order ordinary time-dependent differential equations of the form

$$\frac{T_{i+1} - T_i}{R_{i,i+1}} - \frac{T_i - T_{i-1}}{R_{i-1,i}} = \frac{dH_i}{dt} \tag{2a}$$

where

$$H_i = C_i \cdot T_i \tag{2b}$$

is the heat energy stored at thermal node i. The heat equation and the discretization coefficients ($R_{i,i+1}$, and C_i) are given in Table I for the rectangular coordinate system with y- and x-axis symmetry, Table II for the cylindrical coordinate system with z- and θ-symmetry, and Table III for the spherical coordinate system with θ- and ϕ-symmetry. The discretization coefficients are obtained by integrating the heat diffusion equations across the thermal element represented by each node (e.g., between $(z_{i-1} + z_i)/2$ and $(z_i + z_{i+1})/2$ for

node i in rectangular coordinates), and by then applying finite differences to evaluate the spatial derivatives.

In the discretization process of (2), it is assumed that the temperature gradient and thermal conductivity do not vary substantially between adjacent grid points. Therefore, the accuracy of the thermal component model is determined by the number and locations of the thermal nodes within the component. For high power dissipation levels during short periods of time (e.g., for switching transients), the silicon chip surface temperature rises faster than the heat diffuses into the chip (nonquasistatic heating), and a high density of thermal nodes is required at the silicon chip surface. However, the thermal gradients disperse as the heat diffuses through the chip, so a grid spacing that increases logarithmically with distance from the heat source (silicon chip surface) results in the minimum number of thermal nodes required to describe the temperature distribution for the range of applicable power dissipation levels (heating rates).

C. Saber Simulator Implementation

In the Saber circuit simulator, the models that describe each of the components of the system (first column of Fig. 2(b)) are accessed from the Saber libraries of standard component models, or from user-defined Saber templates where the equations that describe the physical behavior of the new component types are implemented. Saber templates are written in the MAST® modeling language, which is similar to the C programming language with the addition of specially designed modeling constructs [2]. For example, Fig. 5 is an abbreviated outline of the Saber template for the silicon chip thermal model. The first statement in the template header defines the name of the model template, the names of the terminal connection points, and the names of the model parameters. The next statement defines the terminal types of the `junct`[2] and `header` to be `thermal_k` type. The `thermal_k` type terminals have units of temperature (K) across the terminals and units of power (W) flowing through the terminals. The `number` statements in the header section define the default values of the model parameters. The equations that describes the behavior of the thermal component are defined in the body of the template.

To implement thermal component models into Saber templates, the models are formulated such that the components of power flow between the thermal nodes are expressed in terms of nonlinear functions of the system variables and in terms of the time rate of change of these functions of the system variables. System variables for thermal models are the temperatures at the thermal nodes (thermal terminals and internal thermal nodes) and explicitly defined system variables that account for implicit model equations. The local declarations section of the template is used to define constants, designate internal nodes, and explicitly define the additional system variables (in addition to the node temperatures) needed to describe the state of the component. The parameters section of the template is used to calculate quantities that do not change during simulation, such as the node positions and heat

[2]The `sans serif` symbols throughout the text represent computer mnemonics.

```
# ———————— Template Header ————————
template chip_therm junct header = a_chip, thick, list,
                                   zoffset, wp, lambda
thermal_k  junct, header          # thermal type terminals
#default model parameters
number a_chip=0.1      #(cm**2)    #area of chip
number thick=0.05      #(cm)       #thickness of chip
number list=1          #(0,1)      #parameter output flag
number zoffset=0.1     #(cm)       #depth of junct terminal
number wp=0.0          #(cm)       #heat sourced thickness
number lambda=1        #(0<,<1)    #source shape (wp/wj)

{  # ———————— Template Body ————————
   # local declarations
   parameters { # parameters calculated prior to simulation }
   values { # nonlinear function of system variables }
   equations { # equations for system variables }
}
```

Fig. 5. Abbreviated outline of Saber template for silicon chip thermal model.

capacitances. The functions of the system variables such as the nonlinear thermal conductivity of silicon for each node are implemented in the values section of the template. The equations section is then used to describe the components of power flow between the internal thermal nodes in terms of the quantities calculated in the values and parameters sections.

For example, the basic `chip_therm` model has an internal thermal node for each discretization indices i at position z_i, and the terminal nodes are at the silicon chip surface `junct` and the chip-package interface `header`. Fig. 6 shows an abbreviated form of the equation section of the `chip_therm` Saber template where only five internal nodes are indicated for simplicity (the actual model consists of a 15-node quasilogarithmically spaced grid). The first six statements of Fig. 6 describe the heat conduction between the adjacent nodes using the thermal resistances (left-hand side of 2(a)). The next five statements describe the components of power that are stored as heat energy in the thermal capacitance at each thermal node (right-hand side of 2(a)). The last four statements describe the dissipated power at each node due to the distributed heat source (described below). The equations section for the discretized heat diffusion equation has a similar form for all of the thermal component models except that each model uses a different method to calculate the discretization coefficients ($R_{i,i+1}$, and C_i) in the parameters and values sections of the template.

D. Silicon Chip Thermal Model

The silicon chip thermal model is based upon the rectangular coordinate heat diffusion equation and includes the nonlinear thermal conductivity of silicon. The chip thermal model also includes a distributed heat source option if the parameter $w_p > 0$, where the power dissipation density as a function

```
equations {
        p(junct -> node1)       +=      (Tj-T1)/Rj1
        p(node1 -> node2)       +=      (T1-T2)/R12
        p(node2 -> node3)       +=      (T2-T3)/R23
        p(node3 -> node4)       +=      (T3-T4)/R34
        p(node4 -> node5)       +=      (T4-T5)/R45
        p(node5 -> header)      +=      (T5-Th)/R5h

        p(node1)                +=      d_by_dt(H1)
        p(node2)                +=      d_by_dt(H2)
        p(node3)                +=      d_by_dt(H3)
        p(node4)                +=      d_by_dt(H4)
        p(node5)                +=      d_by_dt(H5)

        p(junct -> node2)       +=      Pd2
        p(junct -> node3)       +=      Pd3
        p(junct -> node4)       +=      Pd4
        p(junct -> node5)       +=      Pd5
        }
```

Fig. 6. Abbreviated outline of the equations section of the Saber template for the basic silicon chip thermal model.

of depth into the chip z is given by

$$\mathcal{P}(z,t) = \begin{cases} P_T(t) \cdot \frac{1-\lambda z/w_p}{1-\lambda/2} & \text{for } z \le w_p \\ 0 & \text{for } z > w_p. \end{cases} \tag{3}$$

The heat source of (3) is triangular if the model parameter $\lambda = 1$ corresponding to a depletion region that extends from the surface into the chip, or trapezoidal if $0 < \lambda < 1$ corresponding to a depletion region that is terminated by a high doped layer at w_p. For $\lambda = 0$, the power density is constant between 0 and w_p. Based upon (3) and the model parameters in the parameter list, the silicon chip thermal model calculates the fraction of heat source power that is dissipated in each thermal element within the heat source f_i (i.e., fraction of power dissipated between $(z_{i-1} + z_i)/2$ and $(z_i + z_{i+1})/2$). The heat source power into each node during simulation is then calculated using $P_{\mathrm{di}} = P_{d1} \cdot f_i/f_1$, where the power from the heat source into node 1 is given by $P_{d1} = (T_j - T_1)/R_{j1}$.

A logarithmically spaced grid is used by the chip thermal model to minimize the number of nodes required to accurately represent the dynamic temperature distribution for the full range of applicable power dissipation levels. To aid in the visualization of the transient temperature distribution, a quasilogarithmically spaced grid is used that consists of an evenly spaced grid within segments where the segment size increases logarithmically with distance from the heat source. For improved modularity, the quasilogarithmic grid spacing of the chip thermal model is implemented using a hierarchical approach. Fig. 7 is an abbreviated outline of the 15 node, quasilogarithmically spaced grid, chip thermal model (`chip_th_15log`). The parameters section of the template calculates the thickness of each segment and the z-axis offset from the silicon chip surface to the top of each segment.

```
# ———————— Template Header ————————
template chip_th_15log junct header = a_chip, thick, list
{ #Template Body
parameters {
        thick3 = 4/5 * thick
        thick2 = 4/5 * (thick-thick3)
        thick1 = thick - thick2 - thick3

        zoffset1 = 0
        zoffset2 = thick1
        zoffset3 = thick1 + thick2
         }
  chip_th5.top    junct    level1    =a_chip,thick1,list,zoffset1
  chip_th5.mid    level1   level2    =a_chip,thick2,list,zoffset2
  chip_th5.bot    level2   header    =a_chip,thick3,list,zoffset3
}
```

Fig. 7. Abbreviated outline of Saber template for 15-node, quasilogarithmically spaced grid, silicon chip thermal model.

Each segment is then implemented by netlisting an instance of the five-node, evenly spaced grid, subchip thermal model (`chip_th5`). The offset parameter is used so that the output list of node positions for each segment is specified relative to the location of the chip surface.

Using the values of the model parameters specified in the netlist, the silicon chip thermal model calculates the positions of the internal nodes z_i to form the logarithmic grid spacing. The node positions, the chip area, and the instantaneous node temperatures are used to evaluate the model functions $R_{i,i+1}$, H_i, and P_{di} that are used by the equations section (Fig. 6). The node positions, heat capacitances, and fraction of power dissipated within each element are calculated in the parameters section of the Saber template prior to simulation time because they do not depend on simulator system variables. These calculated parameters can be listed when the templates are loaded by setting the parameter `list` > 0. The thermal conductivities, thermal resistances, heat energies, and the dissipated heat source power for each node are calculated in the values section because they depend upon the instantaneous temperatures of the thermal nodes, which are simulator system variables. Because the expression for the thermal conductivity of silicon in (1b) is not defined for $T \le 0$ K, the calculations of thermal conductivity must be bounded to prevent numerical computation errors.

E. Package Thermal Model

The discretized heat equation of the package thermal model is formulated similarly to the silicon chip thermal model except that the expressions used to calculate the thermal resistances, thermal capacitances, and the heat energies are different. The package model describes the two-dimensional lateral heat spreading, the die attachment thermal resistance, and the heat capacity of the package periphery. In accordance with the logarithmic grid spacing principle, the package model includes five thermal nodes in the heat conduction path from the package header toward the package case. The package

TABLE I
RECTANGULAR COORDINATE y- AND x-AXIS SYMMETRY

$$A\frac{\partial}{\partial z}\left(k(T)\frac{\partial T}{\partial z}\right) = A\rho c\frac{\partial T}{\partial t} \quad (T1.1)$$

$$C_i = A\rho c \cdot (z_{i+1} - z_{i-1})/2 \quad (T1.2)$$

$$R_{i,i+1} = (z_{i+1} - z_i)/A/k_{i,i+1} \quad (T1.3)$$

TABLE II
CYLINDRICAL COORDINATE z- AND θ-SYMMETRY

$$A\frac{1}{r}\frac{\partial}{\partial r}\left(k(T)r\frac{\partial T}{\partial r}\right) = A\rho c\frac{\partial T}{\partial t} \quad (T2.1)$$

$$A = 2\pi r\gamma z \quad (T2.2)$$

$$C_i = \pi\gamma z\rho c\left[\left(\frac{r_{i+1}+r_i}{2}\right)^2 - \left(\frac{r_i+r_{i-1}}{2}\right)^2\right] \quad (T2.3)$$

$$R_{i,i+1} = \frac{1}{2\pi\gamma z k_{i,i+1}}\ln\left(\frac{r_{i+1}}{r_i}\right) \quad (T2.4)$$

TABLE III
SPHERICAL COORDINATE θ- AND ϕ-SYMMETRY

$$A\frac{1}{r^2}\frac{\partial}{\partial r}\left(k(T)r^2\frac{\partial T}{\partial r}\right) = A\rho c\frac{\partial T}{\partial t} \quad (T3.1)$$

$$A = 4\pi r^2\gamma \quad (T3.2)$$

$$C_i = \frac{4}{3}\pi\gamma\rho c\left[\left(\frac{r_{i+1}+r_i}{2}\right)^3 - \left(\frac{r_i+r_{i-1}}{2}\right)^3\right] \quad (T3.3)$$

$$R_{i,i+1} = \frac{1}{4\pi\gamma k_{i,i+1}}\left(\frac{1}{r_i} - \frac{1}{r_{i+1}}\right) \quad (T3.4)$$

periphery is modeled as an additional thermal node that is not in the direct heat conduction path and accounts for the remainder of the heat capacitance outside of the main heat conduction path. The parameters for the generic package thermal model include the chip area, the location of the chip on the package header, the width of the header, the length of the header, and the thickness of the header. Based upon these parameters, the discretization coefficients are calculated in the parameters section of the template and can be listed when the templates are loaded by specifying `list` > 0 in the parameter list. Thus, various package component models can be generated from the generic package template by specifying structural and material parameters, and the user does not need to calculate the internal thermal resistances and thermal capacitances.

The lateral heat spreading in the package results in an effective heat flow area that increases with depth into the package. In the model, the effective heat flow area at each depth into the package is obtained by combining the components of heat flow area due to the cylindrical heat spreading along the edges of the chip, the spherical heat spreading at the corners of the chip, and the rectangular coordinate component of heat flow directly beneath the chip. For $r_{i+1} - r_i \ll r_i$, one can find from Taylor series expansions that the spherical and cylindrical components of thermal capacitance and thermal resistance are given approximately by (T1.2) and (T1.3) in Table I, where the expression for A is replaced by (T2.2) in Table II and (T3.2) in Table III, respectively. This is a resonable approximation because the heat flow area is dominated by the area of the chip for small distances into the package and the cylindrical and spherical components of heat flow area are important only for larger distance into the package where $r_{i+1} - r_i \ll r_i$ is satisfied.

Because the heat does not spread laterally beyond the edges of the package, the radius that the heat spreads beyond each edge of the chip (rxp_i, rxm_i, ryp_i, rym_i) is limited in the model for each node at depth z_i by the distance from each edge of the chip to the edges of the package (dxp, dxm, dyp, dym), e.g.,

$$\mathrm{rxp}_i = \begin{cases} z_i & \text{for } z_i \le \mathrm{dxp} \\ \mathrm{dxp} & \text{for } z_i > \mathrm{dxp}. \end{cases} \quad (4)$$

The cylindrical component of heat flow area at each node is then given by the areas of the one-quarter cylinders at each edge of the chip:

$$\mathrm{Acyl}_i = \frac{\pi}{4}W_{\mathrm{ch}}(\mathrm{rym}_i + \mathrm{ryp}_i) + \frac{\pi}{4}L_{\mathrm{ch}}(\mathrm{rxm}_i + \mathrm{rxp}_i) \quad (5)$$

where one-half of the lateral heat spreading has been assumed to be toward the package periphery and the other half toward the package case (i.e., $\gamma = 1/8$ in (T2.2)). The spherical component of heat flow area at each node is given by the areas of the one-eighth spheres at each corner of the chip:

$$\mathrm{Asph}_i = \frac{\pi}{4}(\mathrm{rym}_i + \mathrm{ryp}_i) \cdot (\mathrm{rxm}_i + \mathrm{rxp}_i) \quad (6)$$

where one-half of the heat spreading has been assumed to be toward the package case (i.e., $\gamma = 1/16$ in (T3.2)). The value of the effective heat flow area used to calculate the thermal resistance and capacitance at each node is then given by $\mathrm{Aeff}_i = \mathrm{Acyl}_i + \mathrm{Asph}_i + \mathrm{Achip}$. The value of the effective heat flow area at the package case is also used as a parameter for the heat sink thermal model (`a_heat` of Fig. 2(b)).

F. Heat Sink Thermal Model

The heat sink thermal model includes a discretized heat equation similar to the chip and package thermal models where the discretization coefficients are determined by the structural and material parameters of the heat sink as well as the value of `a_heat` determined by the package models. The heat sink model describes the lateral heat spreading directly beneath the package-heat sink interface, the semicylindrical heat diffusion from the area beneath the package toward the heat sink fins, and the nonlinear forced and natural convection heat transfer from the heat sink fins to the ambient terminal. The parameters

for the generic heat sink template include the package heat source area, the thickness of the heat sink base, the location of the package on the heat sink, the mass of the heat sink, the fin area, the fin height, and the air velocity for forced convection.

In the vicinity of the heat source (location of package), the heat diffuses vertically toward the back of the heat sink base and also spreads laterally, as described for the package models. After the heat has diffused to the back of the heat sink base beneath the heat source, the heat flow becomes cylindrical as the heat continues to diffuse laterally beyond the location of the heat source. In accordance with the logarithmic grid spacing principle, one thermal node is required to describe the vertical heat flow through the base region, and the radii of the cylindrical grid points surrounding the heat source are given as multiples of the radius of the heat source at the center of the base region (determined using `a_heat`). The cylindrical heat flow symmetry continues until the radius of the thermal nodes reach the edge of the heat sink base or one-half the distance to another heat source. For a single heat source, the heat flow symmetry then becomes semicylindrical with $\gamma = 0.5$ for the remainder of the heat capacitance determined from the heat sink mass parameter. For multiple heat sources, the semicylindrical symmetry is broken when the radius of the thermal nodes reaches one-half of the distance between the heat sources, and the remainder of the heat sink base must be represented using a rectangular grid.

At the heat sink fins, the heat is transferred to the ambient terminal by forced and natural convection. The natural convection thermal resistance is given by [8]

$$h'_{\text{nat}} = 4.84 \times 10^{-4} \frac{A_{\text{fin}}}{P_{\text{fin}}^{0.35}} \tag{7a}$$

$$R_{\text{nat}} = \frac{1}{h'_{\text{nat}} \cdot (T_f - T_a)^{0.35}} \tag{7b}$$

and the forced convection thermal resistance is given by

$$f = \begin{cases} 1.7 + 0.148 \cdot \ln(v_{\text{air}}/508) & \text{for } v_{\text{air}} \le 508 \text{ cm/s} \\ 1.7 + 0.433 \cdot \ln(v_{\text{air}}/508) & \text{for } v_{\text{air}} > 508 \text{ cm/s}, \end{cases} \tag{8a}$$

$$h'_{\text{for}} = f \cdot 4.88 \times 10^{-4} \frac{A_{\text{fin}}}{\sqrt{Z_{\text{fin}}}}, \tag{8b}$$

$$R_{\text{for}} = \frac{1}{h'_{\text{for}} \cdot \sqrt{v_{\text{air}}}} \tag{8c}$$

where the fin-to-ambient thermal resistance is the parallel combination of the forced convection thermal resistance, the natural convection thermal resistance, and the shunt chases mounting thermal resistance. Because h'_{nat} and h'_{for} do not depend upon the simulator system variables, they are calculated in the parameters section of the Saber template and can be listed when the templates are loaded.

V. Verification of Thermal Models

In this section, examples of electrothermal network simulations are given, and the results are verified by comparison with measurements and finite element simulations. The temperature waveforms are verified using several different methods: 1) infrared microradiometer measurements of chip surface temperature waveforms [11], [12], 2) thermocouple probe measurements of heat sink temperature waveforms, 3) three-dimensional transient finite element simulations of temperature [9], and 4) device temperature-sensitive electrical parameter measurements [11], [12]. Because the temperature-dependent electrical characteristics of the IGBT model used for the electrothermal simulations below have been verified in Figs. 6 and 7 of [3], the agreement between the simulated and measured electrical waveforms verifies that the thermal network component models accurately describe the dynamic chip surface temperature waveforms. This is the so-called temperature-sensitive electrical parameter method for measuring the junction temperature of semiconductor devices [11], [12].

Figs. 8 through 12 show the measured and simulated electrical waveforms and the measured and simulated temperature waveforms at selected grid positions within the thermal network for circuit conditions that result in various power dissipation levels (rate that heat is dissipated). The shape of the dynamic temperature distribution within the thermal network depends upon the power dissipation level. For high power dissipation levels during short periods of time, the temperature gradients are high near the surface of the silicon chip, but the heat does not diffuse far into the thermal network. However, for low power dissipation levels during long periods of time the temperature gradients are small, but the heat diffuses throughout the thermal network. The thermal models developed using the logarithmic grid spacing principle accurately describe the temperature distribution for the full range of applicable power dissipation levels without an excessive number of thermal nodes. Therefore, the designer does not need to be concerned with selecting a thermal grid that is suitable for a given problem.

First, consider Fig. 8, which shows a 300-V, 6-A short-circuit test for a gate drive voltage of $V_{\text{gon}} = 7$ V. Fig. 8 is for an IGBT with a base lifetime at the reference temperature of $\tau_{\text{HL}}(300 \text{ K}) = 7.1$ μs. For this short-circuit test condition, the IGBT is turned on for 100 μs with a preexisting short circuit across the load (low load inductance and load resistance). The increase in short-circuit current with time is due to the decrease in threshold voltage with temperature [3]. However, for higher currents (above 15 A), the short-circuit current decreases with time due to the decreasing transconductance. In the intermediate current range (12 A through 15 A), the current initially decreases and then increases at high temperatures. In general, the range of short-circuit currents that have positive or negative temperature coefficients varies from one device type to another and can be predicted by the electrothermal IGBT model using the model parameters and their temperature coefficients.

The circuit conditions of Fig. 8 result in an 1800-W power dissipation level for the 0.1-cm^2 area chip. For this power dissipation level, only the top 140 μm of silicon are heated during the 100-μs pulse, and only 180 mJ of dissipated energy results in a 140-K rise in chip surface temperature. It is evident from Fig. 8 that the grid spacing of 20 μm in the top 100 μm of silicon is necessary to resolve the nonquasistatic

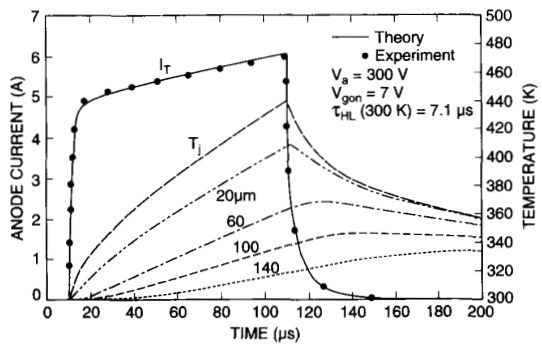


Fig. 8. Simulated and measured IGBT short-circuit current and simulated temperature waveforms at selected depths within the silicon chip.

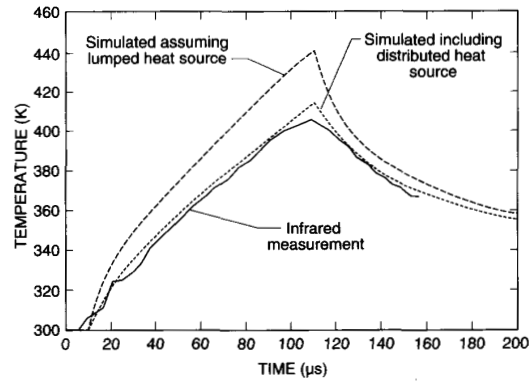


Fig. 9. Comparison of transient infrared silicon chip surface temperature measurement with simulated results for electrical conditions identical to those of Fig. 8. Simulation results are shown for a lumped heat source at the silicon chip surface and for a distributed heat source. The heat source depth of 44 μm is calculated from the depletion depth for this device at 300 V using the IGBT model parameters in [3].

temperate distribution for this high power dissipation level (only selected thermal nodes are indicated in Fig. 8). The quasilogarithmically spaced grid has a 4-μm grid spacing in the top 20 μm of the silicon chip to resolve the temperature distribution for the maximum heating rate of 10 000 W/0.1 cm^2 that occurs for 500-V avalanche sustaining at the 20 A/0.1 cm^2 device current density rating.

Fig. 9 compares the simulated and measured temperature at the surface of the chip for the same short-circuit condition as Fig. 8. Simulation results are shown for two different heat source distributions, one for a planar source located at the surface of the chip and the other for a distributed heat source with a triangular power density distribution. (The power density linearly decreases from a maximum at the chip surface to zero at a depth of 44 μm below the surface. The depletion depth of 44 μm at 300 V is calculated for this device using the IGBT model parameters in [3].) The measurement of the temperature was performed with an EDO/Barnes Computherm III infrared microscope using an optional transient thermal detection scheme. The response time of the optional transient system is expected to be 2 μs. The transient infrared system was calibrated for temperature using a chopped source to eliminate drift in the signal. The actual transient temperature measurement was done by averaging the signal over 25 pulses to reduce random noise in the signal. For the high power dissipation level of this example, the temperature waveform for the planer heat source is 20% higher than the simulations with the actual distributed heat source and the measured results, but for lower power dissipation levels the distributed heat source is less important.

Next, consider Fig. 10, which shows the approximately 10-A, 10-V, 60-Hz output characteristics of an IGBT with a base lifetime of $\tau_{\mathrm{HL}}(300\ \mathrm{K}) = 7.1\ \mu$s. The measured characteristics of Fig. 10(a) are obtained using the TEK 370 curve tracer single-family digital measurement with the 60-Hz rectified sinewave collector supply and the 0.25-Ω power limiting resistance. The device package is mounted on a water-cooled, temperature-controlled test fixture at 300 K. The simulated results of Fig. 10(b)–(d) are obtained for an electrical network that is equivalent to the TEK 370 curve tracer and the thermal network of Fig. 2*b*, but with the ambient temperature source $T_a = 300$ K connected directly to the package case T_c. The simulated output characteristics of Fig. 10(b) are obtained using the Saber PLTOOL waveform calculator to plot the simulated current waveform as a function of the voltage waveform. The positive slope of the saturation current versus anode voltage in Fig. 10(a) and (b) is due to the positive saturation region temperature coefficient [3]. The thermal looping of the saturation characteristics occurs because the chip temperature does not reach a steady-state condition.

Fig. 10(c) shows the transient anode voltage, anode current, and chip surface temperature waveforms for the 8-V and 9-V curves of Fig. 10(b). For this approximately 100-W power dissipation condition, the chip is heated evenly, but the temperature does not reach a steady-state condition, as is evident by the delay in the peak temperature with respect to the peak anode voltage waveform. Fig. 10(d) shows the temperature waveforms at equally spaced depths within the silicon chip (solid lines from 0 through 500 μm) and at selected depths within the package (dashed lines from 500 through 2500 μm). For this 100-W, 60-Hz power dissipation function, the thermal gradient is nearly constant in the silicon chip, and a grid spacing of 100 μm distributed evenly throughout the chip would be sufficient to represent the temperature distribution in the chip. However, only the first 600 μm of the package (500 μm through 1100 μm) have 60-Hz fluctuation in the temperature waveform, and only the top half of the package (500 μm through 1500 μm) is heated significantly at the end of the five-member single-family measurement.

Next, consider Fig. 11, which compares the thermal step response predicted by the thermal component models with three-dimensional finite element simulations [9] for (a) a 0.3-cm^2 area chip and (b) a 0.1-cm^2 area chip in a TO247 package, where the temperature waveforms at various depths in the chip (0 through 500 μm) and the TO247 package (500 μm through 2500 μm) are indicated. The temperature drop in the package ($T_h - 300$ K) is larger for the large chip area (Fig. 11(a)) than for the smaller chip area (Fig. 11(b)) at the same power per

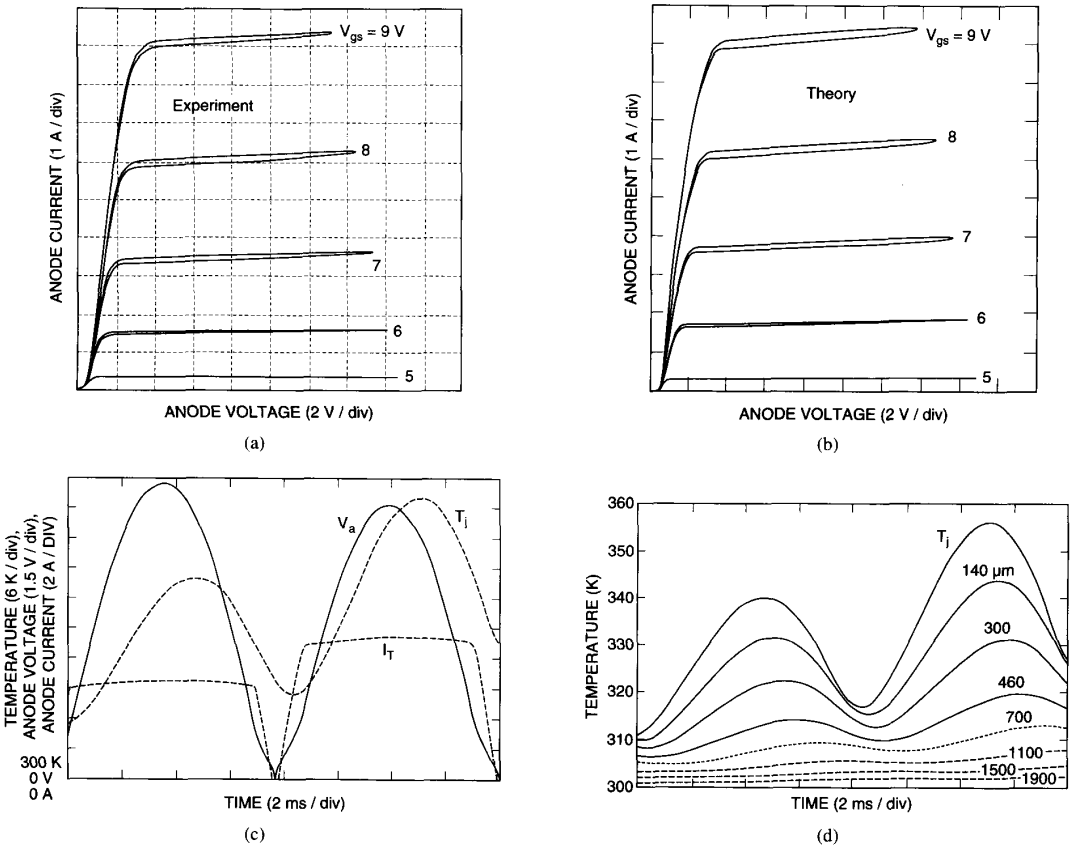


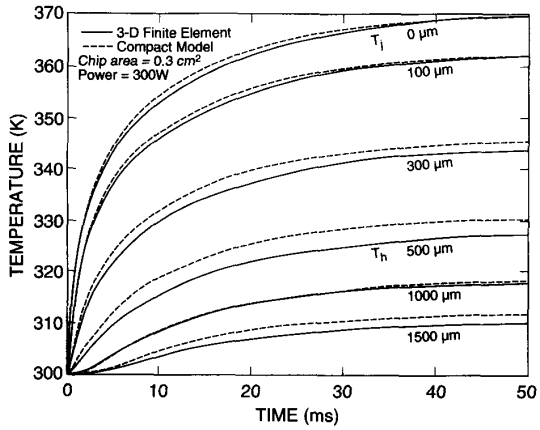
Fig. 10. Output characteristics of a $\tau_{HL}(300\ K) = 7.1\text{-}\mu s$ IGBT including self-heating. (a) Measured using a TEK 370 curve tracer,with a 60-Hz rectified sinewave collector supply. (b) Simulated for same electrical and thermal conditions. (c) Simulated curve tracer anode voltage, anode current, and chip surface temperature waveforms. (d) Simulated temperature waveforms at selected depths within the silicon chip (solid) and package (dashed).

unit area 1000 W/cm^2. This occurs because the lateral heat spreading in the package is more significant for the smaller chip and because the smaller chip is located farther from the edge of the package. The package model accounts for these effects using appropriate symmetry conditions, while the user needs only to specify the dimensions and location of the chip on the package. Although the finite element model describes the temperature distribution accurately, an excessive number of thermal nodes are required (approximately 5000) to provide accurate simulations for the full range of applicable power dissipation levels.

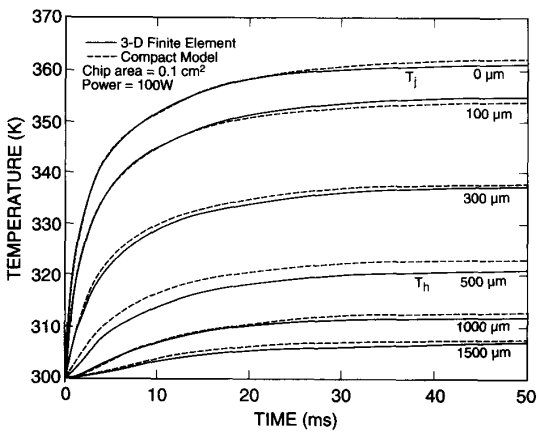
Finally, Fig. 12 shows the thermal drift of the on-state voltage for a constant gate voltage of $V_{gs} = 20$ V and a constant 10-A anode current step, where the heat sink fins are vertically oriented in a 300-K open area. The on-state voltage of the τ_{HL} (300 K) = 0.3-μs IGBT increases with time because it has a positive temperature coefficient [3]. The temperature waveforms were measured by placing thermocouple probes at various locations on the heat sink. Notice that a grid spacing of a few millimeters is adequate within the heat sink as predicted by the logarithmic grid spacing principle. For the 30-W power dissipation level, several seconds are required for the heat to diffuse to the area of the heat sink beneath the package, several tens of seconds are required for the heat to diffuse to a radius of a few centimeters beyond the heat source, and several hundred seconds are required to heat the entire thermal network to a steady-state fin temperature. Thus, for this low power dissipation level, the entire thermal network including the chip, package, and heat sink is heated, and several kJ of dissipated power are required to heat the chip surface to 100 K above the ambient. This is in contrast to the 100 mJ required for the high power short-circuit condition of Figs. 8 and 9.

VI. Conclusion

A new methodology has been developed for simulating the dynamic electrothermal behavior of electronic systems in which the simulator solves for the temperature distribution within the semiconductor devices, packages, and heat sinks (thermal network) as well as the currents and voltages within the electrical network. A procedure is presented for developing accurate, computationally efficient, and easy-to-use thermal models (compact models) to be used in the design of large electrothermal networks. The thermal component models are based upon a discretization of the heat diffusion equation



(a)



(b)

Fig. 11. Comparison of the thermal step response predicted by the thermal network component models with three-dimensional finite element simulations for (a) a 0.3-cm^2 area chip and (b) a 0.1-cm^2 area chip in a TO247 package, where the temperature waveforms at various depths in the chip (0 through 500 μm) and the TO247 package (500 μm through 2500 μm) are indicated.

for various three-dimensional coordinate system symmetry conditions and include the nonlinear thermal conductivity of silicon and nonlinear convection heat transfer. It is shown that a logarithmic grid spacing provides the high resolution needed near the heat sources for high-power dissipation levels without resulting in an excessive number of thermal nodes to describe the entire system. Electrothermal simulations will become a practical tool for the design of electronic systems when models for all of the standard thermal components are available in the network simulators used by circuit designers.

VII. Nomenclature

Achip	Silicon chip area (cm^2).
Acyl$_i$	Cylindrical component of heat flow area at node i (cm^2).
Asph$_i$	Spherical component of heat flow area at node i (cm^2).
Aeff$_i$	Effective heat flow area (cm^2).

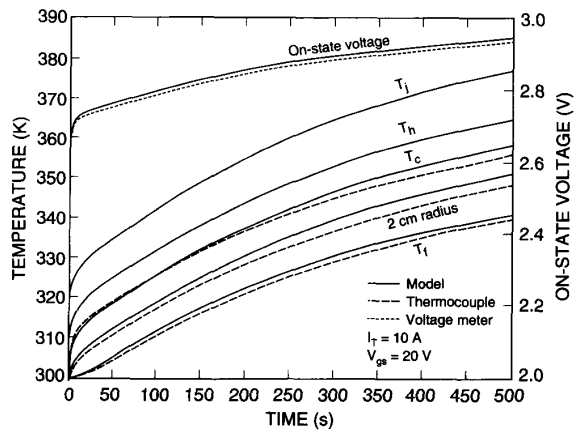


Fig. 12. Simulated and measured thermal drift of the IGBT on-state voltage where the temperature waveforms are measured using thermocouple probes at the package case (T_c), a 2-cm radius from the package within the heat sink, and at the heat sink fins (T_f). The simulated temperaturewaveforms at the silicon chip surface (T_j) and the package header (T_h) are also shown.

A_{fin}	Total heat sink fin area (cm^2).
a_heat	Effective heat flow area at the package case (cm^2).
c	Specific heat (J/cm·K).
C_i	Thermal capacitance of node i (J/K).
dxp	Positive x distance from chip edge to package edge.
dxm	Negative x distance from chip edge to package edge.
dyp	Positive y distance form chip edge to package edge.
dym	Negative y distance from chip edge to package edge.
f	Forced convection correction factor.
f_i	Fraction of power dissipated at node i.
H_i	Heat energy at node i (J).
h'_{for}	Forced convection heat transfer coefficient.
h'_{nat}	Natural convection heat transfer coefficient.
I_T	IGBT anode current (A).
i	Discretization indices.
$k(T)$	Thermal conductivity (W/cm·K).
$k_{i,i+1}$	$k(T)$ between nodes i and $i+1$ (W/cm·K).
L_{ch}	Length of chip (cm).
$P_T(t)$	Semiconductor device dissipated power (W).
$\mathcal{P}(z,t)$	Power dissipation source distribution (W/cm).
P_{fin}	Heatsink fin height, orientation parameter (cm).
P_{di}	Power dissipation at node i (cm).
R_{for}	Forced convection thermal resistance (K/W).
$R_{i,i+1}$	Thermal resistance between nodes i and $i+1$ (K/W).
R_{nat}	Natural convection thermal resistance (K/W).
rxp$_i$	Lateral heat spreading in positive x direction (cm).
rxm$_i$	Lateral heat spreading in negative x direction (cm).
ryp$_i$	Lateral heat spreading in positive y direction (cm).

rym_i	Lateral heat spreading in negative y direction (cm).
r_i	Cylindrical, spherical radius of node i (cm).
T_a	Ambient temperature (K).
T_c	Package case temperature (K).
T_f	Heat sink fin temperature (K).
T_h	Package header temperature (K).
T_i	Temperature at node i (K).
T_j	Silicon chip surface temperature (K).
V_a	Anode-cathode voltage (V).
V_{aa}	Anode supply voltage (V).
V_{gs}	Gate-source voltage (V).
V_{gon}	Gate voltage pulse amplitude (V).
v_{air}	Forced convection air velocity (cm/s).
w_p	Width of power dissipation source (cm).
W_{ch}	Width of chip (cm).
z_i	Depth of node i in chip, package (cm).
Z_{fin}	Height of heat sink fin (cm).
γ	Cylindrical, spherical angle fraction.
λ	Power dissipation source shape parameter.
τ_{HL}	IGBT high-level injection lifetime (s).
ρ	Mass density (g/cm^3).

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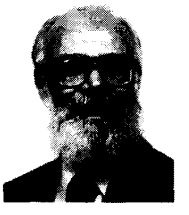
Allen R. Hefner (S'84–M'84–SM'93) was born in Washington, DC, on June 29, 1959. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Maryland, College Park, in 1983, 1985, and 1987, respectively.

He joined the Semiconductor Electronics division of the National Institute of Standards and Technology (formerly the National Bureau of Standards) in 1983. He is currently Project Leader for the Electrical and Thermal Characterization Project in the Device Technology Group of the Semiconductor Electronics Division at NIST. His research interests include characterization, modeling, and circuit utilization of power semiconductor devices.

Dr. Hefner is the author of 20 publications in IEEE TRANSACTIONS and conference proceedings. He received the U.S. Department of Commerce Silver Metal Award for his pioneering work in modeling advanced power semiconductor devices for electrothermal circuit simulation. He is also the recipient of an IEEE Industry Applications Society prize paper award. He was an instructor for IEEE Power Electronic Specialist Conference tutorial course (1991 and 1993). He has served as a program committee member for the IEEE Power Electronics Specialist Conference (1991–1994) and as the IEEE Industry Applications Society Transactions Review Chairman for the Power Semiconductor Committee (1989–1994).



David L. Blackburn (M'71–SM'87–F'93) received the B.S. degree from Ohio University, Athens, OH, in 1965 and the M.S. degree from Case Western Reserve University, Cleveland, OH, in 1968, both in physics.

Since 1968, he has been involved with research on semiconductor materials and devices at the National Institute of Standards and Technology (NIST)—formerly the National Bureau of Standards—in Gaithersburg, MD. His current research interests include the safe limit and thermal characterization of power semiconductor devices and the thermal characterization of GaAs devices and circuits. In addition to his duties at NIST, he has been an Instructor in the Electrical Engineering Department, University of Maryland, College Park. Currently, he is Group Leader for Device Technology Group in the Semiconductor Electronics Division, NIST.

Mr. Blackburn received the U.S. Department of Commerce Silver Medal Award for contributions in reducing electronic failures and increasing the reliability of electronic systems. He has been Program Chairman and General Chairman on two occasions, each for the IEEE SEMITHERM meeting.