# AN EXPERIMENTALLY VERIFIED IGBT MODEL IMPLEMENTED IN THE SABER CIRCUIT SIMULATOR *

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**Abstract** – A physics-based IGBT model is implemented into the general purpose circuit simulator Saber™. The IGBT model includes all of the physical effects that have been shown to be important for describing IGBTs, and the model is valid for general external circuit conditions. The Saber IGBT model is evaluated for the range of static and dynamic conditions in which the device is intended to be operated, and the simulations compare well with experimental results for all of the conditions studied.

### I. Introduction

The IGBT (Insulated Gate Bipolar Transistor) is a new power device that is designed to overcome the high on-state loss of the power MOSFET. The structure of the IGBT shown in Fig. 1 is similar to that of an $n$-channel VDMOSFET (Vertical double Diffused MOSFET), with the exception that the $n$-type drain contact of the conventional VDMOSFET is replaced by the $p$-type anode region for the IGBT. The purpose of the additional anode-epitaxial layer $p$-$n$ junction of the IGBT is to inject a high level of excess minority carriers into the epitaxial layer which thereby reduces the on-state resistance of this layer (conductivity modulation). Thus, IGBTs have the high output current capability of power bipolar transistors but with the efficient gate drive requirements of power MOSFETs.

IGBTs have become widely accepted among circuit designers as an alternative to power bipolar transistors and Darlington transistors in a variety of power converter and motor drive applications. To design power electronic circuits containing IGBTs, circuit simulations are needed to examine the behavior of the devices within the circuit. However, the device models currently available in most commercial circuits simulators were originally intended to describe microelectronic devices and cannot readily be modified to describe IGBTs or other power semiconductor devices.

The basic equivalent circuit of the IGBT is shown in Fig. 2, and the regions of the device structure corresponding to the elements of this circuit are indicated on the right half of Fig. 1. The $n$-channel IGBT behaves as a $p$-$n$-$p$ bipolar transistor that is supplied base current by an $n$-channel MOSFET, and thus the physical phenomena of both bipolar and MOSFET device types influence the behavior of IGBTs. However, the internal MOSFET and the internal bipolar transistor of the IGBT behave differently than their microelectronic counterparts because they have been designed for different functional purposes and have significantly different structures than the microelectronic devices.

For example, the internal VDMOSFET of the IGBT has a thick, lightly doped drain region (epitaxial layer) to support the depletion region for high blocking voltages while still maintaining a short channel length to supply high current densities. As a consequence, the gate-drain overlap capacitance of the VDMOSFET is highly nonlinear. The gate-drain capacitance is equal to the gate-drain overlap oxide capacitance for low drain voltages where the silicon beneath the gate-drain overlap is not depleted. However, at high drain voltages, the gate-drain overlap has a depletion layer in the silicon beneath the gate oxide, and the gate-drain capacitance is reduced by about two orders of magnitude.

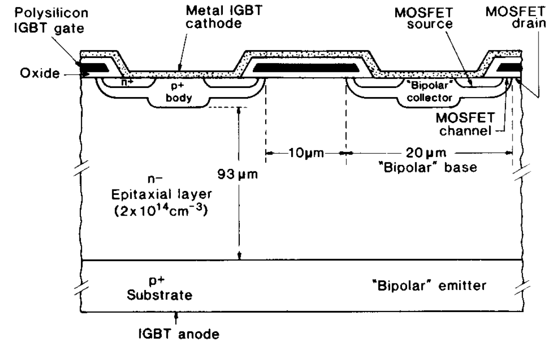


*Fig. 1. IGBT structure indicating the regions associated with equivalent circuit components of Fig. 2*

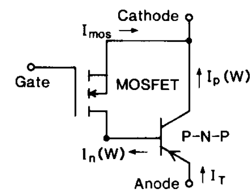


*Fig. 2. Basic IGBT equivalent circuit.*

The bipolar transistor of the IGBT is introduced for the purpose of modulating the conductivity of the epitaxial layer. This transistor has a lightly doped wide base (epitaxial layer) to support high voltages, and its base contact is at the collector edge of the neutral base where the MOSFET channel current supplies electrons to the base. This bipolar transistor is also typically designed with a low excess carrier lifetime in the base to achieve a high speed turn-off. As a consequence, the bipolar transistor of the IGBT has a low current gain and is operated in the high-level injection condition for the practical current density range of the IGBT. This is in contrast to microelectronic bipolar transistors which are designed to have a narrow base, a high base lifetime, and which are typically operated in low-level injection to achieve a high current gain.

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To describe the high-level injection operation of the wide base bipolar transistor of the IGBT and other conductivity-modulated power devices, ambipolar transport theory must be used to describe the transport of electrons and holes in the base, and the transient behavior cannot be described using the conventional quasi-static approach [1]. A physics-based model for the low-gain, high-level injection bipolar transistor of the IGBT is developed in ref. [2] and is combined with a VDMOSFET model in ref. [3], resulting in a general purpose model for the IGBT. The model has been verified for various external circuit conditions [1]-[4] and for the full range of static and dynamic conditions in which the IGBTs are intended to be operated. The model has also been shown to be suitable for simulating the behavior of IGBTs for general external circuit conditions [5],[6].

The purpose of this paper is to describe the methodology for implementing the IGBT mathematical model developed by Hefner into the Saber circuit simulator [7], and to provide a Saber IGBT model that can be used for general purpose circuit simulations. Furthermore, the techniques demonstrated for modeling IGBTs with the Saber circuit simulator are generally applicable to modeling other power semiconductor devices. Many diverse types of power devices are currently available with structures that differ significantly from one another, and different device model equations are generally required to describe each device type. This is in contrast to microelectronic devices for which many different devices can be described by using the appropriate model parameters in a few standard device models. Thus, the techniques described in this paper for implementing model equations into the Saber circuit simulator are essential for accurate simulation of power semiconductor devices.

## II. IGBT Dynamic Model

Figure 3 shows a detailed IGBT equivalent circuit superimposed on a schematic of the structure of one of the many thousand cells of an $n$-channel IGBT. The elements of the circuit of Fig. 3 represent the nonlinear physical phenomena associated with each region of the device structure. The basic IGBT equivalent circuit of a bipolar transistor that is supplied base current by a MOSFET is indicated by the MOSFET and bipolar transistor symbols within the circuit of Fig. 3. The other components connected between the emitter (e), base (b), and collector (c) nodes are associated with the bipolar transistor, and those connected between the gate (g), source (s), and drain (d) nodes are associated with the VDMOSFET.

Table 1 gives a list of the expressions used in the Saber IGBT model to describe the phenomena associated with each of the components in Fig. 3. The IGBT model equations in Table 1 are equivalent to those presented in ref. [3] with the exception that they have been augmented to show how the following effects are included [6]: 1) mobility reduction due to carrier-carrier scattering, 2) mobile carrier space charge concentration in the base-collector depletion region due to velocity saturation, and 3) avalanche multiplication within the base-collector depletion region. The equations have also been reformulated to emphasize the Saber implementation, which is described in the next section. In this section, the circuit elements of Fig. 3 are used to describe the physical origin of the expressions in Table 1 and to explain the influence of each physical phenomenon on the device behavior.

### MOSFET Characteristics

The MOSFET portion of the IGBTs studied in this work behaves similarly to the power VDMOSFET, with the exception that the resistance of the lightly doped epitaxial layer is accounted for as the conductivity-modulated base resistance of the bipolar transistor, $R_b$ [3]. In addition, the drain-source and gate-drain depletion capacitances coincide with the base-collector depletion capacitance of the bipolar transistor and hence are only included in the MOSFET model. In order to describe IGBTs made with MOSFET structures other than the VDMOSFET, only the components of Fig. 3 associated with the MOSFET portion of the device need to be changed. The first-order expression for the current through the MOSFET channel $I_{mos}$ given in Table 1 adequately describes the qualitative behavior of the IGBTs studied in this work, and can be readily modified to include the second-order effects that are important for VDMOSFETs.

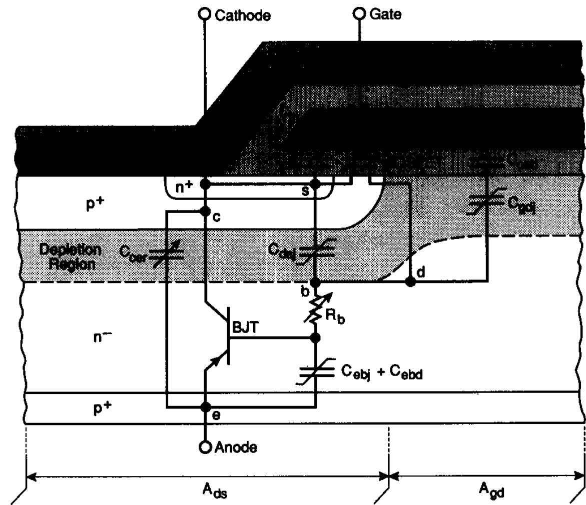



*Fig. 3. Phenomenological IGBT circuit superimposed on schematic of structure.*

The VDMOSFET gate-source capacitance $C_{gs}$ consists of the sum of the gate oxide capacitance of the source overlap $C_{oxs}$ and the source metallization capacitance $C_m$. The VDMOSFET gate-drain feedback capacitance (or Miller capacitance) $C_{gd}$ is equal to the gate oxide capacitance of the gate-drain overlap for $V_{ds} \leq V_{gs} - V_{Td}$, but for $V_{ds} > V_{gs} - V_{Td}$ the silicon beneath the gate-drain overlap becomes depleted, and the gate drain capacitance consists of the series combination of the gate-drain overlap oxide capacitance $C_{oxd}$ and the gate-drain overlap depletion capacitance $C_{gdj}$. The VDMOSFET drain-source capacitance $C_{dsj}$ consists of the depletion capacitance of the drain-body junction.

The gate-drain overlap depletion capacitance $C_{gdj}$ and the drain-source depletion capacitance $C_{dsj}$ are voltage dependent due to the voltage dependencies of the depletion widths. The drain-source depletion width $W_{dsj}$ is proportional to the square-root of the drain-source voltage plus the built-in potential of the junction ($\sim 0.6\ V$). The gate-drain depletion width $W_{gdj}$ is proportional to the square-root of the gate-drain voltage where the threshold voltage for the depletion of the epitaxial layer $V_{Td}$ is approximately equal to zero due to the low doping concentration of the epitaxial layer. The gate-drain capacitance is also proportional to the area of the gate-drain overlap $A_{gd}$, and the drain-source capacitance is proportional to the area of the body region $A_{ds}$ (Fig. 3), where the sum of $A_{gd}$ and $A_{ds}$ is the active area of the chip $A$.

### Bipolar Transistor Characteristics

The transient behavior of the lightly doped wide base bipolar transistor of the IGBT (and other conductivity-modulated

TABLE 1
FUNCTIONS OF SYSTEM VARIABLES

$V_{dg}$ =V(drain) - V(gate)
$V_{gs}$ =V(gate) - V(cathode)
$V_{ds}$ =V(drain) - V(cathode)
$V_{eb}$ =V(emitter) - V(drain)
$V_{ae}$ =V(anode) - V(emitter)
$V_{ec}$ =V(emitter) - V(cathode)
$V_{bc} = V_{ds}$

$$N_{scl} = N_B + N_{sat}$$
$$W_{gdj} = \sqrt{2\epsilon_{si}(V_{dg} + V_{Td})/qN_{scl}}$$
$$W_{dsj} = \sqrt{2\epsilon_{si}(V_{ds} + 0.6)/qN_{scl}}$$
$$W_{bcj} = \sqrt{2\epsilon_{si}(V_{bc} + 0.6)/qN_{scl}}$$
$$W = W_B - W_{bcj}$$

$$Q_{gs} = C_{gs}V_{gs}$$
$$Q_{ds} = A_{ds}\sqrt{2\epsilon_{si}(V_{ds} + 0.6)qN_{scl}}$$
$$Q_B = qAWN_{scl}$$
$$Q_{bi} = A\sqrt{2\epsilon_{si}qN_B 0.6}$$

$$C_{bcj} \equiv A\epsilon_{si}/W_{bcj}$$
$$C_{cer} = QC_{bcj}/3Q_B$$
$$C_{dsj} = (A - A_{gd})\epsilon_{si}/W_{dsj}$$
$$C_{gdj} = A_{gd}\epsilon_{si}/W_{gdj}$$
$$C_{gd} = \begin{cases} C_{oxd} & \text{for} \quad V_{ds} \le V_{gs} - V_{Td} \\ C_{oxd}C_{gdj}/(C_{oxd} + C_{gdj}) & \text{for} \quad V_{ds} > V_{gs} - V_{Td} \end{cases}$$

$$\mu_{nc} = 1/(1/\mu_n + 1/\mu_c)$$
$$\mu_{pc} = 1/(1/\mu_p + 1/\mu_c)$$
$$\mu_{eff} = \mu_{nc} + \mu_{pc}Q/(Q + Q_B)$$
$$D_c = 2(kT/q)\mu_{nc}\mu_{pc}/[\mu_{nc} + \mu_{pc}]$$
$$L = \sqrt{D_c\tau_{HL}}$$

$$P_0 = Q/(qAL \tanh \tfrac{W}{2L})$$
$$\overline{\delta p} \equiv P_0 \sinh(W/2L)/\sinh(W/L)$$
$$n_{eff} \equiv \frac{\frac{W}{2L}\sqrt{N_B^2 + P_0^2\operatorname{csch}^2(\frac{W}{L})}}{\operatorname{arctanh}\left[\frac{\sqrt{N_B^2 + P_0^2\operatorname{csch}^2(\frac{W}{L})}\tanh(\frac{W}{2L})}{N_B + P_0\operatorname{csch}(\frac{W}{L})\tanh(\frac{W}{2L})}\right]}$$

$$R_b = \begin{cases} W/(q\mu_{nc}AN_B) & \text{for} \quad Q < 0 \\ W/(q\mu_{eff}An_{eff}) & \text{for} \quad Q \ge 0 \end{cases}$$

$$V_{ebj} = 0.6 - (Q - Q_{bi})^2/(2qN_B\epsilon_{si}A^2)$$
$$V_{ebd} = \frac{kT}{q}\ln\left[\left(\frac{P_0}{n_i^2} + \frac{1}{N_B}\right)\left(N_B + P_0\right)\right] - \frac{D_c}{\mu_{nc}}\ln\frac{P_0 + N_B}{N_B}$$
$$V_{ebq} = \begin{cases} V_{ebj} & \text{for} \quad Q < 0 \\ \min(V_{ebj}, V_{ebd}) & \text{for} \quad Q_{bi} > Q \ge 0 \\ V_{ebd} & \text{for} \quad Q \ge Q_{bi} \end{cases}$$

$$BV_{cbo} = BV_f \cdot 5.34 \times 10^{13} \cdot N_{scl}^{-0.75}$$
$$M = 1/[1 - (V_{cb}/BV_{cbo})^{BV_n}]$$
$$I_T = V_{ae}/R_b$$
$$I_{css} = \left(\frac{1}{1+b}\right)I_T + \left(\frac{b}{1+b}\right)\frac{4D_p}{W^2}Q$$
$$I_c = I_{css} + C_{cer} \cdot \mathrm{d}V_{ec}/\mathrm{d}t$$
$$I_{bss} = \frac{Q}{\tau_{HL}} + \frac{Q^2}{Q_B^2} \cdot \frac{4N_{scl}^2}{n_i^2}I_{sne}$$
$$I_{mos} \approx \begin{cases} 0 & \text{for} \quad V_{gs} < V_T \\ K_p(V_{gs} - V_T)V_{ds} - K_p\frac{V_{ds}^2}{2} & \text{for} \quad V_{ds} \le V_{gs} - V_T \\ K_p(V_{gs} - V_T)^2/2 & \text{for} \quad V_{ds} > V_{gs} - V_T \end{cases}$$
$$I_{gen} = qn_iA\sqrt{2\epsilon_{si}V_{bc}/qN_{scl}}/\tau_{HL}$$
$$I_{mult} = (M - 1) \cdot (I_{mos} + I_c) + M \cdot I_{gen}$$

devices) was analyzed in reference [2]. In that analysis, the ambipolar transport equations were solved for the boundary conditions of the bipolar transistor to obtain the transient carrier distribution, the collector and base currents, and the emitter-base voltage. Figure 4 shows the coordinate system used to develop the IGBT bipolar transistor model. Because the base-collector voltage changes with time during transient conditions, the base-collector depletion width $W_{bcj}$ changes with time, and the excess carrier charge stored in the base is swept into a neutral base width $W$ that changes with time. The quasi-static condition cannot be assumed for the transient analysis because the base width typically changes faster than the base transit speed for excess carriers, and because the transports of electrons and holes are coupled for ambipolar transport [1].

In addition to the above-mentioned depletion capacitances, the bipolar transistor of the IGBT contributes a collector-emitter redistribution capacitance $C_{cer}$ which is a result of the non-quasi-static behavior of the bipolar transistor base charge for the moving base-collector boundary condition. The expression for the collector-emitter redistribution capacitance in Table 1 is equal to the ratio $Q/Q_B$ times one-third the base-collector depletion capacitance $C_{bcj}$. In the IGBT model, the base-collector depletion capacitance is defined to relate the time rate-of-change of the base-collector depletion width to the time rate-of-change of base-collector voltage, but is not used to describe the base-collector depletion capacitance displacement current which is accounted for in the gate-drain and drain-source capacitances of the VDMOSFET.

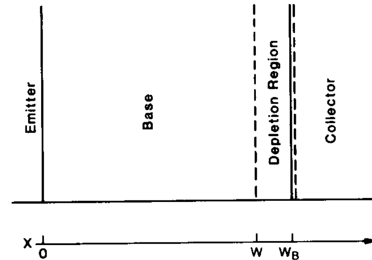



*Fig. 4. Coordinate system used to develop IGBT bipolar transistor model.*

Because the excess carrier base charge $Q$ is much larger than the background base charge $Q_B$ for the high-level injection condition, the redistribution capacitance is much larger than the depletion capacitances and thus dominates the output capacitance of the IGBT at turn-off [1]-[4]. Because the redistribution capacitance is a result of a component of collector current, this capacitance appears as an anode-to-cathode capacitance, and the gate-to-drain feedback capacitance is unchanged from that of the VDMOSFET [3]. The effective output capacitance at turn-off for the IGBT depends upon the device base lifetime, because the steady-state value of $Q$ at the initiation of turn-off depends upon the device base lifetime. The effective output capacitance at turn-on is much less than that at turn-off for the IGBT, because $Q$ is zero in the off-state before the initiation of the turn-on.

The bipolar transistor symbol in Fig. 3 corresponds to the expressions for the component of collector current $I_{css}$ and the component of base current $I_{bss}$. The expression for $I_{css}$ in Table 1 consists of the non-quasi-static component due to the coupling between the transports of electrons and holes in the base [1] (first term on the right-hand side), and the well-known charge-control component due to the diffusion of holes through the base for the high-level injection conditions (second term). The expression for $I_{bss}$ consists of a component due to recombination in the base (first term) and a component due to injection of electrons into the emitter (second term). The base current is a significant component of the total anode current for the low-gain condition of the bipolar transistor of the IGBT, and is also important in determining the time rate-of-change of base charge for transient conditions, i.e., current in the emitter-base capacitor.

The emitter-base voltage consists of the potential across the conductivity-modulated base resistance $R_b$, plus the potential across the emitter-base diffusion capacitance $C_{ebd}$ or the depletion capacitance $C_{ebj}$ [3]. For forward conduction, the emitter-base voltage is determined by the diffusion capacitance and the conductivity-modulated base resistance. The emitter-base diffusion capacitance is represented implicitly in Table 1, because the expression for the emitter-base capacitor voltage $V_{ebq}$ in terms of the base charge $Q$ cannot be inverted to obtain an expression for the charge in terms of voltage. The emitter-base junction depletion capacitance $C_{ebj}$ is important when the emitter-base junction is reverse biased or has a small forward bias, but for larger forward biases the emitter-base diffusion capacitance $C_{ebd}$ is dominant. The charge $Q$ is also used to describe the space charge of the emitter-base depletion capacitance for the bias range where this capacitance is dominant, and a continuous transition between the depletion and diffusion capacitances is obtained by using the larger of the two capacitances or equivalently the minimum voltage. For reverse blocking $Q < 0$, the collector and base currents are also replaced by the emitter-base leakage current and the reverse collector current.

Second-Order Effects

The second-order effects that are incorporated into the IGBT model but are not described on the phenomenological circuit of Fig. 3 are: 1) mobility reduction due to high free-carrier levels, 2) velocity saturation in the base-collector depletion region, and 3) carrier multiplication within the base-collector depletion region [3]-[6]. These effects do not change the qualitative behavior of IGBTs operated within their maximum current and voltage ratings, but do have a second-order effect on the quantitative results of the model. However, the carrier multiplication effect results in avalanche breakdown for operating conditions in which the maximum rated voltage is exceeded. The mobility reduction and velocity saturation effects are a result of the bias dependance of the physical parameters which are used to derive the model. These two effects are included implicitly because an explicit analytical solution is not readily obtained if these effects are included in the derivation of the basic model.

The space charge concentration due to mobile carriers flowing through the base-collector depletion region at the saturation limited velocity has a second-order effect on the time rate-of-change of the base-collector voltage [2]. The component of base-collector space charge due to velocity saturation is given in terms of $I_c$ and $I_{mos}$ by:

$$N_{sat} = I_c/(qAv_{psat}) - I_{mos}/(qAv_{nsat}). \qquad (1)$$

Because the expressions for the currents $I_c$ and $I_{mos}$ in Table 1 depend upon the space charge concentration, the variable $N_{sat}$ is solved for iteratively to satisfy eq 1. The mobility reduction due to carrier-carrier scattering has a second-order effect on the on-state emitter-base voltage at high free-carrier levels [2]. The reciprocal component of mobility due to carrier-carrier scattering is given in terms of the excess carrier concentration by:

$$1/\mu_c = \left[\, \overline{\delta p}\ \ln(1 + \alpha_2\ (\overline{\delta p})^{-2/3}) \right] / \alpha_1. \qquad (2)$$

Because the expression for the average excess carrier concentration $\overline{\delta p}$ given in Table 1 depends upon the mobility, the variable $1/\mu_c$ is solved for iteratively to satisfy eq 2. This technique can also be used to include the influence of other bias-dependent model parameters which cannot readily be included in the derivation of the analytical model, i.e., lifetime reduction due to Auger recombination [8].

Carrier multiplication due to impact ionization in the high electric field of the base-collector depletion region has a second-order effect on the anode current for large anode voltages that are within the device maximum voltage rating. Carrier multiplication also determines the avalanche breakdown behavior for operating conditions in which the device maximum voltage rating is exceeded. Carrier multiplication in the base-collector depletion region results in an additional component of base-to-collector current that increases exponentially with anode voltage near the open-base, collector-emitter breakdown voltage. The carrier multiplication current is included in the derivation of the IGBT model equations by including the additional components of base-to-collector current $I_{mult}$ that is proportional to the electron and hole currents entering the depletion region, $I_c$ and $I_{mos}$, and that is proportional to the multiplication factor $(M-1)$ [3]. The thermally generated leakage current $I_{gen}$ is also included, but this component of current is only important when using the model to describe the structurally equivalent power MOSFET.

## III. Implementing the IGBT Model Into Saber

To describe the behavior of a system such as an electrical network using the Saber circuit simulator, the interconnections of the different components of the system are described using a network listing (net-list). The net-list contains a statement for each component of the system that defines the name of the model template used to describe the component, the terminal connection points of the component, and the values of the model parameters that are to be changed from the default values of the generic model template (see section IV). The models that describe each of the components of the system can be accessed from the Saber libraries of standard component models, or from user-defined Saber templates where the equations that describe

the physical behavior of the device are implemented. The implementation of the IGBT model equations into a Saber template is described in this section, and the net-lists describing the operation of the IGBT within various test circuits are given in the next section.

Saber Templates

Saber templates are written in the MAST® modeling language which is similar to the C programming language with the addition of specially designed modeling constructs which facilitate the implementation of Kirchhoff's laws and aid convergence. Both user-defined models and the standard Saber library models are implemented in Saber templates using the MAST modeling language. Electrical component models are implemented into templates by expressing the current through each element of the component in terms of the system variables of the component; system variables for electrical component models consist of terminal node voltages, internal node voltages, and explicitly defined system variables. The simulator solves for the system variables of the entire network such that the net current into each node of the system sums to zero (i.e., Kirchhoff's current law is satisfied), and such that the equations defining the explicitly defined system variables for each component are satisfied.

A skeleton template of the Saber IGBT model is shown in Fig. 5 [7] where each section performs the following functions: In this example, the IGBT template header defines the anode, gate, and cathode† terminal connection points as well as the names and default values for model parameters such as the high level lifetime $\tau_{HL}$. The local declarations define constants, designate internal nodes, and explicitly define the additional system variables (in addition to the node voltages) needed to describe the state of the device. The parameters section is used to calculate quantities that only need to be calculated once at the beginning of the simulation. Quantities that are functions of the system variables (i.e., Table 1) are implemented in the values section. The control section contains information about the nonlinear model relationships and commands to aid convergence. Finally, the equations section describes how the quantities calculated in the values section are assembled to solve for the system variables.

IGBT Model Formulation

To implement the IGBT model presented in Section II into the Saber circuit simulator, the model is formulated such that the currents between each of the terminal nodes are expressed in terms of the nonlinear functions of the system variables (Table 1) and in terms of the time rate-of-change of these functions of the system variables. Figure 6 is a schematic of the components of current flow between the terminal nodes of the IGBT (gate, anode, and cathode), indicating the internal nodes (drain and emitter) that are required to implement the IGBT model equations given in Table 1 into the Saber circuit simulator. Figure 6 represent an analog circuit for the equations in Table 1. The expressions in Table 1 are implemented in the values section of the Saber template, and these values are used in the equations section of the template to describe the interconnection of the components of current through each element of Fig. 6.

The analog circuit representation of the IGBT model equations of Fig. 6 differs from the phenomenological circuit of Fig. 3 where the bipolar transistor symbol is replaced by the base and collector current sources. In the phenomenological circuit, the emitter-base diffusion capacitance is represented as a lumped capacitor located at the metallurgical emitter-base junction, and only the flow of base current through the conductivity modulated base resistance is indicated. However, the potential drops due to drift and diffusion are actually distributed throughout the base region, and the drift terms of the ambipolar transport equations are coupled [2]. Thus, both the base and collector components of current contribute to the resistive potential drop $V_{ae}$ in the circuit of Fig. 6.

The emitter-base capacitor current $I_{ceb}$ represents the time rate-of-change of the base charge, where the nonlinear expression given in Table 1 for the emitter-base voltage in terms of the base charge describes implicitly the capacitance of the emitter-base junction. The collector-emitter redistribution capacitance

† The "sans serif" symbols throughout the text represent computer mnemonics.

```
Template  IGBT  anode, gate, cathode  =tau_hl
electrical  anode,gate,cathode  # node type
number  tau_hl =1.0u            # default lifetime
{
# local declarations
parameters {
    # parameters calculated prior to simulation
    }
values {
    #values calculated as a function of system variables
    }
control {
    # simulator dependent control statements
    }
equations {
    # equations for system variables
    }
}
```

*Fig. 5. Skeleton template of Saber IGBT model.*

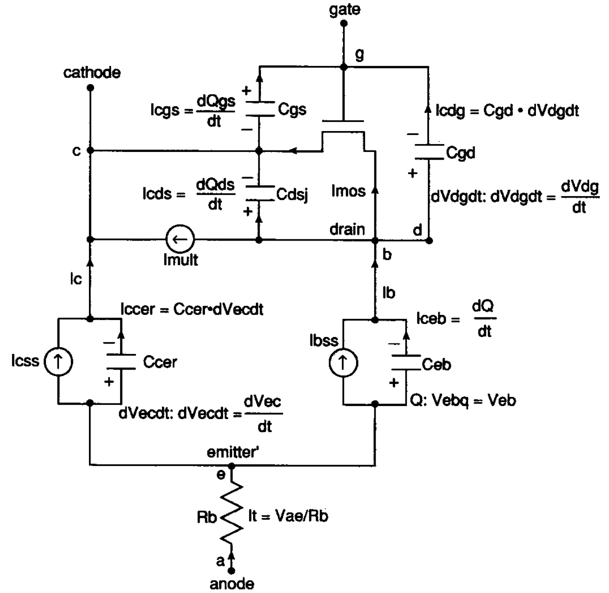



*Fig. 6. Analog circuit representation of IGBT model equations.*

represents the component of collector current that depends upon the time rate-of-change of the base-collector voltage $I_{ccer}$ (represented as the emitter-collector voltage for easier conceptualization). $I_{css}$ represents the component of collector current that does not depend upon the time rate-of-change of the base-collector voltage. $I_{bss}$ represents the component of base current that does not depend upon the time rate-of-change of the base charge and does not flow through the emitter-base capacitor. The avalanche multiplication current $I_{mult}$ flows from the base to the collector and provides an additional component of base current to the bipolar transistor.

Saber Implementation

The expressions in Table 1 are implemented in the values section of the Saber IGBT model template and are functions of the IGBT system variables, the IGBT model parameters (Table 2), and the physical constants of silicon (Table 3). The system variables for the IGBT are the node voltages and the explicitly defined system variables: $Q$, $N_{sat}$, $1/\mu_c$, $dV_{ce}/dt$, and $dV_{dg}/dt$. The first six equations in Table 1 evaluate the voltage differences used by other expressions in Table 1, where the notation V(a) is the MAST syntax for the voltage at node a. The quantities evaluated in the values section (Table 1) are used in the equations section shown in Fig. 7 to describe the currents through each of the elements of Fig. 6, and to describe the expressions that define the explicitly defined system variables; Q, Nsat, mucinv, dVecdt, and dVdgdt.

The first six statements in the equations section of Fig. 7 describe the currents between the node pairs of Fig. 6 in terms of the system variables using the values in Table 1. The notation i(a − > b) indicates that a component of current, given by the expression on the right-hand side of +=, flows from node a to node b. The currents through the gate-source and drain-source capacitances, $I_{cgs}$ and $I_{cds}$, are formulated as the time derivative of the capacitor chargers $Q_{gs}$ and $Q_{ds}$, where d_by_dt is the Saber time derivative operator, whereas the current through the gate-drain capacitance $I_{cdg}$ and the current through the collector-emitter redistribution capacitance $I_{ccer}$ are expressed as the capacitance times the system variables that represent the time derivatives of the capacitor voltages. The additional system variables are necessary because the Saber time derivative operator cannot be multiplied by a function of system variables.

The last five statements in the equations section give the expressions that must be satisfied to determine each of the explicitly defined system variables. The notation of these statements indicates that the system variable on the left-hand side of the colon (:) is to be solved for by the simulator such that the expression on the right-hand side of the colon (:) is satisfied. That is, in addition to iterating the node voltages until Kirchhoff's current law is satisfied at each node, the simulator also iterates the explicitly defined system variables until each of the expressions on the right-hand sides of the colons are satisfied. System variables are introduced in this manner to describe components of current that cannot be expressed as explicit functions of the node voltages and the time rate-of-change of the functions of the node voltages. System variables are also introduced to describe the time derivatives of capacitor voltages where the capacitance formula cannot be integrated to obtain an expression for the capacitor charge and hence the nonlinearities cannot be included within the argument of the Saber time derivative operator.

In the IGBT template, the system variable dVecdt is introduced to describe the current through the collector-emitter redistribution capacitance because this capacitance depends upon several system variables, and the current cannot be described as the time rate-of-change of a capacitor charge. The variable dVdgdt is introduced so that general expressions for the gate-drain capacitance can be readily implemented without the need to integrate the capacitance formulas to obtain the capacitor charge expression. The variable Q is introduced to describe the implicit emitter-base capacitor; that is, the expression for the voltage as a function of charge cannot be inverted. The variables Nsat and mucinv are introduced to account for the implicit relationships for these bias-dependent model parameters, eq 1 and eq 2. Thus, these variables are solved for such that eq 1 and eq 2 as well as the expressions in Table 1 are satisfied.

TABLE 2
Device Model Parameters

| | |
|---|---|
| $N_B$ | $2 \times 10^{14}\ cm^{-3}$ |
| $A$ | $0.1\ cm^2$ |
| $W_B$ | $93\ \mu m$ |
| $I_{sne}$ | $6.0 \times 10^{-14}\ A$ |
| $K_p$ | $0.36\ A/V^2$ |
| $V_T$ | $5.0\ V$ |
| $A_{gd}$ | $0.05\ cm^2$ |
| $C_{oxd}$ | $1.6\ nF$ |
| $C_{gs}$ | $0.6\ nF$ |
| $V_{Td}$ | $\sim 0\ V$ |
| $BV_f$ | 1.0 |
| $BV_n$ | 4 |

TABLE 3
Physical Constants of Si at $T = 25°C$

| | |
|---|---|
| $n_i$ | $1.45 \times 10^{10}\ cm^{-3}$ |
| $\mu_n$ | $1500\ cm^2/V\text{-}s$ |
| $\mu_p$ | $450\ cm^2/V\text{-}s$ |
| $\epsilon_{si}$ | $1.05 \times 10^{-12}\ F/cm$ |
| $\alpha_1$ | $1.428 \times 10^{20} (cmVs)^{-1}$ |
| $\alpha_2$ | $4.54 \times 10^{11} cm^{-2}$ |
| $v_{nsat}$ | $1.1 \times 10^7 cm/s$ |
| $v_{psat}$ | $0.95 \times 10^7 cm/s$ |

```
equations {
  i(gate - > cathode)      +=                     d_by_dt(Qgs)
  i(drain - > gate)        +=                 Cgd * dVdgdt
  i(drain - > cathode)     += Imos + Imult  +     d_by_dt(Qds)
  i(emitter - > cathode)   += Icss          + Ccer * dVecdt
  i(emitter - > drain)     += Ibss          +     d_by_dt(Q)
  i(anode - > emitter)     += Vae/Rb

  dVdgdt :  dVdgdt= d_by_dt(Vdg)
  dVecdt :  dVecdt= d_by_dt(Vec)
  Q      :  Vebq=Veb

  Nsat   :  Nsat=Ic/(q*A*vpsat) - Imos/(q*A*vnsat)
  mucinv :  mucinv = Pm*log( 1. + alpha2/Pm**(2./3.) )/alphal
  }
```

*Fig. 7. Equations section of Saber IGBT model template.*

Techniques Used to Ensure Convergence

The nonlinear solution algorithm (iteration algorithm) of the Saber circuit simulator is unique in that all of the nonlinear

expressions are evaluated in conjunction with an array of sample points for each of the independent variables. At the sample points, the nonlinear expressions are fully evaluated, while at intermediate values of the independent variables, the nonlinear functions are evaluated using multidimensional linear interpolations. One of the benefits of this algorithm in implementing model equations is that the partial derivitives of the model equations with respect to the system variables are not required in order for the simulator to iterate the system variables in a manner that converges to the solution of the system of nonlinear equations. Thus, the model equations can be implemented directly in a straightforward manner as describe above.

The range and density of the sample points can be tailored to the nature of the model nonlinearities by specifying the sample points arrays in the control section of the Saber template. The Saber simulator also provides the capability to control the maximum step size that a given variable can take between successive iterations (Newton steps) in regions where the nonlinear model functions have discontinuous partial derivitives with respect to the system variables. This feature of the Saber simulator is beneficial in implementing models which use different expressions to describe different regions of operation; for example, $I_{mos}$ is described by a different expression for gate voltages above and below $V_{gs} = V_T$. Newton steps for the independent variables can be introduced near the transition between different regions by specifying the Newton step arrays in the control section. The Newton steps tend to confine the iterations of the independent variables to the regions where they are introduced so that the variables do not overshoot the transition regions during iterations.

In implementing the IGBT model into the Saber simulator, the equations in Table 1 must be formulated such that they are continuous and nonsingular in the range that the system variables may take during iterations. For example, $C_{gdj}$ becomes infinite at $V_{dg} = -V_{Td}$ which would result in numerical overflows even though the reciprocal sum that describes $C_{gd}$ is well defined mathematically. This problem is alleviated by reformulating the gate-drain capacitance expression in terms of reciprocal capacitances so that only $1/C_{gdj}$ needs to be evaluated. Some of the expressions in Table 1 are only valid for limited ranges of the system variables and should be left undefined or be given a definite value in the inapplicable range. For example, the expression for $W_{gdj}$ is only applicable when a depletion region exists (i.e., $V_{dg} > -V_{Td}$), and the expressions would result in the square-root of a negative number otherwise.

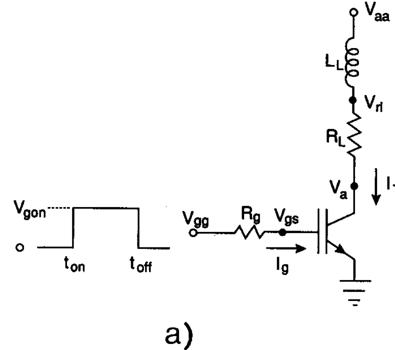
Other expressions are nonsingular and continuous in the range of all physical solutions to the nonlinear equations, but are not so in ranges which may be entered into during the iterations necessary to find the physical solution. For example, the expression for $W_{dsj}$ is not valid for $V_{ds} < -0.6\ V$, and although no physical solutions exist in this range, it is necessary to provide a value in this range, because the drain-source voltage can enter the $V_{ds} < -0.6\ V$ range during the iterations necessary to find the physical solution. However, the values of the expressions in the range where there are no solutions are only important during iterations and have no effect on the results of the model. Therefore, the functions are given values outside the physical range of operation which are continuous at some point arbitrarily near the singularity and that are well defined beyond the range of physical operation.

## IV. Model Evaluation and Validation

The Saber IGBT model described in the last section is evaluated using various test circuits to examine the device behavior for the range of static and dynamic conditions in which the device is intended to be operated. The evaluations are preformed for 20-$A$, 600-$V$ rated IGBTs with the same model parameters as the devices in ref. [3] (Table 2 and Table 3). The evaluations are demonstrated in this paper for a 7.1-$\mu s$ base lifetime, although the model has also been evaluated for faster devices with lower base lifetimes. Figure 8 shows the basic test circuit (a) and the corresponding net-list (b) used for the evaluations. Modifications to this net-list are also discussed below to describe the polarized active feedback snubber circuit results of ref. [3] and to describe the passive polarized turn-off snubber and soft clamp circuit results of ref. [4].

The statements in Fig. 8b describe each of the six circuit elements of Fig. 8a. The first column in these statements designates each component of the circuit, where the name of the given template that is used to model the component is given on the left-hand side of the period (.), and the name of the specific instance of the component within the circuit is given on the right-hand side of the period. The resistor, inductor, and voltage supply templates are provided within the Saber template library, and the user-defined IGBT template is described in Section III. The remaining columns to the left of the equal sign define the connection points for each component, where the names of these connection points are defined in Fig. 8a. The parameters of each component that are to be changed from the default values of the generic templates are given to the right of the equal signs.

Figure 9 compares the low anode voltage static characteristics of the Saber IGBT model (dashed lines) with the characteristics measured on a curve tracer (solid lines). The simulated characteristics are obtained using a Saber command file that varies the gate voltage in 1-$V$ steps and performs a dc sweep analysis for the anode voltage at each gate voltage step.




a)

# Net-list for IGBT with series resistor-inductor load and resistive gate drive.

| | | | | |
|---|---|---|---|---|
| V.Vaa | Vaa | 0 | | =300 |
| L.LL | Vaa | Vrl | | =80u |
| R.RL | Vrl | Va | | =30 |
| R.Rg | Vgg | Vgs | | =0.1k |
| Pulsgen.1 | Vgg | 0 | | =ton=1u, trise=20n, Vgon=20, toff=30u, tfall=20n |
| IGBT.1 | Va | Vgs | 0 | =tau_hl=7.1u |

b)

*Fig. 8. Series resistor-inductor load, resistive gate drive a) test circuit and b) corresponding net-list.*

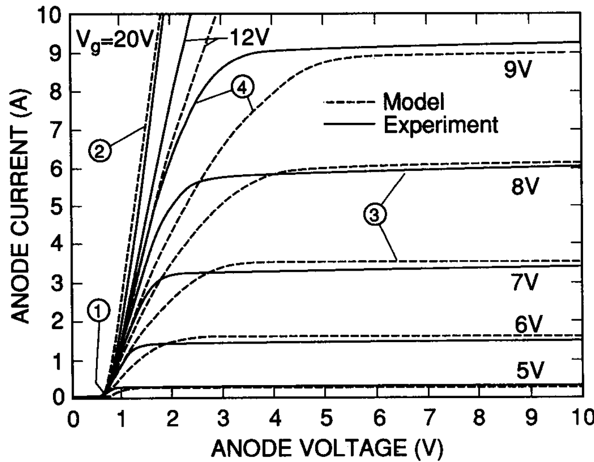



*Fig. 9. Measured and simulated static characteristics indicating 1) the diode voltage offset, 2) the low resistance on-state region, 3) the current saturation region, and 4) triode like region.*

The following features of the low-voltage static characteristics are indicated on Fig. 9: 1) the diode voltage offset due to the anode-epitaxial layer $p$-$n$ junction, 2) the on-state region which has a low resistance due to conductivity modulation, 3) the current saturation region which is due to saturation of the MOSFET channel current, and 4) the triode-like region which is referred to as the linear region for MOSFETs. The agreement between the simulated and measured static characteristics for 1) the diode voltage offset validates the implementation of $V_{ebq}$, 2) the on-state characteristics validate the implementation of $R_b$, and 3) the saturation characteristics validate the implementation of $I_{mos}, I_{bss}$, and $I_{css}$.

The triode-like region indicated as 4) in Fig. 9 has a steeper slope for the measured characteristics than for the simulated characteristics, due to the effect of the graded dopant density in the channel for the diffused body region. This behavior is typical of the channel current for the VDMOSFET structure [9]. However, the triode region is not as evident for power MOSFETs as it is for IGBTs, due to the large series resistance of the epitaxial layer in high-voltage MOSFETs. The VDMOSFET portion of the IGBT Saber model can be readily enhanced to include the following second-order effects on $I_{mos}$ [10]: 1) mobility reduction due to velocity saturation in the MOSFET channel, 2) mobility reduction due to the transverse electric field for high gate voltages, and 3) diffusion of carriers due to the nonuniform channel dopant density. For example, the triode region of the VDMOSFET structure studied in this work is well described by the semi-empirical expression: $I_{mos} = K_p K_f[(V_{gs} - V_T)V_{ds} - K_f V_{ds}^2/2]$ for $V_{ds} \leq (V_{gs} - V_T)/K_f$, where the empirical factor $K_f \approx 1.7$ represents the ratio of the apparent transconductance parameter $K_p$ in the triode region to that in the saturation region. A better fit to the high gate voltage transconductance is also obtained by dividing the $I_{mos}$ expressions by $1 + \theta(V_{gs} - V_T)$, where the empirical parameter $\theta \approx 0.02$ represents the reduction in transconductance at high gate voltage due to the transverse electric field.

The slope of the current saturation region (output conductance) is small for VDMOSFETs, because the channel length modulation effect is minimal for the lightly doped drain [9,10]. However, IGBTs do exhibit a significant output conductance for anode voltages larger than those in Fig. 9, due to the increase in the bipolar transistor current gain with decreasing neutral base width $W$ (Early effect), and due to the increase in avalanche multiplication. In addition, the IGBT anode current increases exponentially with anode voltage near the open-base, collector-emitter breakdown voltage of the internal bipolar transistor ($600V$). Both of these features of the high-voltage static characteristics of the IGBT (not shown in Fig. 9) are also well described by the Saber IGBT model.

Figure 10 compares the Saber IGBT model (dashed lines) with the measured (solid lines) anode voltage, anode current, gate voltage, and gate current waveforms for different values of gate resistance. These characteristics are obtained using a Saber command file that varies the gate resistance in values of 0.1 k, 1 k, 2 k, and 3 kΩ, and performs a transient simulation for each gate resistance. The agreement between the simulations and measurements as indicated on Fig. 10 for 1) the slowly decaying portion of the turn-off current waveform validates the implementation of $C_{ebd}$ and $I_{bss}$, 2) the value of the voltage overshoot at turn-off for the stiff gate drive ($R_g$ = 0.1 kΩ) validates the implementation of $C_{cer}$ which dominates the effective output capacitance, 3) the turn-off delay time for the different values of gate resistance validates the implementation of the low-voltage gate-drain capacitance, and 4) the anode voltage overshoot for different gate resistances validates the high-voltage gate-drain capacitance. The agreement between the simulated and measured gate voltage waveforms also validates the implementation of the VDMOSFET capacitances.

Figure 11 compares the simulated and measured anode voltage turn-off waveforms for an IGBT being switched off both with and without the protection circuits shown in Fig. 12. The anode voltage turn-off waveform of the $R_g$ = 0.1 kΩ curve in Fig. 10 is repeated on Fig. 11 for reference. The soft clamp circuit shown in Fig. 12a is connected to the anode terminal of Fig. 8a. For a polarized turn-off snubber, $R_s$ is connected to $V_a$ instead of $V_{aa}$. The simulations including the soft clamp are performed by adding the following statements to the net-list of Fig. 8b:

```
C.Cs        Vaa   Vcs   = 200n
R.Rs        Vaa   Vcs   = 1k
mr1366.Ds   Va    Vcs
```

where mr1366 is the part number of the 500-$V$, 6-$A$ power diode used in this circuit which is included in the Saber component library. For the large load inductance used in this circuit (200 $\mu H$), the anode voltage would overshoot the IGBT maximum rated voltage (600 $V$) if the protection circuit were not added, but with the protection circuit, the IGBT can be switched off without excessive voltage overshoot. The Saber IGBT model also predicts the IGBT anode current and the diode current waveforms for this circuit [4], and is thus useful in the design and selection of components for the protection circuit.

The polarized active snubber circuit shown in Fig. 12b is connected to the IGBT anode and the IGBT gate in the circuit of Fig. 8a. The simulations including the polarized active snubber are performed by adding the following statements to the net-list of Fig. 8b:

```
R.Rgon       Vron   Vgs    =0.1k
d1n4148.Dg   Vgg    Vron
R.Rf         Vcf    Vgs    =1k
C.Cf         Va     Vcf    =0.2n
```

where d1n4148 is the part number of the 50-$V$, 100-$mA$ small-signal diode used in this circuit which is included in the Saber component library. Notice that the voltage overshoot is reduced

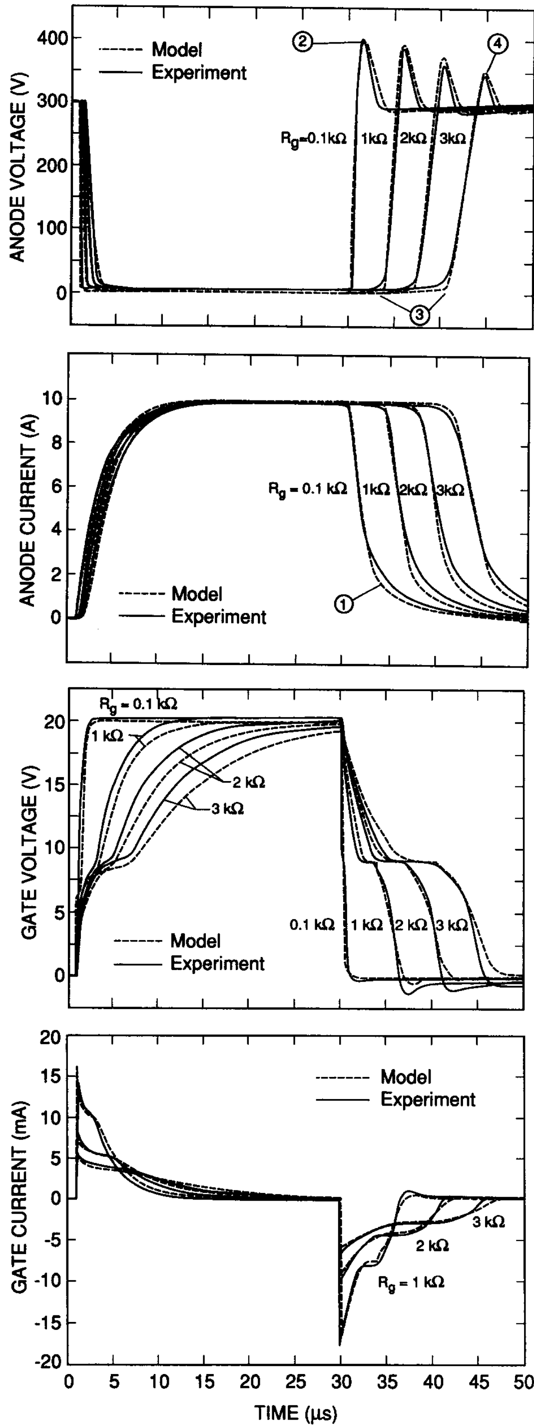



*Fig. 10. Measured and simulated anode voltage, anode current, gate voltage, gate current switching waveforms for different gate resistances. Indicated are 1) the slowly decaying portion of turn-off anode current waveforms, 2) the stiff gate drive, anode voltage overshoot, 3) the turn-off delay, and 4) the gate resistance effect on anode voltage overshoot.*

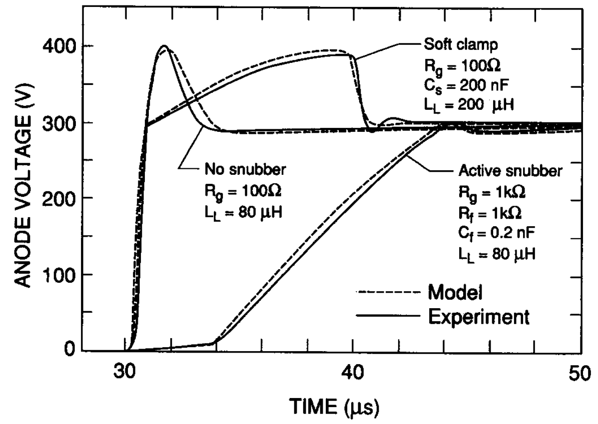



*Fig 11. Anode voltage waveform for an IGBT being switched-off with and without a protection circuit.*

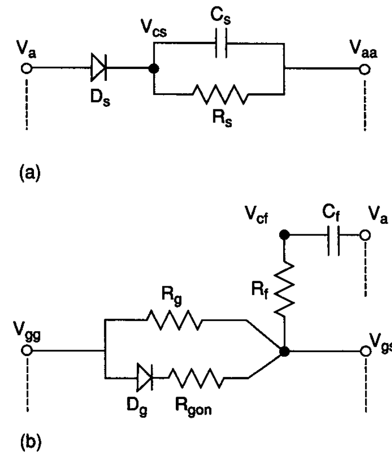



*Fig. 12 Protection circuits used for the waveforms in Fig 11. a) Soft clamp protection circuit, and b) polarized active snubber protection circuit.*

without the need for the large power diode and the large valued snubber capacitor necessary for the circuit of Fig. 12a, and without the large turn-off delay times that result for the large gate resistances of Fig. 10. The optimum component values for this type of protection circuit depend upon the IGBT characteristics as well as the load circuit parameters, and it is thus beneficial to examine the behavior of this circuit using the Saber IGBT model.

## V. Conclusions

The previously developed physics-based model for the IGBT is suitable for implementation into general purpose simulators. To incorporate the IGBT model into the Saber simulator, the model is formulated such that the currents between the terminal nodes are expressed in terms of the system variables, where several system variables are introduced to account for the non-integrable capacitance formulas, for the implicit emitter-base capacitance, and for the bias-dependent model parameters. The resulting Saber IGBT model performs well and describes exper-

imental results accurately for the range of static and dynamic conditions in which the device is intended to be operated. The model has been used to describe the steady-state and the dynamic characteristics for various external circuit conditions. It has been shown that the Saber IGBT model can be used to determine circuit parameters and component ratings in the design of protection circuits. The basic Saber IGBT model can be readily enhanced to describe the characteristics of IGBTs manufactured using the various power MOSFET technologies.

*Certain commercial software products are identified in this paper in order to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology , nor does it imply that these software products are the best available products for the purpose.*

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## NOMENCLATURE

| Symbol | Description |
|---|---|
| $A$ | Device active area ($cm^2$). |
| $A_{ds}$ | Body region area ($cm^2$). |
| $A_{gd}$ | Gate-drain overlap area ($cm^2$). |
| $b$ | $\mu_n/\mu_p$ Ambipolar mobility ratio. |
| $BV_{ceo}$ | Open-base, collector-emitter breakdown voltage ($V$). |
| $C_{bcj}$ | Base-collector depletion capacitance ($F$). |
| $C_{cer}$ | Collector-emitter redistribution capacitance ($F$). |
| $C_{dsj}$ | Drain-source depletion capacitance ($F$). |
| $C_{eb}$ | Implicit emitter-base capacitance ($F$). |
| $C_{ebj}$ | Emitter-base depletion capacitance ($F$). |
| $C_{ebd}$ | Emitter-base diffusion capacitance ($F$). |
| $C_f$ | External feedback capacitance ($F$). |
| $C_{gd}$ | Gate-drain capacitance ($F$). |
| $C_{gdj}$ | Gate-drain overlap depletion capacitance ($F$). |
| $C_{gs}$ | Gate-source capacitance ($F$). |
| $C_{oxd}$ | Gate-drain overlap oxide capacitance ($F$). |
| $C_s$ | Snubber capacitance ($F$). |
| $D_n, D_p$ | Electron, hole diffusivity ($cm^2/s$). |
| $D$ | $2D_nD_p/(D_n + D_p)$ Ambipolar diffusivity ($cm^2/s$). |
| $D_c$ | Carrier-carrier scattering diffusivity ($cm^2/s$). |
| $I_{bss}$ | Steady-state base current ($A$). |
| $I_c$ | Collector current ($A$). |
| $I_{ceb}$ | Emitter-base capacitor current ($A$). |
| $I_{ccer}$ | Collector-emitter redistribution current ($A$). |
| $I_{css}$ | Steady-state collector current ($A$). |
| $I_f$ | Feedback current ($A$). |
| $I_g$ | Gate current ($A$). |
| $I_{gen}$ | Collector-base thermally generated current ($A$). |
| $I_L$ | Load inductor current ($A$). |
| $I_{mult}$ | Avalanche multiplication current ($A$). |
| $I_{mos}$ | MOSFET channel current ($A$). |
| $I_{sne}$ | Emitter electron saturation current ($A$). |
| $I_T$ | Anode current ($A$). |
| $K_p$ | MOSFET transconductance parameter ($A/V^2$). |
| $K_f$ | Triode region MOSFET transconductance factor. |
| $L$ | Ambipolar diffusion length ($cm$). |
| $L_L$ | Series load inductance ($H$). |
| $M$ | Avalanche multiplication factor. |
| $N_B$ | Base doping concentration ($cm^{-3}$). |
| $n_{eff}$ | Effective base doping concentration ($cm^{-3}$). |
| $n_i$ | Intrinsic carrier concentration ($cm^{-3}$). |
| $N_{sat}$ | Velocity saturation component of $N_{scl}$ ($cm^{-3}$). |
| $N_{scl}$ | Collector-base space charge concentration ($cm^{-3}$). |
| $P_0$ | Carrier concentration at emitter end of base ($cm^{-3}$). |
| $\overline{\delta p}$ | Average carrier concentration in base ($cm^{-3}$). |
| $N_{scl}$ | Collector-base space charge concentration ($cm^{-3}$). |
| $q$ | Electronic charge ($1.6 \times 10^{-19} C$). |
| $Q$ | Instantaneous excess carrier base charge (C). |
| $Q_B$ | Background mobile carrier base charge (C). |
| $Q_{bi}$ | Emitter-base junction built-in charge (C). |
| $Q_{ds}$ | Drain-source capacitor charge (C). |
| $Q_{gs}$ | Gate-source capacitor charge (C). |
| $R_b$ | Conductivity-modulated base resistance ($\Omega$). |
| $R_f$ | Series feedback resistance ($\Omega$). |
| $R_g$ | Gate drive resistance ($\Omega$). |
| $R_{gon}$ | Turn-on gate resistance ($\Omega$). |
| $R_L$ | Series load resistance ($\Omega$). |
| $R_s$ | Snubber bleeder resistor ($\Omega$). |
| $V_a$ | Device anode voltage ($V$). |
| $V_{aa}$ | Anode supply voltage ($V$). |
| $V_{ae}$ | Conductivity-modulated base resistance voltage ($V$). |
| $V_{bc}$ | Base-collector voltage ($V$). |
| $V_{ce}$ | Collector-emitter voltage ($V$). |
| $V_{cf}$ | External feedback capacitor voltage ($V$). |
| $V_{dg}$ | Drain-gate voltage ($V$). |
| $V_{ds}$ | Drain-source voltage ($V$). |
| $V_{eb} \equiv V_{ebq}$ | Emitter-base capacitor voltage ($V$). |
| $V_{ebd}, V_{ebj}$ | Emitter-base diffusion, depletion voltage ($V$). |
| $V_{ec}$ | Emitter-collector voltage ($V$). |
| $V_{gg}$ | Gate pulse generator voltage ($V$). |
| $V_{gon}$ | Gate pulse voltage amplitude ($V$). |
| $V_{gs}$ | Gate-source voltage ($V$). |
| $V_T$ | MOSFET channel threshold voltage ($V$). |
| $V_{Td}$ | Gate-drain overlap depletion threshold ($V$). |
| $W$ | Quasi-neutral base width ($cm$). |
| $W_B$ | Metallurgical base width ($cm$). |
| $W_{bcj}$ | Base-collector depletion width ($cm$). |
| $W_{dsj}$ | Drain-source depletion width ($cm$). |
| $W_{gdj}$ | Gate-drain overlap depletion width ($cm$). |
| $\epsilon_{si}$ | Dielectric constant of silicon ($F/cm$). |
| $\mu_n, \mu_p$ | Electron, hole mobility ($cm^2/V$-$s$). |
| $\mu_c$ | Carrier-carrier scattering mobility ($cm^2/V$-$s$). |
| $\tau_{HL}$ | Base high-level lifetime ($s$). |
| $\theta$ | Transverse field transconductance factor ($1/V$). |