A BINARY INDUCTIVE VOLTAGE DIVIDER BRIDGE

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Abstract: An automatic bridge to calibrate inductive voltage dividers from 10 Hz to 100 kHz is described. The bridge is based on a programmable 30-bit binary inductive voltage divider with terminal linearity of 0.1 ppm at 100 Hz (linearity degrades to 10 ppm at frequency extremes). Measurements of programmable test dividers can be completely automated via the General Purpose Interface Bus (GPIB) using software developed to align the bridge components and perform an auto balance.

Measurement system

An automatic bridge has been developed to facilitate in the calibration of programmable, as well as manual, inductive voltage dividers (IVDs). The system is controlled by a computer via the GPIB.

A simplified scheme of the measurement system is shown in Fig. 1. It makes use of a dual channel sine-wave voltage source to supply the main bridge signal (channel A) as well as a quadrature injection signal (channel B).

A lock-in detector is used to sense the in-phase and quadrature differences between the standard and test IVDs. The reference signal for this detector is derived from channel A of the voltage source. By phase shifting the reference signal in the detector it is possible to align this signal with the in-phase component of the difference between the standard and test IVD. The detector then displays both in-phase and quadrature difference components.

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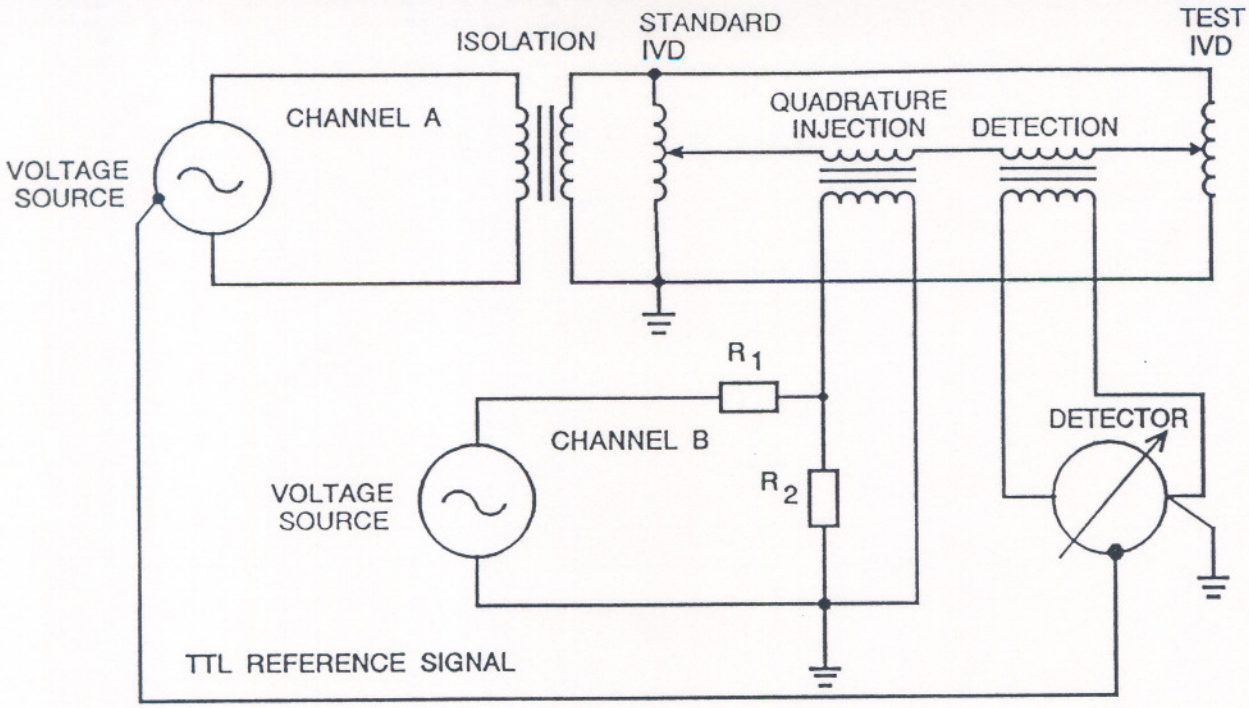

Fig. 1. IVD bridge.

This bridge alignment procedure consists of two steps.

Reference alignment :

The test divider is set to the nominal ratio and the standard divider is set to 1.01 times the nominal ratio. It is assumed that the large difference registered by the detector is in phase with the input signal. The phase of the detector reference signal is shifted to bring the quadrature display to zero.

Quadrature alignment:

When properly aligned the bridge can be balanced with a single iteration.

Binary Inductive Voltage Divider

A 30-bit BIVD was developed to serve as a standard in the automatic IVD bridge. The design of this divider is similar to those described in references [1] and [2]. The BIVD, schematically shown in Fig 2., consists of four relay-switched, binary transformers that are controlled via the GPIB. The first section is a two-stage 7 bit binary inductive voltage divider designed to operate at low frequencies. It consists of a magnetizing winding and 7 separate windings (twisted pairs) wound in a binary sequence. The second section is also a two-stage BIVD, but with 8 bits. The third and fourth sections are small single-stage BIVDs with 8 and 7 bits respectively.

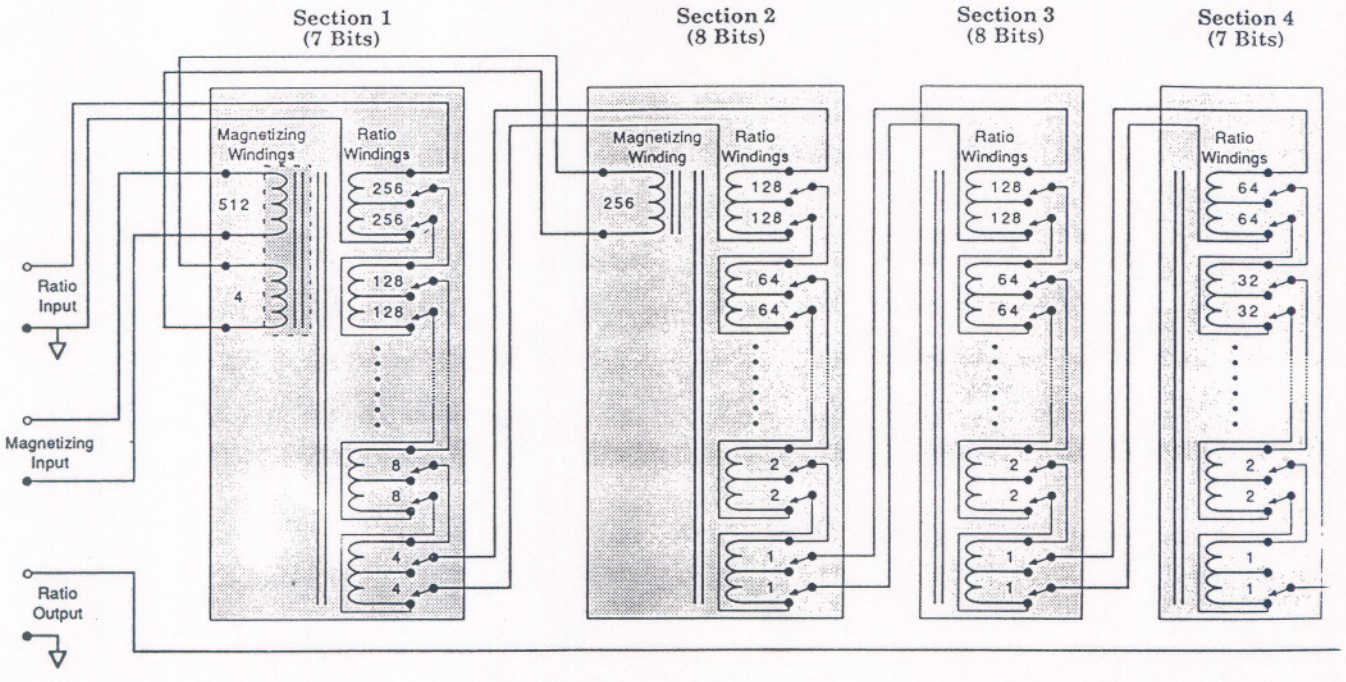

Fig. 2. 30-bit BIVD.

The BIVD is designed to have optimum performance at mid-frequencies when all four sections are used. As the operating frequency increases, the most significant sections are switched out to maintain maximum accuracy. The sections used (and subsequent resolution) at various frequencies are given in Table 1.

Frequency range	Sections used	Total number of bits	Resolution (ppm)
10 Hz - 2 kHz	1,2,3,4	30	0.001
2 kHz - 20 kHz	2,3,4	23	0.1
20 kHz - 100 kHz	3,4	15	30

Table 1. BIVD resolution on different frequency ranges.

Because of the binary structure of this instrument, the largest errors are likely to occur at the transitions of the most significant bits. A separate standard divider was made to measure its bit transition errors.

For a binary divider the bit transition error, e_n, is defined as:

$$e_n = (U_m - U_n - U_N)/U_{in},$$

where:

N is total number of bits,

n is the bit number at which the transition error is measured,

U_n is the voltage difference between taps of the standard and test divider with both set to a binary ratio of 2^{N-n},

U_m is the voltage difference with standard divider set to 2^{N-n} and test divider set to $2^{N-n} - 1$,

U_N is the ideal voltage of the least significant bit,

U_{in} is the voltage applied to both dividers.

For example, when n=2, N=8, $U_N = U_{in}/256$ and the binary ratios are

$$[2^{N-n}] = 0100\ 0000, \qquad [2^{N-n} - 1] = 0011\ 1111\ .$$

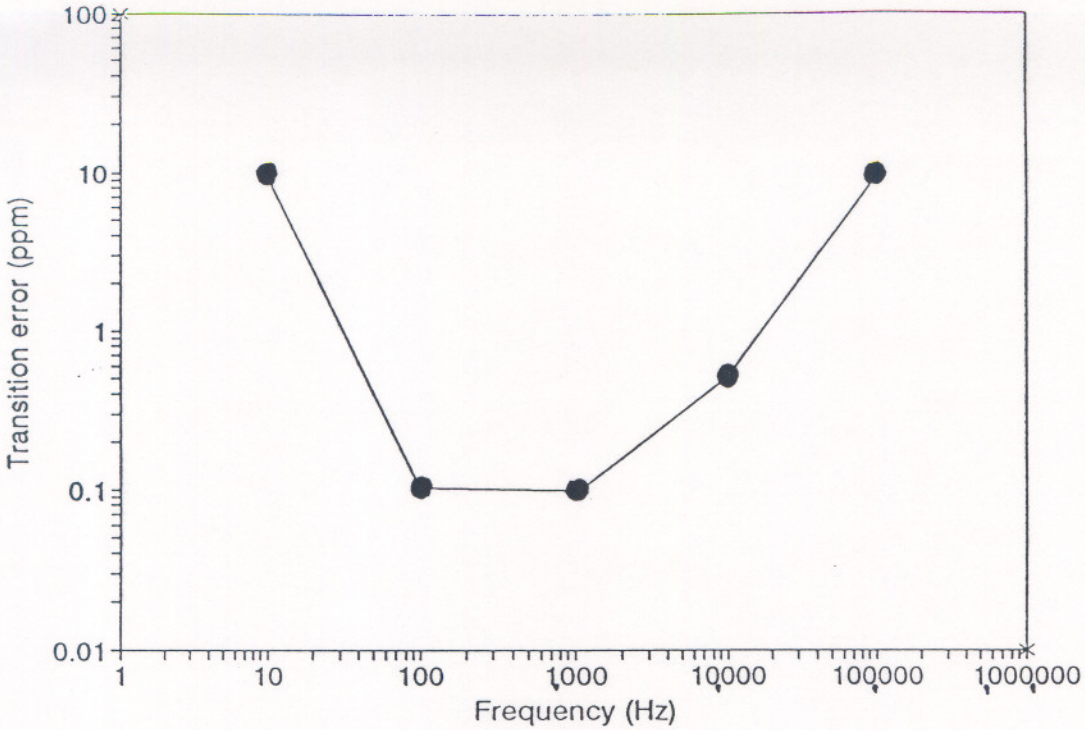

Fig. 3. BIVD most significant bit transition error for the operating frequency range.

BIVD bit transition errors for the most significant bit at different frequencies are given in Fig. 3. By correcting for this and other transition errors it is possible to perform automatic calibrations of programable IVDs with the uncertainties of 0.1 ppm in the mid frequency range.

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References.

[1] N.M. Oldham "A 50 ppm ac reference standard which spans 1 Hz to 50 kHz", IEEE Trans. Instrum. Meas., vol. IM-32, pp. 176-179, Mar. 1983.

[2] N.M. Oldham, O. Petersons, B.C. Waltrip "Audio-Frequency Current Comparator Power Bridge: Development and Design Considerations", IEEE Trans. Instrum. Meas., vol. IM-38, No. 2, April 1989.