Silicon Carbide PiN and Merged PiN Schottky Power Diode Models Implemented in the Saber Circuit Simulator

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Abstract- Dynamic compact electrothermal models are developed for silicon carbide (SiC) power diodes. Model parameters are extracted and model results are presented for both 1500 V SiC Merged PiN Schottky and 5000 V SiC PiN diodes. The models are verified for on-state characteristics' temperature dependence and reverse recovery characteristics' di/dt, dv/dt, and temperature dependence.

I. INTRODUCTION

Almost all circuit simulators contain library parts for various commercially available silicon (Si) devices, but there has yet to be a commercially available silicon carbide (SiC) device library component. This is largely due to the fact that SiC technology is still in its infancy and reliable devices are just beginning to appear. The first generation of these new SiC devices includes Merged PiN Schottky (MPS) and PiN power diodes. These devices have been compared to similarly rated silicon devices and proved to provide significant performance advantages for on-state characteristics, reverse recovery characteristics, temperature dependence, power converter efficiency, and electromagnetic interference [1].

In this paper, dynamic electrothermal circuit simulator models are developed based on the Mantooth unified diode model available in the Saber[®] circuit simulator [2], [3]. These models are used to describe the characteristics of several prototype SiC power diodes. Model results will be presented here for a 0.5 A rated (0.0045 cm²) 1500 V SiC MPS diode, a 0.25 A rated (0.002 cm²) 5 kV SiC PiN, and a 20 A rated (0.04 cm²) 5 kV SiC PiN. The models are verified for the onstate characteristics versus temperature and for a wide range of switching conditions that could occur in various applications.

II. BACKGROUND

SiC power devices are expected to show superior performance compared to devices made with other semiconductors. This is primarily because 4H-SiC has an order of magnitude higher breakdown electric field $(2 \times 10^6$

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V/cm to 4×10^6 V/cm) and higher temperature capability than conventional Si materials. The higher breakdown electric field allows the design of SiC power devices with thinner (0.1 times that of silicon devices) and more highly doped (more than 10 times higher) voltage blocking layers. For majority carrier power devices such as power Schottky diodes, the combination of 0.1 times the blocking layer thickness with 10 times the doping concentration can yield a SiC device with a factor of 100 advantage in resistance compared to that of Si majority carrier devices. For minority carrier conductivity modulated devices such as the PiN diode, a blocking layer of 0.1 times the thickness of a Si device can result in a factor of 100 faster switching speed. This is possible because the diffusion length, L, required to modulate the conductivity of the blocking layer can also be reduced to 1/10th the value required for Si, thus permitting the reduction of the lifetime,

 τ , by a factor of 100 according to $L = \sqrt{D\tau}$, where D is the diffusion coefficient. Because SiC has a larger band gap (3.26 eV for 4H-SiC [4] versus 1.1 eV for Si), SiC devices can be made to operate reliably at much higher temperatures than their Si counterparts (300 °C for SiC versus 150 °C for Si).

Recently, a new class of power semiconductor devices has begun to emerge that utilizes the advantages of SiC. Because power rectifiers are more easily produced than three terminal power-switching devices, they are expected to be among the first SiC electronic components to become available for commercial application. Generally speaking, there are three classes of SiC power rectifiers: (a) Schottky diodes, which offer extremely high switching speed but suffer from high leakage current; (b) PiN diodes, which offer low leakage current but show reverse recovery charge during switching and have a large junction forward voltage drop due to the wide band gap of 4H-SiC; and (c) Merged PiN Schottky (MPS) diodes, which offer Schottky-like on-state and switching characteristics. and PiN-like off-state characteristics [5]. It has been shown that a 1500 V SiC MPS diode provides superior performance over Si diodes with voltage ratings of 600 V to 1500 V [6], and that a SiC PiN diode has superior performance compared to Si diodes with voltage ratings from 1200 V to 5000 V [1].

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III. REVERSE RECOVERY TEST SYSTEM

Fig. 1a shows the test circuit used for characterizing the diodes for reverse recovery, and Fig. 1b shows the behavioral representation including parasitic elements used for diode model validation. The circuit of Fig. 1a uses a 6LF6 vacuum tube as a switch in place of the usual MOSFET switch to achieve low parasitic capacitance at the DUT (Device Under Test) anode and an extremely fast switching speed. The resistor R isolates the DUT from the parasitic capacitance of the inductor and is also used to quickly reset the inductor current to zero after each test. The dv/dt of the square wave applied to the tube screen is varied to achieve different di/dt values for the DUT. With a 700 V peak drive to the screen grid of the tube, the test circuit can test up to 9 A of combined forward and reverse DUT current, and the applied voltage to the DUT can be up to 2000 V.

The reverse recovery tests are performed for various values of V_{drive} , di/dt, and dv/dt where dv/dt is controlled by placing various capacitors across the DUT. By independently controlling V_{drive} , di/dt, and dv/dt the new test circuit enables testing the diode for the full range of conditions that occur for various application conditions. Varying the value of V_{drive} emulates the application conditions for circuits with different DC buss voltages, varying the value of di/dt emulates the application conditions of different speed anti-parallel switching devices, and varying the value of dv/dt emulates the application conditions of using anti-parallel switching devices of different output capacitance. Also, varying the value of dv/dt aids in the determination of the portion due to device capacitance.

The behavioral representation of the test circuit, Fig. 1b, uses an ideal bipolar transistor model with a local emitter degeneration resistor, Re, to emulate the di/dt applied by the tube. The bipolar transistor model capacitance parameters are set to zero and replaced by the constant 40nF capacitance of the tube (combined with C_{drive} in Fig. 1b). The next most important parasitic elements of the circuit are the 100 nH tube inductance L_t and the 50 Ω tube resistance R_t that result in a small voltage overshoot near the end of the diode current recovery waveform. The amplitude of the pulse generator waveform $V_b=19$ V and the emitter resistor $R_e=2$ Ω emulate the 9 A saturation current behavior for the tube circuit in Fig. 1a. The pulse width of the signal generator V_b is varied to determine the forward current for the reverse recovery test, and the rise time of V_b determines the di/dt applied to the DUT at turn off.

IV. SIC COMPACT MODEL FOR CIRCUIT SIMULATION

The SiC compact power diode model for circuit simulation is capable of modeling a wide variety of technologies. The SiC model is based on the Mantooth unified diode model available in the Saber circuit simulator. Since the SiC model is based on the Mantooth model, it is capable of



Fig. 1a. Circuit diagram for the high-speed diode reverse recovery test system.



Fig. 1b. Behavioral equivalent circuit used to emulate the test system of Fig. 1a.

accurately describing forward-bias, reverse-bias, forward recovery, reverse recovery, temperature dependence, and self-heating conditions. The primary interests of the research presented here are the forward-bias condition, reverse recovery condition and the temperature dependence in these regions.

To describe accurately the transient characteristics of the power diodes, the model uses two forms of the diode equation. First, the most widely known form,

$$i = IS(e^{v_j/N \cdot v_T} - 1),$$
 (1)

is used for depletion region recombination and emitter recombination, where *IS* is the saturation current, V_j is the forward diode voltage, *N* is the emission coefficient, and V_T is the thermal voltage. Similar equations to (1) are used for the high and low level injection regions, but in this case the equations are coupled to provide better continuity and flexibility in characterization to form

$$i_{0} = \frac{2i_{L}}{1 + \left[1 + \left(2\frac{ISL}{ISH}\right)N_{eff}e^{V_{f}/V_{T}}\right]^{N_{eff}}},$$
(2)

where

$$N_{eff} = \frac{1}{\frac{1}{NL} - \frac{1}{NH}}.$$
(3)

In (2), i_L is the low level injection current that takes the form of (1), and *ISL*, *ISH*, *NL*, and *NH* are the saturation currents for the low and high level injection regions and the corresponding emission coefficients, respectively. The value of i_0 is the current value used in calculating the total injected charge, q_0 . The injected charge is calculated using

$$q_0 = TT \cdot i_0, \tag{4}$$

where *TT*, the carrier lifetime, is a model parameter. This implementation represents the device physics where the stored charge results from the forward injection current and not the depletion region recombination or emitter recombination current. The charge, q_0 , is then divided into two portions: Q_{SW0} , the portion that is removed via sweep out effects, and Q_{R0} , the portion that recombines or diffuses out of the drift zone. To divide the charge, the model parameter *ALPH*0 is invoked as follows:

$$Q_{SW0} = ALPH0 \cdot q_0, \text{ and}$$
(5)

$$Q_{P0} = (1 - ALPH0) \cdot q_0. \tag{6}$$

The SiC model also utilizes a two time constant response or *double-tau model*. The model parameters *TSW* and *TM* control the nonquasi-static charge sweep out effect and the nonquasi-static diffusion effect, respectively.

TT, TSW, and TM can be varied according to temperature through relationships of the form

$$TT(T) = TT(T_{nom}) \cdot \left(\frac{T}{T_{nom}}\right)^{p},$$
(7)

where each time constant possesses a unique β and the model parameters are defined at a nominal temperature, T_{nom} . The forward-biased saturation currents available in the model are also a function of temperature. Their relationships have the following form

$$IS(T) = IS(T_{nom}) \cdot \left(\frac{T}{T_{nom}}\right)^{XTI/N} \cdot e^{[(T/T_{nom})-1](E_g/NV_T)},$$
(8)

where *XTI* is the saturation current temperature parameter and Eg is the semiconductor bandgap.

The temperature dependence of the forward series contact resistance, RS, implemented to provide greater flexibility in describing the series resistance due to the device and package effects, is given by

$$RS(T) = RS(T_{nom}) \cdot ((1/T_{nom})^{\gamma} T^{\gamma} + TRS1(T - T_{nom}) + TRS2(T - T_{nom})^{2}),$$
(9)

where γ is the exponential temperature parameter, *TRS1* is the linear temperature parameter, and *TRS2* is the quadratic temperature parameter.



Fig. 2. Simulated (dashed) and measured (solid) on-state characteristics for the 1500 V SiC MPS diode.

V. SIC MERGED PIN SCHOTTKY (MPS) DIODE MODEL

The SiC MPS diodes studied in this work are designed such that the PiN diode does not turn on in normal forward bias operation. This type of operation is typically referred to as the junction-barrier-controlled-Schottky (JBS) diode mode. The PN junctions serve only to shield the Schottky barrier from high electric fields, thus preventing Schottky barrier lowering and reducing leakage current.

Fig. 2 shows the simulated (dashed) and measured (solid) on-state characteristics for the 1500 V SiC MPS diode for different temperatures in the range of 25 °C to 225 °C. In these curves, the built-in potential decreases with increasing temperature because the increasing thermal energy of electrons in the metal surmounts the Schottky barrier height at a lower forward voltage. The decrease in slope of the onstate voltage curves with increasing temperature is indicative of the reduction of mobility with temperature for a majority carrier device.

The model parameter γ must be used along with *TRS1*, *TRS2*, β , and *XTI* in order to provide an accurate fit for the temperature dependence of the MPS diode's on-state characteristics.

Fig. 3 shows the measured (solid) and simulated (dashed) reverse recovery waveforms of the 1500 V SiC MPS diode for two different di/dt values and no external driver capacitance. Fig. 4 shows the measured (solid) and simulated (dashed) reverse recovery waveforms for the same di/dt but with two different values of external driver capacitance, C_{drive} . Fig. 5 shows the measured (solid) and simulated (dashed) reverse recovery waveforms versus temperature for a di/dt of 95 A/µs and no external driver capacitance. Waveforms for both 25 °C and 225 °C are shown, demonstrating that the MPS diode has no reverse recovery temperature dependence. In these figures, the initial measured

forward current is 0.6 A and the diode is switched by applying a constant negative di/dt with the tube. The tube current decreases linearly until it saturates at -9 A or when the voltage reaches the voltage supply value, V_{drive} . In general, the negative tube current is supplied by the device minority carrier charge reverse recovery current and the capacitive current through the DUT junction capacitance,



Fig. 3. Measured (solid) and simulated (dashed) reverse recovery waveforms of the 1500 V SiC MPS diode for two different di/dt values and no external driver canacitance.



Fig. 4. Measured (solid) and simulated (dashed) reverse recovery waveforms of the 1500 V SiC MPS diode for two different values of external driver capacitance C_{drive}.



Fig. 5. Measured (solid) and simulated (dashed) reverse recovery waveforms versus temperature for a di/dt of 95 A/µs and no external driver capacitance.

the DUT package capacitance C_p , the external driver capacitance C_{drive} , and the tube parasitic capacitance.

These waveforms demonstrate the wide range of applications to which this new SiC power diode model can be applied. In MPS diode modeling it is necessary to set TT equal to zero since it operates primarily like a Schottky diode. Setting TT to zero eliminates charge storage effects from the model. Thus, the MPS model provides the correct reverse recovery response, one that is capacitive in nature with no minority carrier charge storage.

The voltage waveforms in Figs. 3 and 4 are determined by the rate that the tube current charges the tube capacitance, the external driver capacitance, and the DUT capacitance. In Fig. 3, the dv/dt is faster for the higher di/dt curve because the tube current reaches a larger negative value during the voltage rise phase and thus charges the capacitance faster. In Fig. 4, the dv/dt seen by the diode is reduced for the added driver capacitance because the same tube current charges the additional external driver capacitance. From Figs. 3 and 4 one can conclude that the MPS reverse recovery is capacitive in nature and does not have a minority carrier charge storage time. This conclusion is reached by observing that the reverse voltage rise occurs during the entire reverse current period.

The diode capacitance can be calculated from these waveforms by dividing the instantaneous reverse current by the dv/dt value. For example, the high di/dt curve in Fig. 3 (di/dt equal to 95 A/ μ s) has a maximum dv/dt equal to 60 V/ns and the maximum reverse current is 0.2 A at this point. Using these values, the capacitance is calculated to be 3.3 pF when the reverse voltage is equal to several hundred volts. This value is a combination of the junction depletion

capacitance and the package parasitic capacitance and does not vary with temperature as observed in Fig. 5.

VI. SIC PIN DIODE MODEL

Fig. 6 shows the simulated (dashed) and measured (solid) on-state characteristics for the 0.002 cm² 5000 V SiC PiN diode for different temperatures in the range of 25 to 225 °C. Because the bandgap for 4H-SiC is 3.26 eV, the built-in potential for the SiC PiN diode is nearly 3 V. The decrease in on-state voltage with temperature is indicative of the decrease in built-in potential with increasing temperature and the increase in lifetime with temperature for conductivity modulated devices. The SiC PiN model is capable of modeling both the decrease in built-in potential and the increase in lifetime by providing the user with temperature parameters for carrier lifetimes and saturation currents. Also, it is apparent that the model strays from the measured curve slightly at low current. This is primarily due to the high contact resistance inherent in the early generations of SiC devices.

The reverse recovery switching tests are performed using the same techniques for controlling di/dt and dv/dt as discussed in the previous section. Fig. 7 shows the measured (solid) and simulated (dashed) reverse recovery waveforms of the 5000 V SiC PiN diode for three different di/dt values and no external driver capacitance. For the lowest value of di/dt (27 A/ μ s), the reverse recovery current is determined by the device capacitance, whereas a stored charge recovery peak becomes more evident as the di/dt is increased (i.e. 95 A/ μ s and 224 A/ μ s curves).

Fig. 8 shows the measured (solid) and simulated (dashed) reverse recovery waveforms for the same di/dt, but with three different values of external driver capacitance C_{drive} . As the driver capacitance is increased from 0 pF to 2000 pF, the voltage rate of rise is decreased and the internal diode capacitor current is reduced. For the case where no driver capacitance was added, the reverse current waveform consists of a stored charge recovery portion followed by the capacitive portion. For the case of the highest driver capacitor value ($C_{drive} = 2000 \text{ pF}$), dv/dt is substantially reduced and the current required to charge the internal diode capacitance is minimal. Thus, the waveforms consist of a stored charge recovery portion followed by a small current tail due to the decay of the remaining stored charge.



Fig. 6. Simulated (dashed) and measured (solid) on-state characteristics for the 0.002 cm² 5 kV SiC PiN diode.



Fig. 7. Measured (solid) and simulated (dashed) reverse recovery waveforms of the 5 kV SiC PiN diode for three different di/dt values and no external driver capacitance.



Fig. 8. Measured (solid) and simulated (dashed) reverse recovery waveforms for the same di/dt but with three different values of external driver capacitance C_{drive}.



Fig. 9. Simulated (dashed) and measured (solid) on-state characteristics for the 0.04 cm² 5 kV SiC PiN diode.

The SiC model scales well with device area and current rating. The measured temperature dependence of the on-state characteristics for the 5 kV, 20 A (0.04 cm²) rated SiC PiN diode is shown in Fig. 9. Again, the decrease in on-state voltage with temperature is indicative of the increase in lifetime with temperature for a conductivity modulated device, and a decrease in bandgap of the PN junction. However, at a high temperature of 225 °C, a reduction in carrier mobility starts to increase the differential onresistance across the drift layer. This leads to a cross-over in the I-V characteristics at a high current density of 500 A/cm². In the entire 25 °C to 225 °C range, the on-state voltage drop remains in a somewhat insignificant 0.4 V range, as seen from Fig. 9. This shows that SiC PiN diodes are remarkably stable with increasing temperature.

VII. CONCLUSION

Dynamic electrothermal circuit simulator models are developed for silicon carbide power diodes. The models are validated for the on-state characteristics' temperature dependence and reverse recovery characteristics' di/dt, dv/dt, and temperature dependence. The verification is performed using a well-characterized test system that enables independent variation of each of the circuit condition parameters. Both the SiC MPS model and the SiC PiN model perform well for the wide range of test circuit conditions and temperatures.

REFERENCES

- A. Hefner, R.Singh, J.S. Lai, D.W. Berning, S. Bouche, C. Chapuy, "SiC power diodes provide breakthrough performance for a wide range of applications," *IEEE Trans. on Power Electronics*, vol. 16, no. 2, March 2001.
- [2] H. A. Mantooth, J. L. Duliere, "A unified diode model for circuit simulation," *IEEE Trans. on Power Electronics*, vol. 12, no. 5, September 1997.
- [3] Saber is a registered trademark of Avant! Inc., 9205 SW Gemini Dr., Beaverton, OR, 97008. Certain commercial products or materials have been identified in order to specify or describe the subject matter of this paper adequately. This does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that these products are the best for the purpose.
- [4] N. G. Wright, D. J. Morrison, "Electrothermal simulation of 4H-SiC power devices," *Materials Science Forum*, vols. 264-268, 1998.
- [5] R. Singh, S. Ryu, J. Palmer, A. Hefner, J. Lai, "1500 V, 4 Amp 4H-SiC JBD diodes," Proceedings of the 2000 International Symposium on Power Semiconductor Devices and ICs, pp. 101-104, May 2000.
- [6] A. Hefner, D. Berning, J. Lai, C. Liu, and R. Singh, "Silicon Carbide Merged PiN Schottky diode switching characteristics and evaluation for power supply applications," *Conference Recordings of IEEE IAS Annual Meeting, October 2000.*