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Nanofabricated SNS junction series arrays in superconductor–normal metal bilayers

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Abstract
We have applied our existing focused ion beam based nanoscale planar SNS bridge junction technology to the fabrication of series arrays, with a view to lumped array applications. Single junctions are created in a micrometre-width bilayer track (125 nm Nb on 75 nm Cu) by milling a trench 50 nm wide in the upper superconducting layer. Individual junctions with non-hysteretic, resistively-shunted current–voltage characteristics, critical current $I_C \sim 1$ mA and characteristic voltage $I_C R_N \sim 50$ μV at 4.2 K can be fabricated routinely. The characteristics of 10-junction series arrays at junction spacings of 0.2 μm to 1.6 μm have been studied at 4.2 K and above. Locking of all the junctions in the array under an applied microwave field is observed as the transition temperature is approached. This effect is achieved at a lower temperature for shorter junction spacings, suggesting a penetration depth-dependent electromagnetic coupling mechanism. Measurements of differential resistance versus current reveal the I_C distribution of individual junctions within the array. Spreads of critical current $\delta I_C = I_{Cmax}/I_{Cmin} \sim 1.5$ at 4.2 K are typically observed. The spread in normal state resistance, R_N between junctions is negligible in comparison, as the unbroken normal metal layer shunts all of the junctions in the array. This allows locking to be achieved in spite of the appreciable spread in I_C.

1. Introduction

A nanoscale junction technology is required for lumped arrays, which would allow increased output voltages for both programmable and ac voltage standards [1, 2]. We have developed a reliable and versatile technique for fabricating nanoscale SNS junctions in superconductor normal metal bilayers using a focused ion beam microscope [3, 4]. A micrometre-width track is defined in the bilayer. A trench 50 nm wide is milled in the upper superconducting layer to achieve weak coupling. We are able to determine the depth of the trench by an *in situ* resistance measurement technique [4, 5]. In this device architecture the majority of the Josephson current transport is through the remaining Nb in the bottom of the trench; the normal layer acts as a resistance shunt and heat sink [4]. By carefully selecting the thicknesses of the superconducting and normal metal layers (125 nm Nb on 75 nm Cu), junctions with non-hysteretic current–voltage characteristics corresponding to the resistively shunted junction (RSJ) model, critical current (I_C) $\sim$ 1 mA per micrometre of track width and characteristic voltage ($I_C R_N$) $\sim$ 50 μV at 4.2 K can be obtained over a range of milling depths. The choice of normal metal is significant, as

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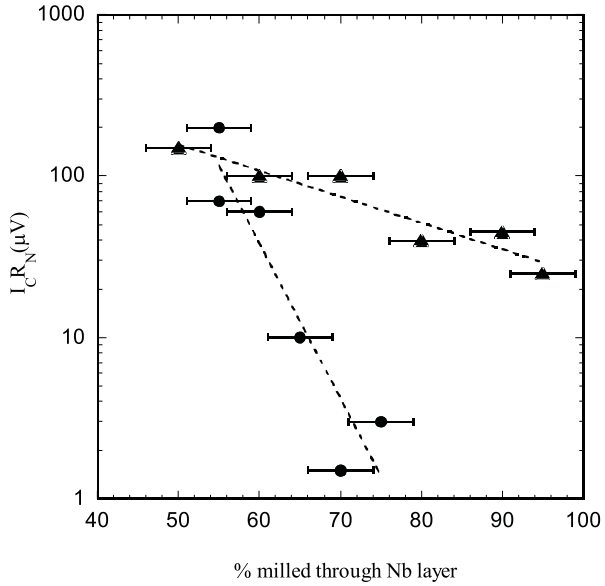

Figure 1. $I_C R_N$ versus percentage milled through Nb layer for 125 nm Nb 75 nm Cu (triangles) and 125 nm Nb 50 nm PdAu (circles). The uncertainty in the milling depth is ±5 nm (∼4%).

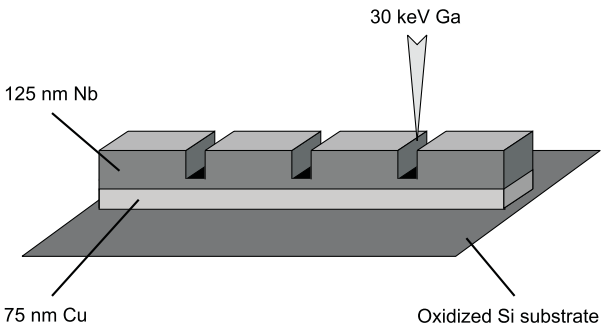

Figure 2. Schematic diagram of the array-writing procedure.

illustrated in figure 1. Figure 1 shows individual junction $I_C R_N$ (at 4.2 K) versus percentage milled through the Nb layer for 125 nm Nb 75 nm Cu and 125 nm Nb 50 nm PdAu bilayers. In both cases the normal metal layer thickness is greater than the dirty limit coherence length at 4.2 K. This figure shows clearly that with a cleaner normal metal (Cu) a slower variation of $I_C R_N$ with milling depth is achieved. For lumped array applications a spacing between individual junctions of ∼100 nm would be required [2]. Using the FIB (spot size ∼10 nm) the junctions can in principle be placed as close together as one wishes. Early studies of coupling between pairs of junctions [6] suggested that in this geometry individual junction properties are only degraded when the nearest neighbour spacing is much less than 100 nm, over which length scale order parameter and quasiparticle coupling mechanisms through the unbroken normal metal layer come into play.

2. Device fabrication

A 125 nm Nb 75 nm Cu bilayer is deposited on an oxidized Si substrate in an ultra-high vacuum magnetron sputtering system

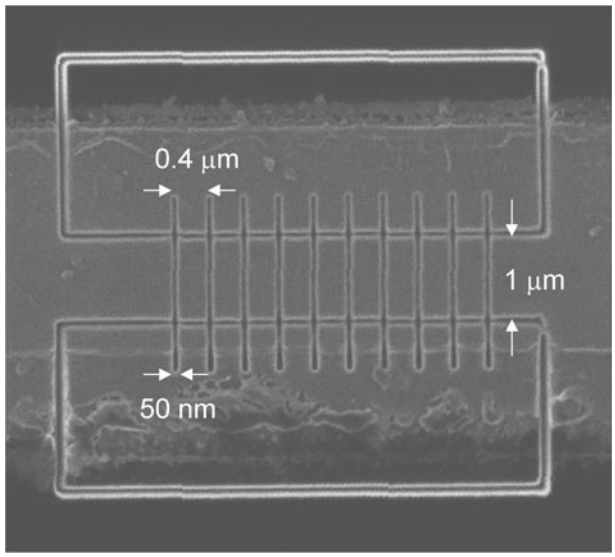

Figure 3. A finished 10-junction array viewed from directly above in the FIB. The track width was narrowed to 1 μm on an 11 pA beam current (large rectangles). The array of 10 2 μm × 50 nm lines (spacing 0.4 μm) was milled on a 4 pA beam.

in sequence without breaking vacuum. This ensures both excellent film and interface quality. A main track containing sections of width 3–8 μm intersected by voltage taps is defined in the bilayer by photolithography and reactive ion etching. The patterned sample is wirebonded to a holder in a four-point resistance measurement configuration and the sample is transferred to a standard focused ion beam microscope (FIB) for device fabrication. The FIB uses a liquid Ga source and the column voltage is 30 keV. A region of track 1 μm wide is defined by milling on a high beam current (11 pA). Then an array of junctions is milled using a 4 pA beam either in series (milling each junction sequence) or in parallel (milling the array as a single object). For comparison a single junction is milled in a neighbouring section of track. This whole process is performed without altering the beam focus. A schematic diagram of the array writing procedure is shown in figure 2. The milling depth can be deduced from an *in situ* resistance measurement. Customized software allows us to halt milling when the desired change in resistance (and hence milling depth) is reached. For this study arrays of 10 junctions with spacings of 0.2 μm to 1.6 μm were milled in parallel along the main track of a single 10 mm × 10 mm chip. The milling time per junction (area milled 2 μm × 50 nm) was 11 s. A finished array (spacing 0.4 μm) is shown in figure 3.

3. Results

Basic device characterization was performed between 4.2 K and the transition temperature (T_C) using a dip probe including magnetic field coils and microwave antenna. Current–voltage (I–V) characteristics were obtained in a quasi-static current-biased measurement. Microwave measurements were possible in the range 12–18 GHz.

If a microwave signal is applied to a series array of N phase locked Josephson junctions, the first Shapiro step will appear at a voltage $V = N(h/2e) f_{HF}$, where f_{HF} is the microwave

Table 1. Statistics for arrays of spacings 0.2 to 1.6 μm at 4.2 K. The beam was refocused for the milling of each array, so although the current, area, and milling time per junction were equal, the focusing conditions are only identical for junctions within that particular array.

Spacing (μm)	I_C (μA) Min	Max	Mean	Spread (standard dev./mean) (%)	δI (I_{max}/I_{min})	Locking temperature (K)
0.2	890	1700	1389	19.8	1.56	4.2
0.4	2140	3000	2521	10.7	1.40	5.0
0.6	510	1410	904	36.2	2.76	—
0.8	980	1510	1291	11.8	1.54	5.0
1.6	1290	1970	1550	12.3	1.53	5.5

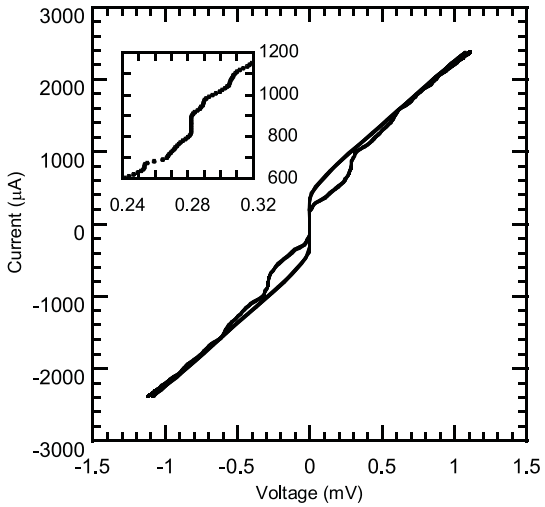

Figure 4. 10JJ array (spacing 1.6 μm) at 6.0 K exhibiting a nearly flat Shapiro steps (14.0 GHz). Inset: low-noise measurement of $\times 10$ step exhibiting non-ideal features.

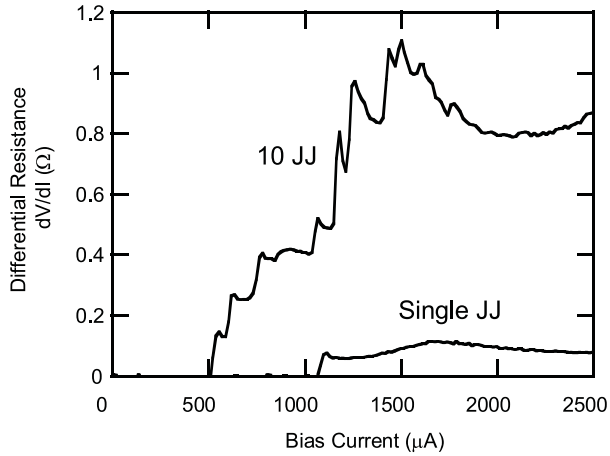

Figure 5. Differential resistance measurement for a 10 junction array (0.6 μm spacing) and a single junction (below) at 4.2 K.

frequency [7]. An example of phase locking is shown in figure 4 (10-junction array, 1.6 μm spacing, 14.0 GHz, 6.0 K—the first step appears at 0.28 mV). Table 1 shows parameters for arrays of spacing 0.2–1.6 μm. The locking temperature given is the lowest at which a convincing $\times 10$ step was observed. In general this temperature is lower when the junction spacing is shorter, suggesting a penetration depth-dependent electromagnetic coupling mechanism [8]. The exception is the 0.6 μm spacing array, in which no locking was observed. It should be noted, however, that this array also had an anomalously large I_C spread ($\delta I_C = 2.7$).

Low noise differential resistance measurements as a function of bias current ($\mathrm{d}V(I)/\mathrm{d}I$) were made with the aid of a lock-in amplifier. This allowed the switching of individual junctions in an array to be observed. Figure 5 shows the $\mathrm{d}V(I)/\mathrm{d}I$ characteristic of an array and a single junction at 4.2 K. From the deduced I_C distribution (statistics shown in table 1), the I–V characteristic of an array can be convincingly reconstructed by scaling the I–V characteristic of a single junction and summing. Significantly this best fit is obtained by scaling the single junction I–V characteristic assuming constant R_N (rather than constant $I_C R_N$). In these devices, when the milled trench does not penetrate the Cu layer, R_N is effectively constant (Cu has a resistivity a factor of 10 lower than that of Nb in the normal state).

A low-noise measurement of an array under microwave irradiation reveals structure in addition to the Shapiro-like step (see figure 4 inset). This may arise due to the non-ideal characteristics sometimes observed in individual junctions. The single junction differential resistance profile shown in figure 5 is clearly not ideally RSJ-like, with a bump at $\sim 1.5 \times I_C$ (common in SNS junctions with long diffusive barriers [9, 10]). Furthermore, such junctions display fractional Shapiro steps under microwave irradiation. The addition of a superconducting ground plane should lead to a more uniform current distribution throughout the array and may counter such effects.

4. Discussion

In an SNS junction I_C depends exponentially on the barrier width, so even small variations in the width of the FIB-milled trenches will translate to large variations in I_C. For this reason directly-written junctions will always have larger I_C spreads than sandwich or ramp-type structures, where the barrier thickness can be controlled on the order of angstroms by the deposition process. Beam fluctuations have been eliminated as a source of error by milling all the junctions in the array in parallel, but to little avail. Repeated measurements of the arrays over a period of weeks showed no noticeable drift in properties, suggesting that the migration of implanted Ga is not an issue. The fundamental cause of the I_C variation may be the polycrystalline microstructure of the films leading to an uneven milling rate and hence uneven trench width and depth. Hence to achieve a significant improvement in parameter spreads it would be necessary to use truly epitaxial films (the current films are polycrystalline [4]).

It seems that locking is achieved in these arrays in spite of the appreciable spread in I_C because the spread in R_N is so small, due to the shunting effect of the unbroken Cu layer. This is in accordance with the analysis of Borovitskii *et al* [11]. Indeed, external resistive shunts have been deliberately added to arrays of high-temperature superconductor junctions to achieve precisely this effect, with encouraging results [12, 13].

For a 10 V programmable voltage standard system it is estimated that ∼10 000 junctions at ∼100 nm spacing would be required [2]. For array fabrication on this scale a direct-writing technique such as this would be extremely time consuming, even if sufficient uniformity could be achieved (e.g. with the aid of state-of-the-art autofocusing in the FIB). An indirect method of patterning (anisotropic etch with a mask and etch-stop layer) may be required.

5. Conclusions

We have applied our existing nanoscale junction technology to the fabrication of series arrays. At 4.2 K the spread in I_C, $\delta I_C = I_{Cmax}/I_{Cmin} \sim 1.5$. R_N is determined by the shunting Cu layer thickness. The spread in R_N is hence small, allowing phase locking in spite of the significant spread in I_C. Locking behaviour is observed at elevated temperatures. For arrays of comparable spreads in I_C, the temperature at which locking first occurs is lower when the junction spacing is shorter, suggesting a penetration depth-dependent electromagnetic coupling mechanism.

Acknowledgments

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