Failure Dynamics of the IGBT During Turn-Off for Unclamped Inductive Loading Conditions

Chih-Chieh Shen, Allen R. Hefner, Jr., *Senior Member, IEEE*, David W. Berning, and Joseph B. Bernstein, *Member, IEEE*

***Abstract*—The internal failure dynamics of the insulated gate bipolar transistor (IGBT) for unclamped inductive switching (UIS) conditions are studied using simulations and measurements. The UIS measurements are made using a unique, automated nondestructive reverse-bias safe operation area test system. Simulations are performed with an advanced IGBT circuit simulator model for UIS conditions to predict the mechanisms and conditions for failure. It is shown that the conditions for UIS failure and the shape of the anode voltage avalanche-sustaining waveforms during turn-off vary with the IGBT temperature, and turn-off current level. Evidence of single- and multiple-filament formation is presented and supported with both measurements and simulations.**

***Index Terms*—Avalanche, current constriction, failure, filament, insulated gate bipolar transistor, modeling , nondestructive testing, reverse-bias safe operation area.**

I. Introduction

INSULATED gate bipolar transistors (IGBT's), having the unique advantages of bipolar conduction characteristics and insulated gate control, have received much attention in recent years for their energy-efficient and rugged performance for a wide range of power applications. These devices are frequently employed in hard-switching applications, where the device is required to turn off high currents under inductive loading conditions. Ruggedness of devices used in such applications is a desirable feature, and a premium is placed on these devices having a large reverse-bias safe operation area (RBSOA). Although RBSOA characteristics of the IGBT do not severely limit the capability of the device in most clamped applications, inductive spikes can cause the device to avalanche and possibly fail. An understanding of the failure mechanisms of IGBT's can surely benefit future IGBT designs.

Historically, hard switching was performed with bipolar transistors which have severe limitations on their RBSOA. RBSOA failure occurs because dynamic switching conditions result in current constriction leading to excessive current density in a small region of the device. The excessive current density results in device failure characterized by a rapid collapse of collector blocking voltage. Typically, the device is destroyed within nanoseconds after the voltage collapse. Many studies have been done both to characterize and to understand the mechanisms of bipolar transistor RBSOA failure [1]–[9], because of its importance in bipolar transistor power switching applications.

As power MOSFET's devices emerged, it was thought that the devices would be immune from the RBSOA restrictions of the bipolars. However, due to the internal parasitic bipolar of the power MOSFET structure, some RBSOA limitations persisted with the earlier power MOSFET devices [10]. Further development of the power MOSFET has eliminated the restrictions of the earlier devices and resulted in the unclamped inductive switching (UIS) energy rated devices which provide enhanced reliability and offer certain circuit design advantages. These UIS rated devices will withstand avalanche conditions at full current until the active area of the silicon chip is uniformly heated to the failure temperature.

The IGBT contains both bipolar and MOSFET elements and could be expected to exhibit RBSOA characteristics originating from both devices. However, the low-gain wide-base bipolar structure within the IGBT is quite different from that of the conventional power bipolar transistor, leading to much less severe limitations on the RBSOA performance than in the discrete bipolar transistor. Although the RBSOA characteristics of the IGBT are adequate for most switching applications, the bipolar structure imposes RBSOA capabilities far short of the UIS energy rated power MOSFET. Further improvements in RBSOA capability in IGBT's could lead to reliability improvements and circuit design advantages now enjoyed by power MOSFET's. For example, fast IGBT turn-off at high current results in high di/dt that causes a voltage spike resulting from parasitic inductance in the anode circuit. This can subject the IGBT to overvoltage stress similar to that encountered in the unclamped RBSOA measurement.

In this paper, RBSOA measurements have been made on IGBT's using the nondestructive RBSOA tester and automatic test controlling system developed at the National Institute of Standards and Technology (NIST), Gaithersburg, MD [8]. The UIS tests were performed for a range of currents, temperatures,

Paper IPCSD 99–74, presented at the 1998 Industry Applications Society Annual Meeting, St. Louis, MO, October 12–16, and approved for publication in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS by the Power Electronics Devices and Components Committee of the IEEE Industry Applications Society. Manuscript submitted for review October 15, 1998 and released for publication November 5, 1999. This work was supported in part by the National Institute of Standards and Technology Office of Microelectronics Programs and by the Office of Naval Research Power Electronic Building Block Program under Grant N000149710824.

C.-C. Shen was with the Center for Microelectronics Reliability, University of Maryland, College Park, MD 20742 USA. He is now with the Advanced Process Technology Department, Conexant Systems Inc., Newport Beach, CA 92660 USA (e-mail: bruce.shen@conexant.com).

A. R. Hefner, Jr., and D. W. Berning are with the Semiconductor Electronics Division, National Institute of Standards and Technology, Gaithersburg, MD 20899-8120 USA (e-mail: hefner@nist.gov; berning@nist.gov).

J. B. Bernstein is with the Center for Microelectronics Reliability, University of Maryland, College Park, MD 20742-2115 USA (e-mail: joey@glue.umd.edu).

Publisher Item Identifier S 0093-9994(00)02396-3.

0093–9994/00$10.00 © 2000 IEEE

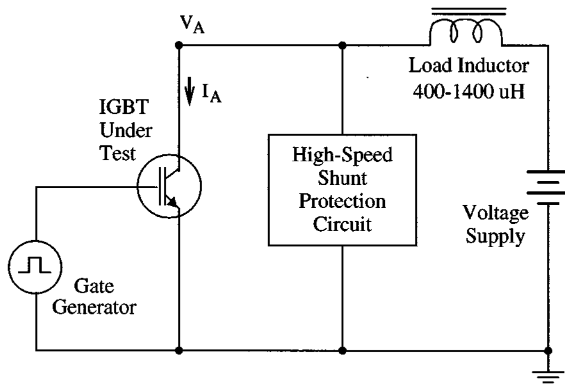


Fig. 1. Simplified schematic of the nondestructive RBSOA tester.

load inductor values, and device types. The expermental results are compared with simulations of the UIS condition performed using the NIST IGBT model [11] with modifications for high-temperature physics and multiple-filament formation. The model describes experimentally observed trends in current and voltage waveforms and failure conditions versus turn-off current and temperature.

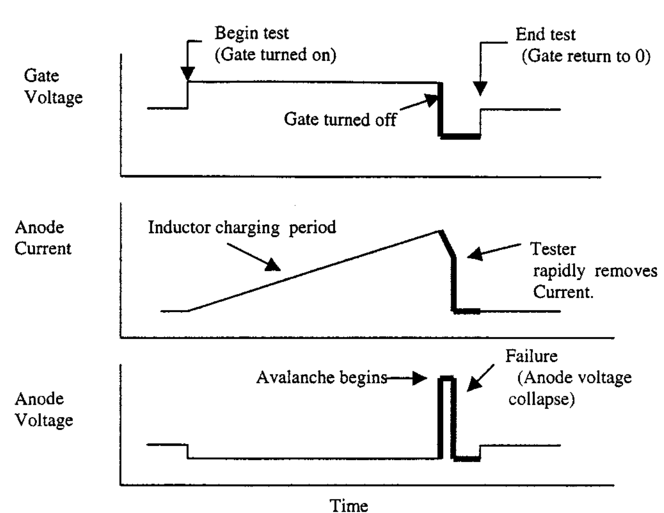
II. Nondestructive RBSOA Measurement

The NIST nondestructive test system is used to stress the device near to and beyond the normal limits of failure. This system permits repeated and extensive measurements to be made on single devices for conditions which would normally cause the device to be destroyed. Fig. 1 is a simplified schematic of the nondestructive RBSOA testing circuit used in this work. Conceptually, the circuit consists of the IGBT (device under test), a load inductor in the anode circuit, a voltage power supply to charge the inductor, and a pulse voltage source for the IGBT gate. The high-speed shunt protection circuit in the NIST RBSOA tester is a sophisticated vacuum tube-based circuit with a 2000-V 100-A capability. The high-speed shunt protection circuit detects the voltage collapse at the onset of RBSOA failure and diverts the inductor current away from the device within 30 ns, thus preventing the device from being destroyed and enabling repeated failure tests to be performed on a single device.

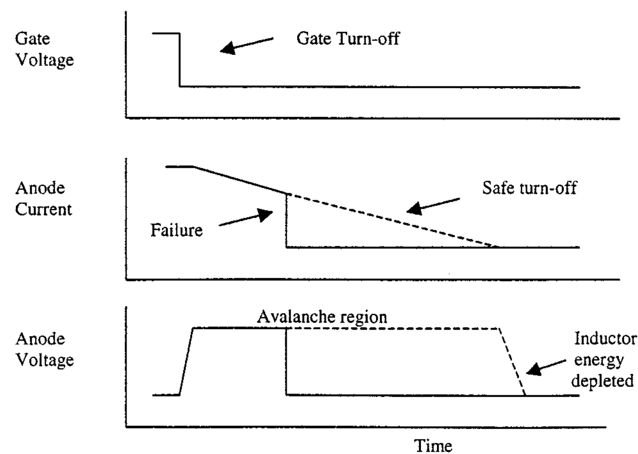
A. UIS Failure Characteristics

Fig. 2(a) shows idealized waveforms for the RBSOA test, displaying gate voltage, anode current, and anode voltage waveforms. The test is initiated when the IGBT gate voltage is turned on, causing the anode current to ramp up as the inductor is charged by the inductor voltage supply. At the point in time when the inductor current reaches the desired test value, the IGBT gate voltage is switched off, initiating the RBSOA turn-off event. The RBSOA measurements are made between the time the gate voltage is switched off and the time when the protection circuit is fired. This region of the waveform is indicated by the intensified portion of Fig. 2(a) and is expanded in Fig. 2(b).

When the gate voltage is turned off [Fig. 2(b)], the anode voltage is driven to a high value by the inductor as the IGBT



(a)



(b)

Fig. 2. (a) Idealized RBSOA waveforms for entire testing cycle. (b) Expanded turn-off portion of RBSOA waveforms [intensified region of (a)].

attempts to interrupt current. Because the anode voltage is not externally clamped, the IGBT experiences avalanche-sustaining voltage breakdown. For most of the results shown in this paper, the IGBT avalanches for a period of time before it actually fails. It should be noted, however, that at high currents and high temperatures, the device can fail before the voltage reaches the avalanche-sustaining voltage. In either case, the protection circuit fires when failure is detected and successfully prevents destruction of the device. Additionally, at low currents, the device can successfully sustain the voltage for the full time necessary to discharge the inductor without failing [shown by the dashed lines in Fig. 2(b)].

The important characteristics of the unclamped inductive switching event are the RBSOA curve which consists of the voltage at failure for each test current and is included in most power device data sheets. This was particularly important for bipolar transistors where the failure voltage could be reduced by 50% of the dc blocking capability of the device. This placed severe limitations on the maximum clamp voltage that could be

used for switching. Power MOSFET's typically avalanche at the dc blocking voltage for a period of time before failing. For MOSFET's, the UIS event is better characterized by sustaining time or energy dissipated during the sustaining time. UIS energy rated power MOSFET's typically are characterized by a single maximum sustaining energy value. IGBT UIS failures can either occur during the anode voltage rise before reaching a voltage sustaining condition or after sustaining for a period of time at a voltage that is lower than the dc blocking capability. Thus, IGBTs are characterized in this study using both RBSOA and sustaining energy curves.

B. Automated Failure Analysis System

The NIST RBSOA tester is an IEEE488 bus-controllable instrument and, in this work, it was interfaced to a computer using LabWindows/CVI.[1] The highly automated user interface enables the collection and analysis of many IGBT failure conditions. This capability was used in this study to analyze the voltage and current sustaining waveforms, failure energies, and sustaining times for various currents, temperatures, device types, and load inductor values. The program controls and takes data from the RBSOA tester, a Tektronix TDS644 digitizing oscilloscope, and a temperature controller. The program sends the test current and anode clamp voltage values to the RBSOA tester and then initiates a test. Upon completion of each test, the program retrieves the failure status from the RBSOA tester and the anode current and voltage waveforms from the TDS644 digitizing oscilloscope for subsequent analysis.

Fig. 3 shows an example of the computer screen user-interface panels, setup options, and typical types of data that can be obtained and displayed. Fig. 3(a) shows the computer screen user-interface panel that is used for running a series of RBSOA tests on a single device in a sequential automated fashion. On this panel, the user specifies the current ranges and the number of current steps that are to be used for tests, the method of testing (either clamped or unclamped peak voltage), the clamp voltage ranges and the number of clamp voltage steps if the clamp voltage method is used, and the test temperature. The unclamped method was used for all of the measurements performed in this study. For this method, the clamp voltage is set to its maximum value of 2000 V, and the RBSOA voltage is calculated by the program as the maximum value of the voltage waveform measured by the TDS644 digitizing oscilloscope. The test temperature specified on the user interface panel is sent to the temperature controller which regulates the temperature of the temperature controlled test fixture upon which the IGBT is mounted. The instantaneous value of the test fixture temperature is also displayed to allow the user to wait until the set temperature is reached before performing a test.

The graphs on the right side of Fig. 3(a) display the measured data as the series of RBSOA measurements are performed. The upper graph shows the actual voltage–current data points as they are collected. The data points plotted are designated by "S" for safe turn-off, and "F" for failure. If during an RBSOA test, the IGBT avalanches until all of the energy stored in the inductor is transferred to the IGBT without the device failing, the peak avalanche-sustaining voltage is, thus, labeled "S" for the given test current. Otherwise, if the IGBT anode voltage collapses before the current in the inductor goes to zero and the protection circuit fires, the RBSOA tester failure status bit is set indicating to the program that a failure has occurred, and the data point is labeled with an "F." The lower graph of Fig. 3(a) shows the calculated energy absorbed by the IGBT for each test as described below. Throughout this study, the measured sustaining voltage and energy at a given current were repeatable to within one 1%.

Fig. 3(b) shows the computer screen user-interface subpanel for reviewing the measured voltage, current, and power waveforms. The controls on the lower left-hand side of Fig. 3(b) enable the display of the waveforms associated with each of the test points in Fig. 3(a). The graph in the upper right-hand side of Fig. 3(b) shows the voltage waveforms for the selected test points, and the graph in the lower right-hand side shows the current waveforms. Note that, once the IGBT voltage collapses, the tester diverts the inductor current away from the device, and no more energy is dissipated in the device. The power versus time shown in the upper left-hand side of Fig. 3(b) is calculated by multiplying the voltage and current waveform. The asterisk on each curve indicates the position determined by the program as the onset of failure. This failure time is determined using the derivative of the waveform including filtering of noise. The energy for each test shown on Fig. 3(a) is calculated by performing the integral of the power waveforms between the time when the anode voltage begins to rise and the time when the onset of failure occurs.

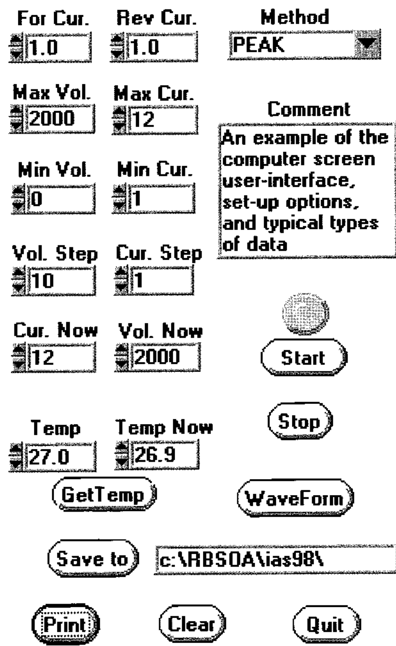
III. MODELING IGBT UIS FAILURE

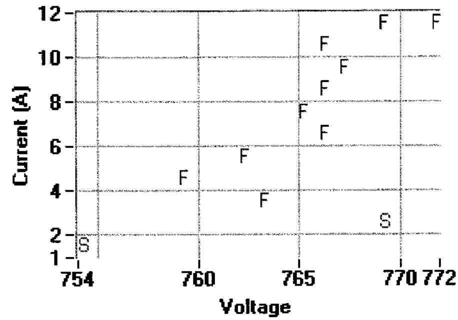
In this study, the previously developed electro-thermal IGBT model [11]–[13] is combined with an equivalent circuit for the RBSOA test system to simulate the UIS condition. This model is a general-purpose compact analytical model that includes all of the physics necessary to describe the steady-state and transient operation of the IGBT, including the dynamic avalanche-sustaining conditions. The model was modified in this study to include the high-temperature intrinsic conduction of the base region and to include multiple diffusion length sized filaments in parallel with the main device. The Saber[2] circuit simulator is used because of the ease of making the model modifications necessary for the high-temperature operation using the MAST modeling language.

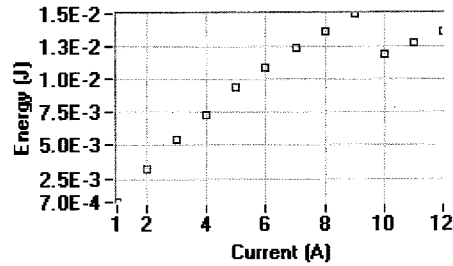
In this section, the key equations describing the temperature and current dependence of the IGBT avalanche sustaining voltage are given, and the basic mechanism for IGBT RBSOA failure is described. The inclusion of multiple filaments in parallel with the main device enables the predictions of the effects of current constriction during avalanche-sustaining conditions. The inclusion of the high-temperature intrinsic conduction mechanism is necessary to predict the voltage collapse at

[1]LabWindow/CVI, National Instruments Corporation, Austin, TX. Certain commercial software products and electronic instruments are identified in this paper in order to specify the experimental procedure adequately. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that these products are the best available products for the purpose.

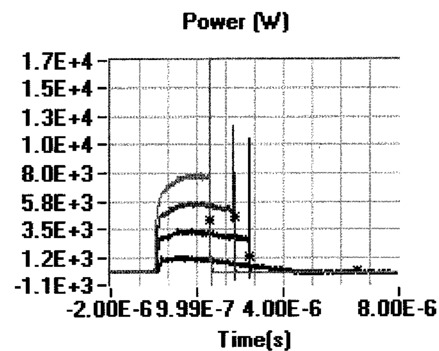
[2]Saber and MAST are trademarks of Analogy Inc., Beaverton, OR.

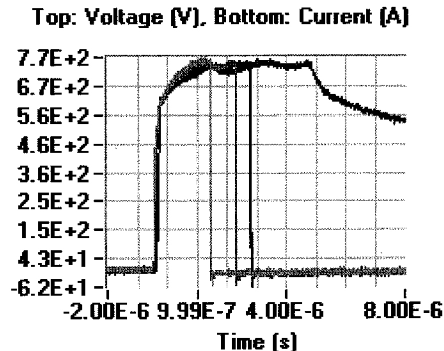


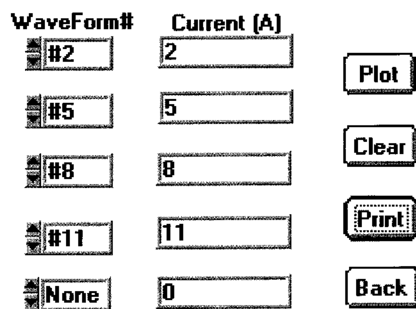


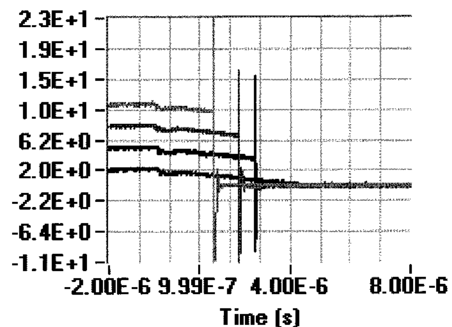


(a)









(b)

Fig. 3. (a) Example computer screen user–interface panel consisting of current and voltage range specification, RBSOA test data (upper graph), and absorbed energy (J) versus current test data (lower graph). (b) Example computer screen user–interface subpanel consisting of the measured voltage waveforms (upper right-hand graph), current (A) waveforms (lower right-hand graph), and power (W) waveforms (upper left-hand graph).

failure when the filament reaches the intrinsic temperature in the base region. In Section IV, it is shown that these modifications are necessary to describe the avalanche-sustaining voltage waveforms during current filament formation and to predict the conditions that will result in failure based upon the test current, device case temperature, and load inductance.

A. Avalanche-Sustaining Voltage

The avalanche breakdown voltage of the IGBT is determined by the open-base, collector–emitter breakdown voltage of the bipolar transistor (BV_{ceo}). The BV_{ceo} is reached when the product of the carrier multiplication factor M and the common base current gain α is unity [14]

$$\alpha \cdot M = 1. \tag{1}$$

An empirical expression for M in terms of the base–collector junction voltage (V_{bc}) is widely used in the literature [15] for a one-sided step junction. A closed-form analytical expression for the multiplication factor that includes the effects of reach-through to the buffer layer was introduced in [11] and is used in the IGBT model

$$M = 1/[1 - (V_{nrt}/BV_{cbo})^{BV_n}] \tag{2}$$

where V_{nrt} is given in terms of V_{bc} [12, eq. (38)], and accounts for the depletion region shape including the reach-through effect. The collector–base breakdown voltage for a one-sided abrupt step junction is given by [13], [15]

$$BV_{cbo} = BV_f \cdot 5.34 \times 10^{13} \cdot \left(\frac{T_j}{300}\right)^{0.35} \cdot N_{scl}^{-0.75} \tag{3}$$

where N_{scl} is the collector–base junction space-charge density, BV_f is the avalanche uniformity factor, and T_j is the junction temperature. The temperature dependence of (3) is due to the the reduction of the impact ionization coefficients with temperature. The saturated limited velocity in the collector–base depletion region results in an additional component of space charge in the depletion region

$$N_{scl} = \frac{J_f}{qv_{p\text{sat}}} + N_B \tag{4}$$

where J_f is the total filament current density, N_B is the base dopant density, and $v_{p\text{sat}}$ is saturation velocity for holes.

There are several key factors related to the temperature and current dependence of the avalanche-sustaining voltage.

1) The avalanche voltage of (3) increases with temperature due to the decrease in impact ionization coefficient with temperature.
2) The collector–base space-charge density of (4) increases with current density, thus decreasing the avalanche-sustaining voltage through (3).
3) The bipolar transistor current gain α increases with temperature due to the increase in lifetime with temperature:

$$\tau_{HL}(T_j) = \tau_{HL0} \cdot \left(\frac{T}{300}\right)^{3.0} \tag{5}$$

where τ_{HL0} is the high-level lifetime at the reference temperature of 300 K. The increasing α results in a lower M at breakdown according to (1) and, thus, a lower breakdown voltage according to (2).
4) The current gain α also decreases with increasing current density due to emitter efficiency reduction and, thus, the avalanche voltage increases with current according to (1) and (2). The current and temperature dependence of avalanche voltage determine the failure mechanism and safe sustaining time for the IGBT.

B. Second Breakdown Mechanism

Because the breakdown voltage decreases with increasing current due to the collector–base junction space-charge density, a positive feedback mechanism can exist during avalanche conditions which results in current constriction and filament formation. That is, as the current density increases in one region of the IGBT chip, the breakdown voltage of that region is lowered, resulting in a further increase in current density in that region. This constriction continues until the area of the high current density region reaches the minimum area of a stable current filament. The minimum area of a stable current filament is determined by the diffusion length in the base region, because the carriers that are generated in the collector–base depletion region by avalanche multiplication must diffuse the entire length of the base region in order to produce collector current and form a regenerative process. The minimum area of the current filament can also stablize because the current gain decreases with increasing current density.

After the formation of the current filament, the filament temperature increases rapidly due to self-heating until the filament temperature reaches the intrinsic temperature of the base region (485 K for the low doping concentration 2×10^{14}/cm^3 in the base region) [16]. When the intrinsic temperature is reached, the base region begins to conduct because the thermally generated carrier density n_i becomes much larger than the base dopant density. As a result, a rapid collapse in voltage across the device occurs, defined as a second breakdown failure event. It should be noted that, as this intrinsic conduction mechanism begins to dominate over the avalanche-sustaining mechanism, the filament is no longer limited to a minimum size as it is for the avalanche sustaining mechanism. As a result, the filament constricts, which further increases the voltage collapse rate. This filament constriction occurs during the intrinsic conduction mode because the intrinsic conduction current is a direct result of the local temperature and the heat cannot diffuse as fast as the heat is generated (adiabatic heating). Conversely, for the avalanche-sustaining mode, the current is a result of excess carriers that can diffuse as they are generated and, thus, a stable filament can form.

In this study, the IGBT model was modified to include the high-temperature effect of intrinsic conduction. To do this, the equilibrium majority carrier concentration in the base (represented in the model by N_B) is replaced by the expression including the thermally generated carrier concentration

$$N_{Bi} = \frac{1}{2}(N_B + \sqrt{N_B^2 + 4n_i^2}). \tag{6}$$

This equation implies that, for low temperatures, the equilibrium majority carrier concentration is equal to the base dopant density N_B, but at high temperatures, it becomes dominated by the intrinsic carrier concentration n_i that increases rapidly with temperature. This effect reduces the majority carrier base resistance, depletion width, and avalanche voltage in the IGBT

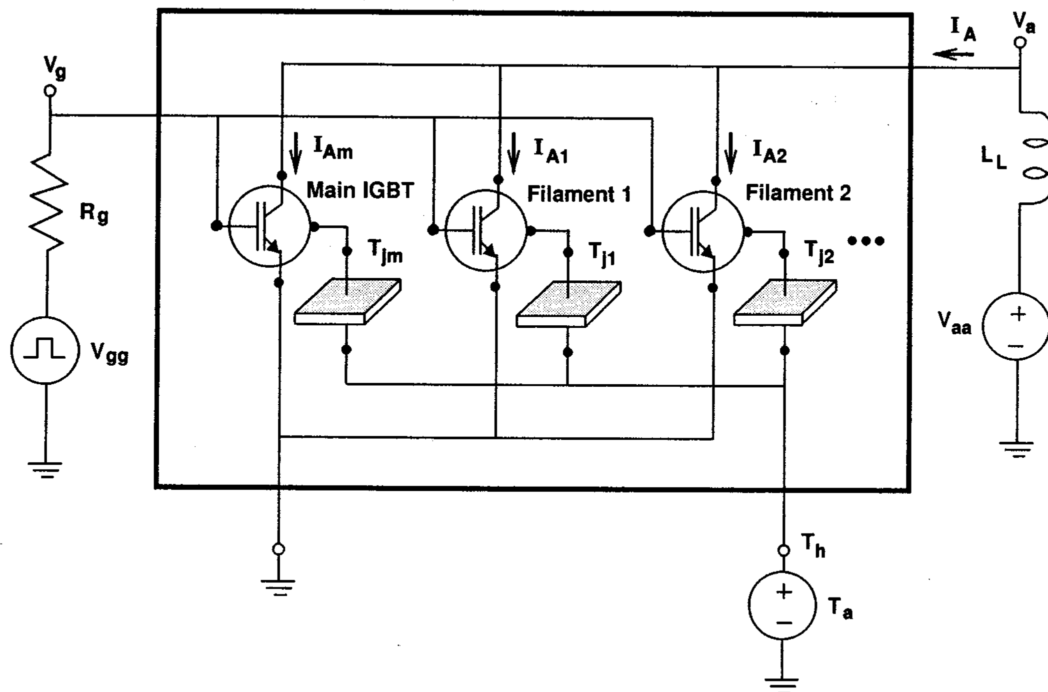


Fig. 4. Equivalent circuit used to simulate the IGBT UIS failure consisting of current constriction IGBT model (components within box) and equivalent circuit for RBSOA tester (components outside of box).

model. In addition, the minority carrier resistance of the base becomes small as the region becomes intrinsic

$$R_{\text{int}} = \frac{W_B}{q \cdot A \cdot u_p} \cdot \frac{N_B}{n_i^2} \tag{7}$$

where W_B is metallurgical base width, u_p is hole mobility, and A is the active area. This intrinsic resistance is of the same carrier type as the emitter and collector regions and, thus, forms a shunt resistance that directly connects the IGBT anode to cathode. The addition of these intrinsic conduction effects results in a latching mechanism when the critical intrinsic temperature is reached, enabling the prediction of conditions that will result in failure.

C. Circuit Simulation Model

The equivalent circuit used to simulate the IGBT UIS failure condition is shown in Fig. 4. The circuit consists of an equivalent circuit for the IGBT indicated by the components within the box and an equivalent circuit for the RBSOA tester indicated by the components outside of the box. The equivalent circuit for the tester consists of the load inductor L_L, the load supply voltage V_{aa}, the gate pulse generator V_{gg}, and the drive impedance of the gate pulse generator R_g. The protection crowbar circuit is not represented in the simulations because the intent of the study is to simulate the conditions that lead to failure and the failure event for the IGBT device. The purpose of the crowbar in the measurement circuit is to prevent destruction of the IGBT after failure has already occurred, thus enabling the device to be tested for multiple failure conditions.

The equivalent circuit for the IGBT, indicated by the components within the solid box in Fig. 4, consists of the main IGBT in parallel with several filament-sized IBGT's, each having a corresponding thermal model for the silicon chip. For most of the paper, only one filament is used except in Section IV. For the simulations, each IGBT component is represented by the physics-based, electro-thermal IGBT model which contains all of the physical mechanisms described above. In addition, each of the silicon chip segments are represented using the silicon chip thermal component model including the heat-source thickness effect described in [17]. It is important to include the heat-source thickness effect because the heat does not diffuse during the RBSOA event (adiabatic heating). Although the model includes both diffusion and heat-source thickness effects, the heat thickness is most important because the heat only diffuses a few micrometers beyond the 50-μm heat-source thickness for the few microsecond avalanche conditions. In addition, the chip thermal models are not laterally coupled between filaments because the typical filament width is 100 μm and the heat only diffuses a few micrometers.

The model parameters of the IGBT's and chip thermal models are obtained using the IGBT extraction process similarly to that described in [11]–[13] except that the area of the IGBT chip is divided between the area of the filaments and the area of the main IGBT. To initiate the current constriction process, a nonuniformity is introduced between the parameters of the main IGBT and those of the filaments. In order to do this, the avalanche uniformity factor (BV_f) is made to be 2% smaller in the filaments than in the main device. This value is large enouth to initiate the filament formation process and the results of this study are insentive to this value.

As described in Section III-B, the minimum area for a stable filament is determined by the diffusion length in the IGBT base.

A limitation of the lumped representation for the filaments is that the area of the filament must remain constant during simulations. Because the current density and avalanche voltage are determined by the IGBT filament area, an effective filament area is used by the model to represent the filament formation process. The effective area is larger than the minimum area determined by the diffusion length. Furthermore, because the filament chip thermal model area determines the rate of temperature rise and transition to intrinsic temperature conduction, the effective chip thermal model area is used to represent the process of further filament constriction after the base region reaches the intrinsic temperature. This effective chip thermal model area is smaller than the stable filament IGBT model area. In this study, the area of the filament chip thermal model is chosen to be one-third of the area of the filament IGBT model.

Several approximations are made in using the equivant circuit of Fig. 4 to model the current constriction process. As described above, the filaments are represented with a lumped IGBT and thermal model with constant area. The IGBT components also neglect the lateral coupling of current between filaments due to the difficulty of modifying the IGBT model to include lateral current flow. As a consequence of these approximations, the model can not duplicate the exact shape of the measured failure waveforms, but it does predict the mechanisms and conditions for failure and describes the trends in temperature and current dependance of failure conditions. In order to improve the ability of the IGBT model to better predict the actual shape of the failure waveforms, a much more complex IGBT model would have to be developed that includes lateral current flow and dynamically changing active area.

IV. Simulated and Measured Results

In this section, the model developed in Section III is used to explain the unclamped inductive load avalanche-sustaining voltage waveforms and the conditions that result in failure. It is shown using simulated results that the mechanisms discussed in Section III are responsible for the variations in the shape of the anode sustaining voltage waveforms for different test currents and external device case temperatures. The predictions of the model are supported with experimental data for both the anode voltage waveform shape and failure times. Finally, evidence of multiple filament formation is given, indicating that the failure time is extended when current is transferred from a heated filament to another area of the device.

A. Simulated Avalanche Sustaining Waveforms

The shape of the avalanche-sustaining voltage waveform can be described in terms of the basic physical mechanisms discussed in Section III. These include the dependence of avalanche voltage on current and temperature, and the transitioning of current from the main IGBT to the filament. When the IGBT is turned off for the UIS condition, the voltage rises to the point where avalanche breakdown occurs. The initial avalanche sustaining voltage is determined by the external device case temperature and the inductor current.

Several competing mechanisms determine the shape of the avalanche-sustaining voltage waveform as time progresses. The avalanche sustaining voltage tends to increase with time because: 1) increasing junction temperature increases BV_{cbo} and 2) decreasing inductor current reduces N_{scl}. Conversely, the avalanche sustaining voltage tends to decrease with time because: 1) self-heating increases lifetime and, thus, increases current gain; 2) the current density and, thus, N_{scl} increase during the process of current filament formation; and 3) decreasing inductor current increases current gain due to emitter efficiency.

For a given current and external case temperature test condition, a combination of the above five mechanisms determines the shape of the avalanche sustaining voltage waveform and the conditions for device failure. The device failure occurs when the temperature of a filament reaches the intrinsic temperature. Figs. 5–8 give example simulations demonstrating several of these mechanisms using the model descrived in Section III. Although the range of conditions where each mechanism dominates depends upon the device model parameters, the qualitative behavior given in Figs. 5–8 is typical for a high-speed buffer-layer-type IGBT.

Fig. 5 shows an example simulation of an avalanche-sustaining voltage waveform where the voltage decreases with time due to the transition of current to the filament. This mechanism tends to dominate the shape of the voltage waveform for higher device-case-temperature conditions. The voltage waveform in Fig. 5 begins to avalanche at approximately 800 V, but decreases with time as current is transferred to the filament. The total current is initially shared between the filament and the main IGBT. Because the filament has a 2% lower BV_f, the current slowly begins to be transferred to the filament. As the current density begins to rise in the filament, N_{scl} increases, resulting in a decreasing avalanche voltage (see (3)) of the filament and, thus, the decreasing terminal avalanche voltage. The decreased filament avalanche voltage increases the rate of transfer of current to the filament.

Fig. 6 shows an example simulation of an avalanche sustaining voltage waveform that increases with time due to the decreased N_{scl} as the inductor current falls. This mechanism tends to dominate the shape of the voltage waveform for lower device case temperature and lower test current conditions. The avalanche voltage waveform in Fig. 6 initially decreases with time ($t < 2\ \mu$s) due to the transition of current to the filament. After the initial decrease in voltage, the voltage waveform in Fig. 6 begins to increase because N_{scl} in the filament is reduced as the current density (J_f) is reduced due to the inductor load current decreasing. For the low test current condition of Fig. 6, the effects of self-heating are negligible because the temperature only rises about 30 °C in the filament.

Fig. 7 shows an example simulation of a sustaining voltage waveform that increases with time due to self-heating. This mechanism tends to dominate the shape of the voltage waveform for lower device case temperature and medium to high anode current conditions. After the initial decrease in voltage due to the transition of current to the filament, the voltage waveform in Fig. 6 begins to increase. For this medium test current condition, the self-heating effect increases the filament temperature about 110 °C in 6 μs. The increasing temperature increases the avalanche voltage through the temperature dependence of (3).

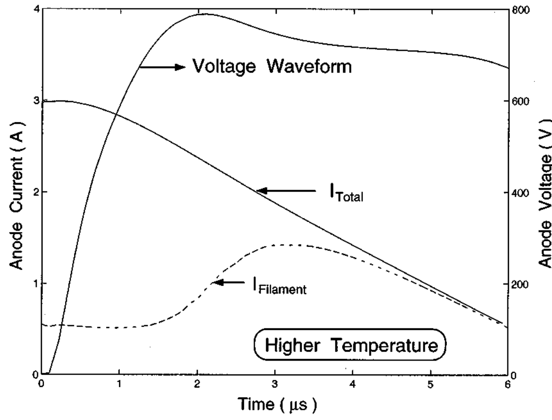


Fig. 5. Example simulation of an avalanche-sustaining voltage waveform that decreases with time due to the transition of current to the filament for high case temperature and lower test current conditions.

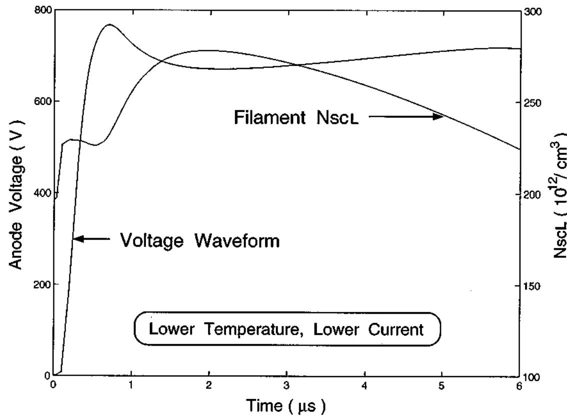


Fig. 6. Example simulation of an avalanche-sustaining voltage waveform that increases with time due to the decreased in collector–base space-charge density with decreasing inductor current for lower case temperature and lower test current conditions.

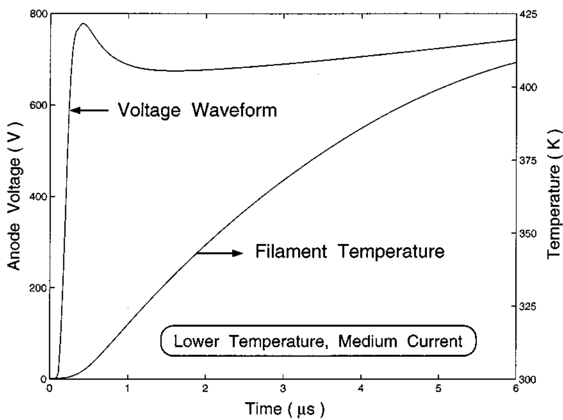


Fig. 7. Example simulation of an avalanche-sustaining voltage waveform that increases with time due to self-heating for low case temperature and medium test current conditions.

Fig. 8 shows an example simulation of the voltage waveform that collapses, signifying a failure event when the filament temperature reaches the intrinsic temperature. When the intrinsic temperature is reached, n_i become larger than N_B, resulting in conduction of current through the intrinsic resistance. It should be noted, that the active area of the entire IGBT's is sufficiently large that uniform power dissipations of several kilowatts for several microseconds (that is, the worst case temperature rise is given by $\Delta T = (P{\cdot}\Delta t/C_p{\cdot}\rho{\cdot}A{\cdot}W) = 10\,°\mathrm{C}, P = 3\,\mathrm{kw}$ is the power, $\Delta t = 3\,\mu\mathrm{s}$ is the sustaining time, $C_p = 0.7(\mathrm{Joule/g\text{-}°C})$ is the specific heat, $W = 50\,\mu\mathrm{m}$ is the heat source thickness, $\rho = 2.328\ (\mathrm{g/cm^3})$ is the density, and $A = 0.1\,\mathrm{cm^2}$ is the entire active area of the IGBT) would not cause enough self-heating to increase the avalanche voltage in Fig. 7 or cause failure in Fig. 8. Thus, filament formation is a key factor in determining the shape of the avalanche-sustaining voltage waveform and the failure time.

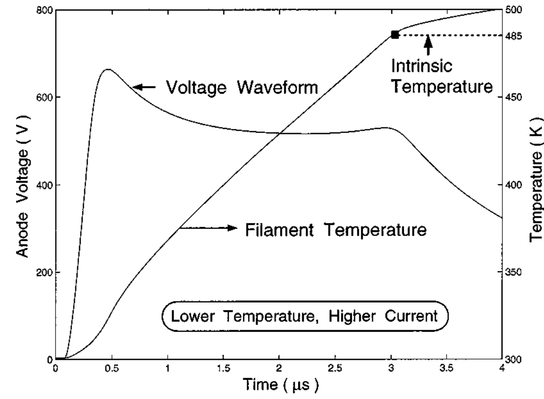
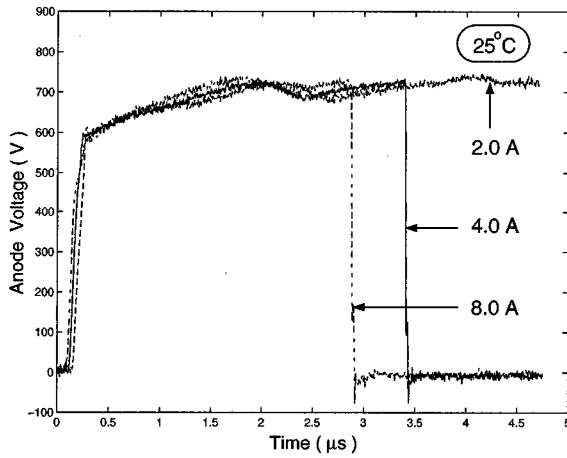


Fig. 8. Example simulation of an avalanche-sustaining voltage waveform that collapses, signifying a failure event when the filament temperature reaches the intrinsic temperature.

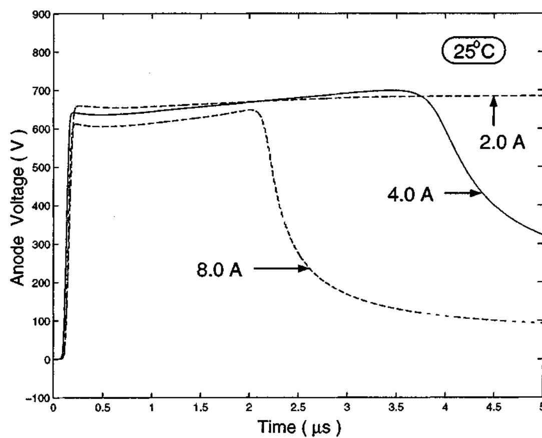
B. Validation of Current Constriction IGBT Model

RBSOA measurements were made on IGBT's for various values of test current, case temperature, inductor values, and device types. The voltage waveforms and failure times were repeatable to within 1%, and the devices could be successfully tested hundreds of times without detectable degradation due to the high-speed protection circuit. All of the trends observed in the voltage waveforms and failure times can be explained using the model described in Section III. Figs. 9 and 10 are example comparisons of simulated and measured UIS switching events for high and low temperature and over the current rating range of the device. The results indicate that the shape of the anode voltage waveform and the failure time can be described using the model.

Fig. 9 shows the simulated and measured UIS switching waveforms for a 25 °C case temperature. For the low-temperature and low-current conditions (25 °C, 2.0 A), the device is safely turned off without failure. This turn-off occurs beyond the 5-μs time shown in the figure. For the 4-A and 8-A cases, both the simulated and measured waveforms have a rapid voltage collapse, indicating a device failure. This occurs because the filament temperature reaches the intrinsic temperature. The voltage collapse after the intrinsic temperature is reached is more rapid in the measurement than in the simulation because the area of the filament can further constrict, whereas the area remains constant in the model.

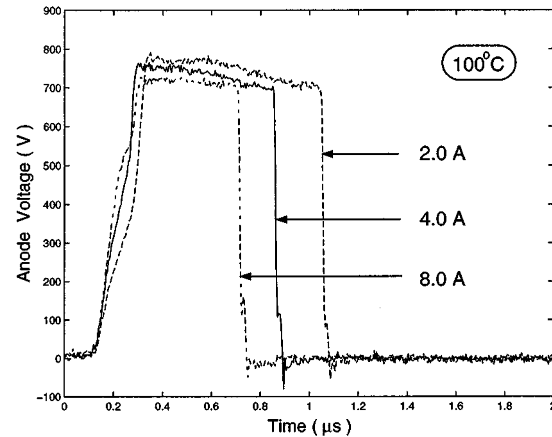


(a)

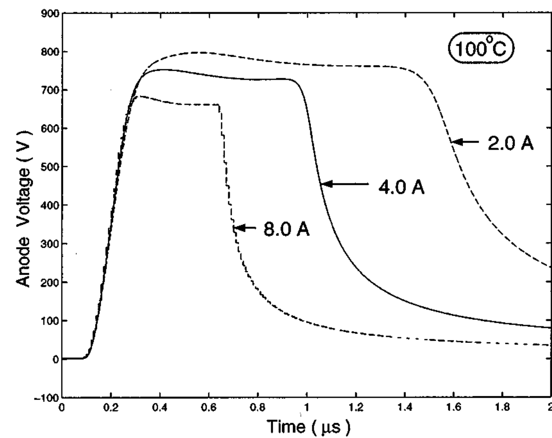


(b)

Fig. 9. (a) Measured and (b) simulated voltage waveforms for different turn-off currents at 25 °C.



(a)



(b)

Fig. 10. (a) Measured and (b) simulated voltage waveforms for different turn-off currents at 100 °C.

For the low IGBT case temperature of Fig. 9, the current filament takes a long time to form and, therefore, much of the voltage waveform is dominated by nearly uniform current flow. To best represent the filament size effect on the voltage waveform, the IGBT model filament area is chosen to be half of the device area. The area of the device shown in Figs. 9 and 10 is 0.08 cm^2.

From the comparisons between Fig. 9(a) and (b), the simulated avalanche voltage waveforms closely agree with the measured avalanche voltage waveforms except for the bump in the measured avalanche voltage waveforms. The bump is explained further in Section IV-C. In general, the avalanche voltage waveforms are influenced by all of the mechanisms discussed in the above Section IV-A. For the low test current condition and the device discussed in this study, though, the avalanche voltage of Fig. 9 increases with time because: 1) the reduced N_{scl} as the inductor load current decreases and 2) the increased breakdown voltage as the temperature rises.

Fig. 10 shows the simulated and measured UIS switching waveforms for a 100 °C IGBT-case-temperature test condition. For this condition (100 °C), the device fails for all of the currents from 2 through 8 A, whereas for the low-case-temperature condition of Fig. 9, the device did not fail for the low test currents of 2 A. In addition, the failure time is much shorter for the high-case-temperature condition than for the low-case-temperature condition. This shortened failure time occurs because the filament forms faster and because the filament temperature is already elevated by the external case temperature before the self-heating begins. For the 100 °C case, the IGBT model filament area is chosen to be closer to the stable filament area because the filament forms faster. The value of IGBT model filament area used for the simulations was 0.014 cm^2.

From the comparisons between Fig. 10(a) and (b), the simulated avalanche voltage waveforms closely agree with the measured avalanche voltage waveforms, but have contrasting features with the low-IGBT-case-temperature waveforms of Fig. 9. For the high-case-temperature waveforms of Fig. 10, the avalanche voltage starts out higher, then decreases as current falls for all of the different current levels. This occurs because the effect of the transition of current to the filament is dominant. This behavior is in contrast to the waveforms of Fig. 9 where the avalanche voltage increases with time.

The initial values of the avalanche voltages are higher for the high-case-temperature condition than for the low-case-temperature condition due to the temperature dependence of (3). In addition, the initial avalanche voltage decreases with increasing test current for the high-case-temperature condition, whereas the

initial avalanche voltage is less dependent on the test current for the low-case-temperature waveforms. The decreased avalanche voltage with test current is due to the effect of N_{scl} in (3) and (4). This effect is compensated for in the low-case-temperature waveforms by the decrease in current gain with increasing current, thus increasing the avalanche voltage according to (1).

C. Evidence of Multiple Filament Formation

The IGBT's tested showed evidence of multiple filament formation for many different test conditions. For example, Fig. 11 shows the sustaining voltage waveform as a function of time for various turn-off currents at 25 °C. The sustaining voltage waveform initially increases with time due to filament self-heating. When the filament avalanche voltage becomes larger than that of the unheated area, the current transfers to a second filament. The sustaining voltage waveform then drops rapidly as the current density is increased in the second filament, thus increasing N_{scl}. This voltage drop is followed by an increasing sustaining voltage due to self-heating of the second filament. This repeated rising and falling behavior of the avalanche-sustaining voltage waveform is also observed in simulations using multiple filaments.

As the turn-off current is increased from 8 to 9 A, as shown in Fig. 11, there is a discontinuous jump in the sustaining time before failure. The discontinuity in sustaining time occurs because the first filament is no longer heated after current is transferred to the second filament and additional time is required to heat the second filament to the intrinsic temperature. Fig. 12 shows the sustaining time (closely related to failure energy) versus test current, indicating the discontinuity in sustaining time due to the second filament formation. For the test currents higher than 9 A, the device fails before the formation of a second filament, whereas at lower currents, the sustaining time is longer because the current is transferred to the unheated filament.

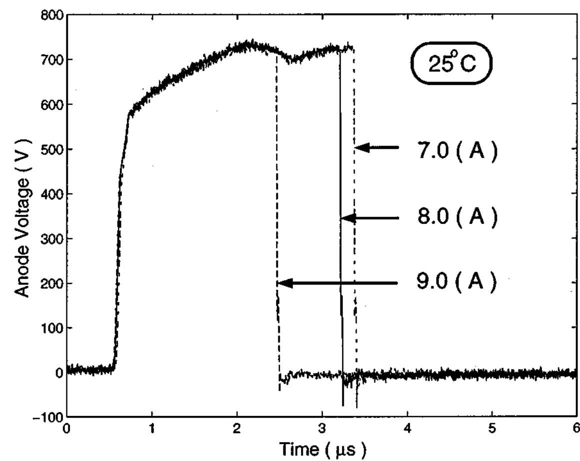


Fig. 11. Measured dynamic avalanche-sustaining voltage waveforms showing failure times, indicating formation of a second filament.

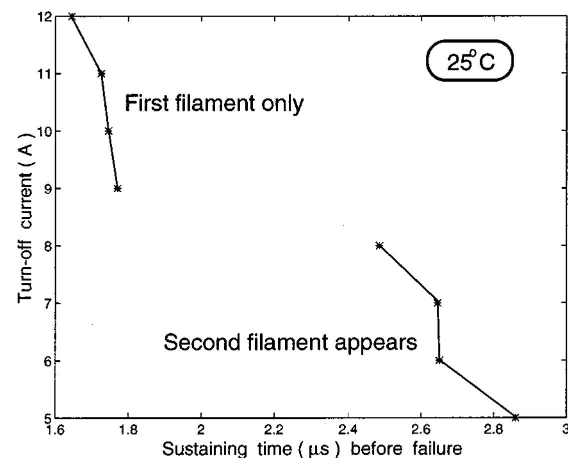


Fig. 12. Sustaining time versus turn-off currents indicating discontinuity in sustaining time due to multiple filament formation.

V. Conclusions

The NIST automated nondestructive RBSOA tester enables repeatable and extensive measurements to be made on power semiconductor devices, and is used to measure IGBT failure for unclamped inductive loading turn-off conditions. This RBSOA tester detects the onset of failure and diverts the current away from the device within 30 ns, thus preventing the device from being destroyed and enabling repeated failure tests to be performed on a single device. A highly automated user interface is presented for the IEEE–488 bus-controllable RBSOA test system enabling the collection and analysis of many IGBT failure conditions. Individual IGBT's can be tested hundreds of times with the RBSOA tester without observable degradation, and the measured failure characteristics are repeatable to within 1%.

For the first time, unclamped inductive loading measurements are analyzed using the NIST electro-thermal IGBT model to simulate the avalanche-sustaining voltage waveforms and conditions for failure. The IGBT model is modified to include the high-temperature intrinsic conduction of the base region and to include multiple diffusion length sized filaments in parallel with the main device. The inclusion of multiple filaments in parallel with the main device enables the predictions of the effects of current constriction during avalanche-sustaining conditions. The inclusion of the high-temperature intrinsic conduction mechanism is necessary to predict the voltage collapse at failure when the filament reaches the intrinsic temperature in the base region. The model describes experimentally observed trends in current and voltage waveforms and failure conditions versus turn-off current and temperature.

It is shown that the conditions for failure and the shape of the anode voltage avalanche sustaining waveforms during turn-off vary with the IGBT case temperature, turn-off current level, and load inductance. For given test conditions, a combination of various mechanisms determines the shape of the avalanche-sustaining voltage waveform and failure time. The detailed analysis of the physical mechanisms indicates that uniform power dissipation would not result in the measured avalanche voltage waveforms or failure times, thus indicating that filament formation is essential for describing the failure event. Furthermore, evidence of multiple-filament formation is given, indicating that the failure time is extended when current is transferred from a heated filament to another area of the device.

ACKNOWLEDGMENT

The authors wish to thank C. B. Tu for his assistance in software development and RBSOA measurements, and D. Blackburn for his helpful discussions.

REFERENCES

[1] P. L. Hower and V. G. K. Reddi, "Avalanche injection and second breakdown in transistors," *IEEE Trans. Electron Devices*, vol. 17, pp. 320–335, Apr. 1970.

[2] S. Krishna and P. L. Hower, "Second breakdown of transistors during inductive turn-off," in *Proc. IEEE*, vol. 61, Mar. 1973, pp. 393–395.

[3] B. A. Beatty, S. Krishna, and M. S. Adler, "Second breakdown in power transistors due to avalanche injection," *IEEE Trans. Electron Devices*, vol. 23, pp. 851–857, Aug. 1976.

[4] D. L. Blackburn and D. W. Berning, "Experimental study of re-verse-bias second breakdown," in *Tech. Dig. 1980 Int. Electron Devices Meeting*, 1980, pp. 297–301.

[5] D. Y. Chen, F. C. Lee, D. L. Blackburn, and D. W. Berning, "Reverse-bias second breakdown of high power Darlington transistors," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 19, pp. 840–847, Nov. 1983.

[6] T. M. Jahns, "Investigation of reverse-bias second breakdown in power transistors," M.S. thesis, Dep. Elect. Eng., Massachusetts Inst. Technol., Cambridge, May 1974.

[7] D. W. Berning, Semiconductor measurement technology: A reverse-bias safe operating area transistor tester, National Bureau of Standards Special Pub., pp. 400–454, Mar. 1979.

[8] ——, "Semiconductor measurement technology: A programmable reverse bias safe operation area transistor tester," NIST Special Pub., Aug. 1990.

[9] G. Busatto, L. Fratelli, and A. Patti, "Advanced RBSOA analysis for advanced power BJTs," *Microelectron. Reliab.*, vol. 36, no. 7/8, p. 1077, July 1996.

[10] D. L. Blackburn, "Failure mechanisms and nondestructive testing of power bipolar and MOS gated transistors," in *EPE-MADEP*, 1991, pp. 252–257.

[11] A. R. Hefner and D. M. Diebolt, "An experimentally verified IGBT model implemented in the saber circuit simulation," *IEEE Trans. Power Electron.*, vol. 9, pp. 532–542, Sept. 1994.

[12] A. R. Hefner, "Modeling buffer layer IGBT's for circuit simulation," *IEEE Trans. Power Electron.*, vol. 10, pp. 111–123, Mar. 1995.

[13] ——, "A dynamic electro-thermal model for the IGBT," *IEEE Trans. Ind. Applicat,*, vol. 30, pp. 394–405, Mar./Apr. 1994.

[14] A. R. Hefner and D. L. Blackburn, "A performance trade-off for the insulated gate bipolar transistor: Buffer layer versus base lifetime reduction," *IEEE Trans. Power Electron.*, vol. 2, pp. 194–207, July 1987.

[15] B. J. Baliga, *Power Semiconductor Devices*. Boston, MA: PWM, 1995, pp. 235–236.

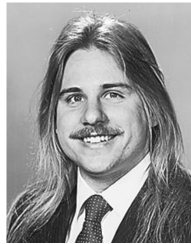
[16] S. M. Sze, *Physics of Semiconductor Devices, 2nd ed.*. New York: Wiley, 1981, pp. 20–21.

[17] A. R. Hefner and D. L. Blackburn, "Thermal component models for electrothermal network simulation," *IEEE Trans. Comp., Packag., Manufact. Technol. A*, vol. 17, pp. 413–424, Sept. 1994.

Chih-Chieh (Bruce) Shen received the B.S. degree in physics from Tamkang University, Taipei, Taiwan, R.O.C., the M.S. degree in physics from the University of Oregon, Eugene, and the M.S. degree in electrical engineering and the Ph.D. degree in electronic materials from the University of Maryland, College Park.

His research has concentrated on IGBT's, deep-submicrometer MOSFET's, and EEPROM device physics. He was affiliated with the Semiconductor Electronics Division, National Institute of Standards and Technology (NIST), where his Ph.D. dissertation led him to the area of power electronic devices. He also developed a novel flash EEPROM cell with improved reliability for which he has applied for a U.S. patent. He is currently with the Advanced Process Technology Department, Conexant Systems Inc., Newport Beach, CA.

Dr. Shen was the recipient of the C. Raymond Knight Award for excellence in reliability studies.



Allen R. Hefner, Jr. (S'84–M'84–SM'93) was born in Washington, DC, in 1959. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Maryland, Colege Park, in 1983, 1985, and 1987, respectively.

He joined the Semiconductor Electronics Division, National Institute of Standards and Technology (NIST), Gaithersburg, MD, in 1983. He is presently the Group Leader for the NIST Semiconductor Electronics Division's Device Technology Group and the Project Leader for the Metrology for Simulation and Computer Aided Design Project. He was also the NIST Research Advisory Committee member for the NIST Electronic and Electrical Engineering Laboratory (1997–1999). His research interests include characterization, modeling, and circuit utilization of power semiconductor devices. He is the author of 30 publications in IEEE TRANSACTIONS and conference proceedings.

Dr. Hefner was the recipient of an IEEE Industry Applications Society Prize Paper Award. He has presented 20 invited seminars and was an instructor for the IEEE Power Electronic Specialist Conference tutorial course (1991 and 1993) and for the IEEE Industry Applications Society Annual Meeting tutorial course (1994). He has served as a Program Committee Member for the IEEE Power Electronics Specialist Conference (1991–1999) and as the Transactions Review Chairman for the IEEE Industry Applications Society Power Electronics Devices and Components Committee (1989–1997). He has also served as the IEEE Electron Device Society Standards Technical Committee Chairman (1996–1999) and is a member of the IEEE Electron Devices Society Power Devices and Integrated Circuits Technical Committee. He is also the Founder and Chairman of the NIST/IEEE Working Group on Model Validation. He received a U.S. Department of Commerce Silver Medal Award in 1993 for his pioneering work in modeling advanced power semiconductor devices for electro-thermal circuit simulation. He is also the recipient of the 1996 NIST Applied Research Award for development and transfer of the IGBT model to circuit simulator software vendors.

David W. Berning was born in Cincinnati, OH, in 1951. He received the B.S. degree in physics from the University of Maryland, College Park, in 1973.

In 1974, he joined the National Institute of Standards and Technology, Gaithersburg, MD, where he has worked in the area of laser scanning of semiconductor devices. He is currently working on the development of test methods for measuring various parameters of power semiconductor devices. He also holds three U.S. patents concerning the design of audio electronics.

Joseph B. Bernstein (S'81–M'89) received the Ph.D. degree in electrical engineering from Massachusetts Institute of Technology, Cambridge, in 1990.

He is an Assistant Pofessor of Reliability Engineering in the Materials and Nuclear Engineering Department, University of Maryland, College Park, with appointments in Electrical Engineering and the Institute for Plasma Research. He is actively involved in several areas of microelectronics reliability research, including power device reliability, gate oxide integrity, radiation effects, MEMS, and metal interconnect. He supervises the laboratory for laser processing of microelectronic devices in the Materials and Nuclear Engineering Department. His research areas include studies of thermal, mechanical, and electrical interactions and failure mechanisms of dielectrics and power IGBT's, as well as laser processing for defect avoidance, programmable interconnect, and repair in microelectronic circuits and packaging.