AN ACTIVE HIGH VOLTAGE DIVIDER WITH 20-PPM UNCERTAINTY
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Abstract
A voltage divider has been designed which consists of a group of solid-dielectric capacitors maintained in a temperature-controlled environment, an external compressed-gas capacitor, and special electronic circuitry. The prototype divider has been constructed and preliminary results obtained to validate the operating principle and accuracy target. The principal innovative part is a feedback amplifier, complemented with an "open-loop" voltage source controlled from the high voltage. This enables achievement of a voltage ratio that is equal to the reciprocal of the capacitance ratio to well within one ppm without encountering dynamic instability problems.

Basic divider operating principle
Conceptually, the active divider comprises a high-voltage capacitor $C_1$ in series with a low-voltage capacitor $C_2$ in an elementary operational amplifier circuit, as described in [1]. This configuration ensures that the junction point voltage is near zero yielding the voltage ratio

$$\frac{V_2}{V_1} = \frac{C_1}{C_2} \left[ 1 + \frac{C_1 + C_2}{C_2} G \right]^{-1} = \frac{C_1}{C_2} (1 - 1/G). \quad (1)$$

Here $G$ is the open-loop gain of the amplifier and the typical component values encountered in this application are such that $G \gg 1$ and $C_2 \gg C_1$, which enable the simplification of Eq. (1). Theoretical and practical considerations impose an upper limit for the gain of amplifiers in closed-loop applications, which for typical general-purpose operational amplifiers at 60 Hz is 5000 to 10,000.

Methods to overcome this limitation in precise measurements have been invented and utilized. A method described in [1] uses the concept of a controlled voltage source, phase-locked to the input hv signal, that is inserted on an open-loop basis in the low-voltage arm of the divider to add to the amplifier output. If the voltage of the source is adjusted to the value

$$V_2 (C_1/C_2) (1 - d),$$

where $d$ is a small deviation from the desired value, the equation for the voltage ratio becomes

$$\frac{V_2}{V_1} = -(C_1/C_2) (1 - d/G). \quad (2)$$

It is relatively easy to obtain $d < 0.001$ and $G > 10^4$ and a relative difference between the ideal and actual ratios that is smaller than $10^{-6}$. The controlled source is implemented as a dual operational amplifier circuit.

The previous circuit of [1] requires two high-voltage capacitors which are available in some hv capacitor structures as dual low-voltage electrodes coupled to the same hv electrode. To accommodate most existing hv capacitors having a single low-voltage electrode, an alternative was developed as shown in Fig 1. The large-value, low-voltage capacitor $C_3$, is inserted in series with $C_1$ to act as a voltage-sensing impedance for the controlled source. In this circuit, the guard capacitance, $C_g$, becomes significant, causing the effective three-terminal capacitance, $C_1'$, of the hv arm of the divider to be

$$C_1' = C_1 \left[ 1 - (C_1 + C_2)/C_3 \right]. \quad (3)$$
Fig. 1. Circuit Illustrating Operating Principle

Neglecting the higher order terms in Eq.(3) is valid since typically $C_i = 100 \, \text{pF}$, $C_a < 200 \, \text{pF}$, and $C_e = 2 \, \mu\text{F}$. The modification of less than $200 \times 10^{-6}$ ($200 \, \text{ppm}$) can be treated either as a permanent addition to $C_i$ or removed with additional compensating circuits. The simplest circuit consists of a capacitor, $C_i'$, having the value of $(C_1+C_a)/(C_i/C_e)$. Assuming such a compensation, and adjusting the closed-loop gain of the amplifier $A_2$ so that $(R_1+R_2)/R_1 = C_2/C_2 (1 - d)$, we obtain the condition described by Eq.(2).

Detailed Circuit

The detailed circuit is shown in Fig. 2. The principal feedback amplifier loop contains amplifiers $A1$, $A3$, and $A4$ and has a gain of approximately 3000 provided by $A1$. $A1$ has a local feedback via $A2$ and a double-lag network to provide dc feedback. The T-network between $A1$ and $A3$ stabilizes the loop at high frequencies. The controlled source consists of $A6$ and $A7$ with a nominal gain of 2. The gain is adjustable using variable resistors $R40$ and $R41$ to exactly match the required value. $R32$ and $C4$ stabilize this loop at high frequencies. Although the controlled source is in a closed-loop configuration, at operating frequencies the loop gain is nearly zero due to the rest of the circuit. The combination operates effectively on an open-loop basis.

The power stage is a dual operational amplifier circuit, as described in [1], with a fixed gain of 10 that increases the output voltage to 120 V. All the passive components that affect the ratio are of the precision type. The low-voltage capacitors have polystyrene dielectrics; any residual dissipation factor of these capacitors is compensated with an RC T-network [1]. The resistors are wire-wound with low temperature coefficients.

Preliminary Test Results

The circuit was simulated using network analysis software with realistic models of components, including the operational amplifiers. This demonstrated that the circuit should be dynamically stable and that the summing-point voltage (input to $A1$) can be reduced to a negligible value. The stability was then verified in practice. Initially the controlled source was adjusted to bring the summing-point voltage to zero, then monitored, in amplified form at the output of $A1$ over a four-day period, for any drift. For an output voltage of 6 V, the voltage at the output of $A1$ did not exceed $200 \, \mu\text{V}$ (or equivalently, $70 \, \text{nV}$ at the input to $A1$), yielding a relative error contribution well below $1 \times 10^{-6}$ (1 ppm) and below the noise level of the circuit. This suggests that the gain instability of the controlled source is less than $10^{-4}$. Further tests were conducted to verify that the capacitors have temperature coefficient of capacitance in the specified $-10^2 \degree\text{C}$ range and negligible voltage dependence in the 0 V to 12 V operating range.

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Reference