

Operating Margins for a Superconducting Voltage Waveform Synthesizer

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Abstract—Operating margins for a bipolar superconducting voltage waveform synthesizer were measured. Current ranges were determined for 101 equally spaced dc voltage steps between -18.6 and $+18.6$ mV. The measured voltages of these steps deviated from the expected voltages by less than ± 0.6 μ V.

I. INTRODUCTION

We are developing a superconducting Josephson digital-to-analog converter as an accurate time-dependent voltage waveform synthesizer with precise spectral output for both amplitude and frequency [1]-[4]. The original circuit of the pulse-driven Josephson digital-to-analog converter uses an input drive of pulses [1]-[2]. Unfortunately, this technique is limited to the generation of unipolar ac waveforms. We recently demonstrated that bipolar waveforms could be synthesized by using a combined input drive consisting of a two-level bias representing the digital code and a sine wave [3]-[4]. This combined input drive provides a six-fold increase in output voltage compared to the original circuit using the same high-speed digital code generator. Bipolar ac generation is an important step toward achieving practical output voltages greater than or equal to 1 V.

In this paper, we confirm the functionality of the bipolar voltage waveform synthesizer by measuring the time-averaged dc voltage of an array of junctions for 101 different patterns of a 100 bit-long code. We demonstrate that the operating current margins are greater than 1.1 mA for every one of 101 equally spaced dc voltages between -18.6 and $+18.6$ mV. We show that the measured voltage agrees with the expected theoretical voltage within ± 6 parts in 10^6 . We discuss measured harmonic spectra of sine waves that were synthesized using the optimized bias conditions determined from the 100 bit codes. Undesirable harmonics in these ac waveforms were reduced to 80 dB below the fundamental.

II. BIPOLAR VOLTAGE GENERATION

In this section we describe how bipolar ac and dc voltages are generated. When a Josephson junction is biased with a sinusoidal microwave signal $I_{ac}\sin(2\pi ft)$, with frequency f and amplitude I_{ac} , its dc voltage-current characteristic exhibits constant voltage steps at $V_n = n\Phi_0 f$. The flux quantum $\Phi_0 = h/2e$ is the ratio of Planck's constant and twice the electron charge. The step voltage is the time-averaged value of many junction voltage pulses. The quantum step number n is an integer $0, \pm 1, \dots$ that corresponds to the number and polarity of quantized voltage pulses per period of the sinusoidal drive $1/f$. The time integral of every pulse is precisely equal to the flux quantum. In Fig. 1, we show that the center of the current range of the $\pm n$ th step is selected by appropriately choosing bias current $\pm I_0$.

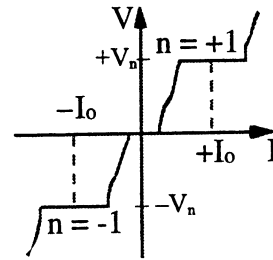


Fig. 1. Simulated voltage-current curve of a sinusoidally driven, resistively shunted Josephson junction showing constant voltage steps.

Bipolar pulse-quantized waveforms are generated by direct control of individual pulses of both polarities, such as those on the $+n$ and $-n$ steps. Pulses of either polarity can be selected by rapidly switching the dc current bias between these steps at a rate comparable to and synchronized with the sinusoidal drive frequency. Time-averaged dc voltages between the values $+V_n$ and $-V_n$ are generated by repeating periodic sequences of high and low biases to generate the appropriate number and polarity of pulses. The appropriate pulse sequence for a given voltage is created by using a digital code that specifies the timing of the high $+I_0$ and low $-I_0$ current biases. Thus, the sine wave frequency determines the maximum and minimum voltages that can be synthesized, whereas the digital code specifies the particular voltage within this range. In general, any dc voltage $(p-q)V_n/(p+q)$ can be generated using a digital code with p 1's and q 0's. For example, a periodically repeated 10 bit code of six 1's and four 0's yields a time-averaged voltage $+0.2V_n$. A code of all 0's gives the minimum output voltage $-V_n$.

Similarly, time-dependent periodic voltage waveforms are synthesized by repeating more complex bit patterns. The peak amplitude of these bipolar ac waveforms is $+V_n$. Figure 2(a) shows an example of how a sine wave is generated using a two-level digital code. The sine wave peak amplitude corresponds to the highest density of 1's. The nodes correspond to an equal density of 1's and 0's.

Figure 2(b) shows a block diagram of the method used to synthesize a sine wave of frequency f_1 or any other bipolar periodic waveform $S(t)$ using quantized pulses. The modulator algorithm is a computer program that digitizes the input waveform and creates a digital code $S(i)$ of length N_s at a sampling frequency f_s . The digital code generator re-creates this two-level code as a bipolar output voltage in real time $S_D(t)$ by clocking its memory at the sampling frequency. The two-level high-speed code is combined with a sinusoidal drive of frequency f using a directional coupler, indicated by "C". The sinusoidal drive frequency must be locked to the code generator's clock in order to prevent phase drift between the two drive signals. The combined signal is used to current-bias the Josephson quantizer consisting of either a single junction or an array of junctions. A three-pole low-pass Butterworth filter is used to remove unwanted

quantization noise from the spectrum of the quantizer output signal $S_J(t)$, leaving the desired waveform $S'(t) \approx S(t)$. Knowledge of the digital code, the drive frequency, and the number of junctions in the array is sufficient to precisely calculate the output waveform.

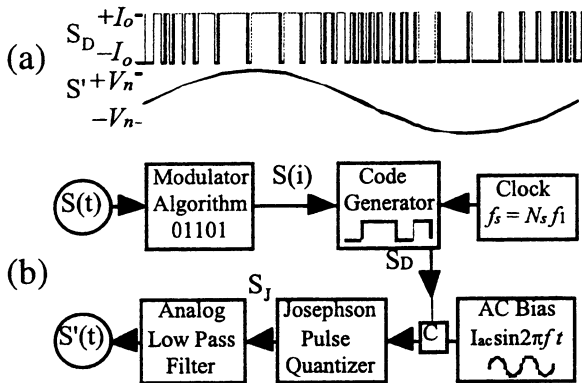


Fig. 2. (a) A two-level high-speed bias corresponding to the digital code of a synthesized sine wave S' . (b) A block diagram of the synthesized bipolar voltage source based on a Josephson junction pulse quantizer. "C" designates a directional coupler.

The sinusoidal frequency should be at precisely half-integral multiples of the sampling frequency $f = mf/2$, where the integer $m \geq 2$ [4]. The optimum operating margins occur when m is an odd integer and when the sine and clock signals are "in phase," that is, when transitions between different bits of the code signal are in the opposite direction from the rising or falling edge of the sine wave. Under these frequency (odd m) and phase conditions, all of the steeply rising edges are removed from the combined input code, provided that the code is separated into three pairs of consecutive bits, Low (00), Medium (01), and High (11). The (10) pattern is excluded because it produces steeply rising edges. Both the dc and ac input waveforms presented in this paper were generated under these conditions.

III. DC VOLTAGE MEASUREMENTS

The operating current range of the bipolar voltage synthesizer can be determined by measuring the current range of dc voltage steps that correspond to different digital codes. The range that is common to all codes is the total operating current range of the device. We investigated a small set of 101 codes for a 100 bit pattern to demonstrate the functionality of the bipolar synthesizer.

Measurements were performed on an array of 1000 Nb-PdAu-Nb Josephson junctions distributed along a 7 mm length of 50 Ω Nb coplanar waveguide [5]. The critical current of each junction in the array is about 4.1 mA, and the resistance of each junction is about 3.8 m Ω . The transmission line is terminated with a 50 Ω PdAu resistor. Four-point measurements of the array are made using four bias taps. Each tap has a 50 Ω resistor close to the transmission line.

The array was driven with a 9 GHz sine wave, and the digital code generator was clocked at 2 GHz ($m = 9$). The code generator's rise time is 30 ps, about 25 % of the sine period. A digital voltmeter was used to measure the voltage

of 101 equally spaced dc voltages between +18.6 and -18.6 mV.

We generated alternating positive and negative voltages starting with the maximum (all 1's) and minimum (all 0's) and decreasing toward 0 V (alternating 01 pattern). For each iteration, the positive and negative voltage patterns were changed by appending 01 to the right end of each 100 bit-long code. The resulting measurement sequence was +18.6, -18.6, +18.2, -18.2, ..., +0.4, -0.4, 0 mV. Each pattern corresponds to different harmonic components of the input. Each voltage can be generated using a number of different patterns, each with its own harmonic signature. Thus, the 101 patterns measured here are only a subset of all possible patterns for these particular voltages, even within the set of 100 bit-long codes.

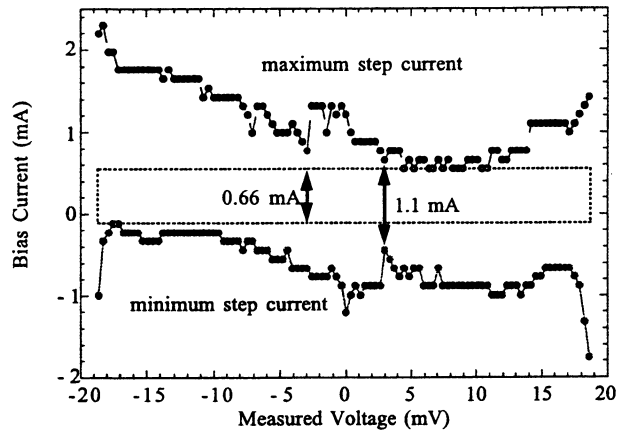


Fig. 3. Maximum and minimum bias currents as a function of the measured voltage showing the current range for 101 digitally synthesized patterns of a 100 bit code. The 1000 junction array was biased with a 9 GHz sine wave, and the code generator was clocked at 2 GHz. The dashed box indicates the common operating current range of all 101 patterns.

Figure 3 shows the current range of each pattern as a function of the measured voltage. The step edges were determined using a large 6 standard deviation search criterion. The voltmeter averaged each voltage measurement over 20 power line cycles. The current range for all 101 patterns is greater than 1.1 mA. The smallest current range occurs for the pattern corresponding to about 3 mV. Although the current range of all steps is greater than 1.1 mA, the combined operating range for all 101 patterns is only 0.66 mA, as indicated by the dashed box in Fig. 3.

Figure 4 shows the measured voltage deviation from the expected voltage with the thermal voltage subtracted for the 101 different 100 bit patterns. The *measured* voltage for each pattern is the *average* of all points on each step when the voltage was measured over the full current range of the step in 100 μ A increments (≥ 11 points each). The *expected* voltage is the voltage $(p-q)Nmf [K_{J,90} (p+q)]^{-1}$ calculated using the Josephson constant $K_{J,90} = 483\,597.9$ GHz/V and the number of junctions N . The thermal voltage is estimated from consecutive patterns with voltages of opposite polarity. The thermal voltage drift over the 75 minute measurement is about 1.3 μ V. The measured voltage agrees with the expected voltage within ± 0.6 μ V, or ± 6 parts in 10^6 of the

full-scale voltage for this 100 mV range. However, the analog-to-digital linearity of the nanovoltmeter is only 50-66 nV for our 20 mV measurements. This suggests that the average measured voltage contains points where the step is not flat, probably near the edges. Thus a finer search criterion (<6 standard deviations) should be used to determine the step edges, and the midpoint of the steps should be used to determine the best average voltage.

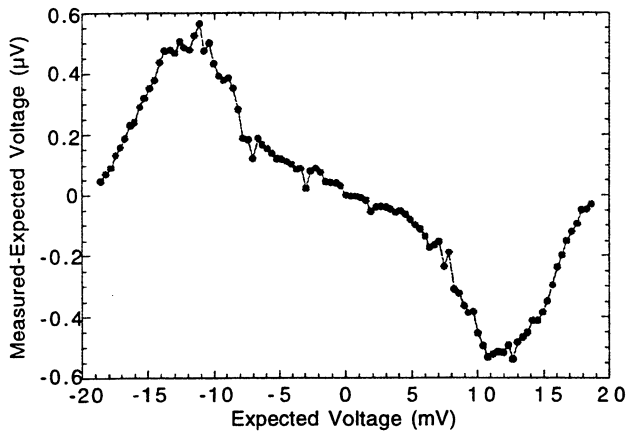


Fig. 4. Deviation of the average measured voltage from the expected voltage with the thermal voltage subtracted for 101 different patterns of a 100 bit code.

IV. DISCUSSION

Since the voltage comparison data suggest that the steps are not flat, the true operating current range may be even smaller. However, even the "best" data above achieve the optimum operating current range (0.66 mA) for only a narrow range of bias conditions. These other important bias conditions determine the complete operating margins of the array and include the sine wave amplitude, the code generator amplitude, and the relative phase delay between the generator and the sine wave. For this set of codes, two patterns were extremely sensitive to the generator amplitude and phase delay, producing a non-zero current range for all 101 patterns only at single generator amplitude. The phase delay was adjusted four times during the measurement set (13 ps total shift) for optimum performance. This suggests that other patterns, either of 100 bit length for the same voltages or longer patterns yielding finer voltage resolution, may have zero operating current range.

Measurements of synthesized low-frequency ac waveforms, in particular a sine wave with 524 288 bits, confirm the lack of operating margins for very long bit patterns. Operating margins exist only if all bias parameters can be varied over a finite range with no change in the output. For these waveforms, we find only a single set of bias conditions that yields the lowest unwanted harmonics [3]. For example, a 3.8 kHz sine wave synthesized using the above "optimized" parameters successfully reduced higher harmonics to -80 dB (carrier), about 50 dB lower than the code generator output, as has been demonstrated previously [2], [3]. The 9 GHz input sine wave amplitude could be varied from -10 to -10.6 dBm. The phase could be shifted by about 4 ps. But single values for the code generator amplitude and offset

(100 μ V increments) were required to minimize the harmonics.

V. CONCLUSIONS

The dc voltage measurements of different patterns and the spectral measurements of ac voltage waveforms both demonstrate the difficulty in achieving operating margins for this broadband circuit. Depending on the digital code pattern, the input waveform contains different harmonics over the range from dc to 9 GHz. Any distortion of these harmonics will distort the input waveform and decrease the operating margins. The most likely cause of our poor operating margins are that the resistive bias taps are inadequate as low pass filters. In future circuit designs we hope to improve the broadband design of our circuit by developing lumped superconducting low-pass filters and arrays, whose dimensions are smaller than one-fourth of the wavelength of the sine wave drive frequency.

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